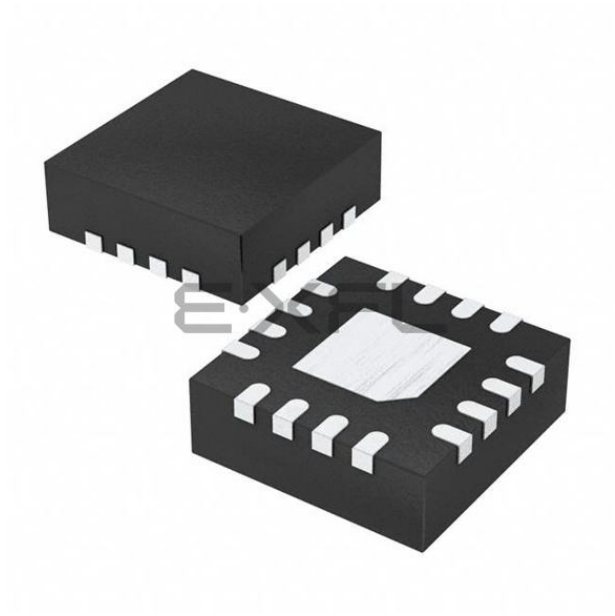

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f610-i-ml

4.0 I/O PORTS

There are as many as eleven general purpose I/O pins and an input pin available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 4-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Reading the PORTA register (Register 4-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note:	The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

EXAMPLE 4-1: INITIALIZING PORTA

```
BCF    STATUS,RP0      ;Bank 0
CLRF   PORTA           ;Init PORTA
BSF    STATUS,RP0      ;Bank 1
CLRF   ANSEL           ;digital I/O
MOVLW  0Ch             ;Set RA<3:2> as inputs
MOVWF  TRISA           ;and set RA<5:4,1:0>
                       ;as outputs
BCF    STATUS,RP0      ;Bank 0
```

REGISTER 4-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-0	R-x	R/W-0	R/W-0	R/W-0
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **RA<5:0>**: PORTA I/O Pin bit
1 = PORTA pin is > V_{IH}
0 = PORTA pin is < V_{IL}

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1: TRISA<3> always reads '1'.
2: TRISA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

7.0 TIMER2 MODULE (PIC16F616/16HV616 ONLY)

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 7-1 for a block diagram of Timer2.

7.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (FOSC/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

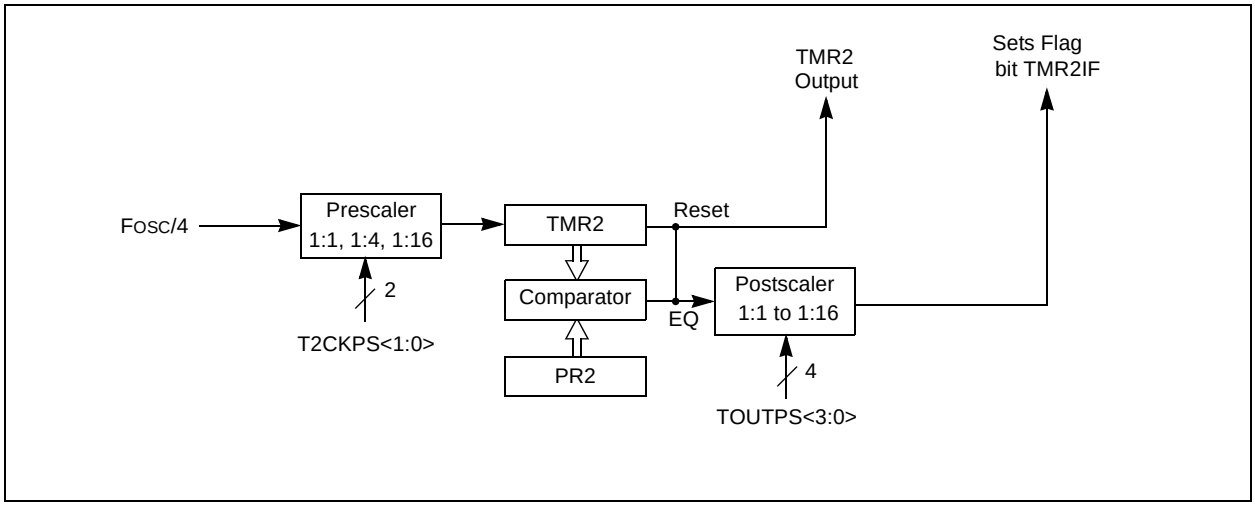
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by setting the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset, or Brown-out Reset).

Note:	TMR2 is not cleared when T2CON is written.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



8.2 Comparator Control

Each comparator has a separate control and Configuration register: CM1CON0 for Comparator C1 and CM2CON0 for Comparator C2. In addition, Comparator C2 has a second control register, CM2CON1, for controlling the interaction with Timer1 and simultaneous reading of both comparator outputs.

The CM1CON0 and CM2CON0 registers (see Registers 8-1 and 8-2, respectively) contain the control and Status bits for the following:

- Enable
- Input selection
- Reference selection
- Output selection
- Output polarity

8.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator for minimum current consumption.

8.2.2 COMPARATOR INPUT SELECTION

The CxCH<1:0> bits of the CMxCON0 register direct one of four analog input pins to the comparator inverting input.

Note:	To use CxIN+ and CxIN- pins as analog inputs, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

8.2.3 COMPARATOR REFERENCE SELECTION

Setting the CxR bit of the CMxCON0 register directs an internal voltage reference or an analog input pin to the non-inverting input of the comparator. See **Section 8.11 "Comparator Voltage Reference"** for more information on the internal voltage reference module.

8.2.4 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CM2CON1 register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CxON bit of the CMxCON0 register must be set.

Note 1:	The CxOE bit overrides the PORT data latch. Setting the CxON has no impact on the port override.
2:	The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

8.2.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 8-1 shows the output state versus input conditions, including polarity control.

TABLE 8-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVIN- > CxVIN+	0	0
CxVIN- < CxVIN+	0	1
CxVIN- > CxVIN+	1	1
CxVIN- < CxVIN+	1	0

8.3 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 15.0 "Electrical Specifications"** for more details.

8.8 Additional Comparator Features

There are three additional comparator features:

- Timer1 count enable (gate)
- Synchronizing output with Timer1
- Simultaneous read of comparator outputs

8.8.1 COMPARATOR C2 GATING TIMER1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CM2CON1 register will enable Timer1 to increment based on the output of Comparator C2. This requires that Timer1 is on and gating is enabled. See **Section 6.0 "Timer1 Module with Gate Control"** for details.

It is recommended to synchronize the comparator with Timer1 by setting the C2SYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

8.8.2 SYNCHRONIZING COMPARATOR C2 OUTPUT TO TIMER1

The Comparator C2 output can be synchronized with Timer1 by setting the C2SYNC bit of the CM2CON1 register. When enabled, the C2 output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 8-3) and the Timer1 Block Diagram (Figure 6-1) for more information.

8.8.3 SIMULTANEOUS COMPARATOR OUTPUT READ

The MC1OUT and MC2OUT bits of the CM2CON1 register are mirror copies of both comparator outputs. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note 1:	Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

REGISTER 8-3: CM2CON1: COMPARATOR 2 CONTROL REGISTER 1

R-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MC1OUT:** Mirror Copy of C1OUT bit

bit 6 **MC2OUT:** Mirror Copy of C2OUT bit

bit 5 **Unimplemented:** Read as '0'

bit 4 **T1ACS:** Timer1 Alternate Clock Select bit
1 = Timer1 clock source is the system clock (FOSC)
0 = Timer1 clock source is the internal clock FOSC/4)

bit 3 **C1HYS:** Comparator C1 Hysteresis Enable bit
1 = Comparator C1 Hysteresis enabled
0 = Comparator C1 Hysteresis disabled

bit 2 **C2HYS:** Comparator C2 Hysteresis Enable bit
1 = Comparator C2 Hysteresis enabled
0 = Comparator C2 Hysteresis disabled

bit 1 **T1GSS:** Timer1 Gate Source Select bit
1 = Timer1 gate source is $\overline{T1G}$
0 = Timer1 gate source is SYNCC2OUT.

bit 0 **C2SYNC:** Comparator C2 Output Synchronization bit
1 = C2 Output is synchronous to falling edge of Timer1 clock
0 = C2 Output is asynchronous

TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3(1)	ANS2(1)	ANS1	ANS0	1111 1111	1111 1111
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
CM2CON1	MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC	00-0 0010	00-0 0010
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	—	ADIE(1)	CCP1IE(1)	C2IE	C1IE	—	TMR2IE(1)	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF	-000 0-00	-000 0-00
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--x0 x000
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 00xx	--uu 00uu
SRCON0	SR1	SR0	C1SEN	C2REN	PULSS	PULSR	—	SRCLKEN	0000 00-0	0000 00-0
SRCON1	SRCS1	SRCS0	—	—	—	—	—	—	00-- ----	00-- ----
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC			TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
VRCON	C1VREN	C2VREN	VRR	FVREN	VR3	VR2	VR1	VR0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used for comparator.
Note 1: PIC16F616/16HV616 only.

TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0(1)	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
ADCON1(1)	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	-000 ----
ANSEL	ANS	ANS6	ANS5	ANS4	ANS3(1)	ANS2(1)	ANS1	ANS0	1111 1111	1111 1111
ADRESH(1,2)	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL(1,2)	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	C2IE	C1IE	—	TMR2IE(1)	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF	-000 0-00	-000 0-00
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--u0 u000
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 00xx	--uu 00uu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

Note 1: PIC16F616/16HV616 only.

2: Read-only Register.

10.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

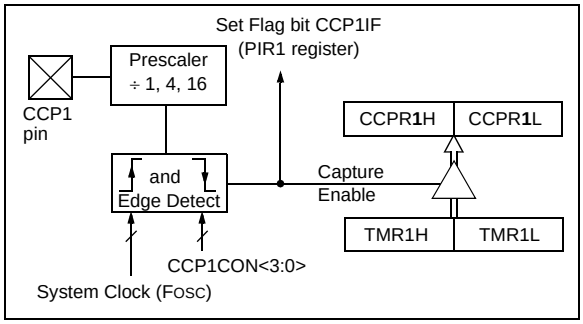
When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 10-1).

10.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCP1 pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 10-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

10.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

10.1.4 CCP PRESCALER

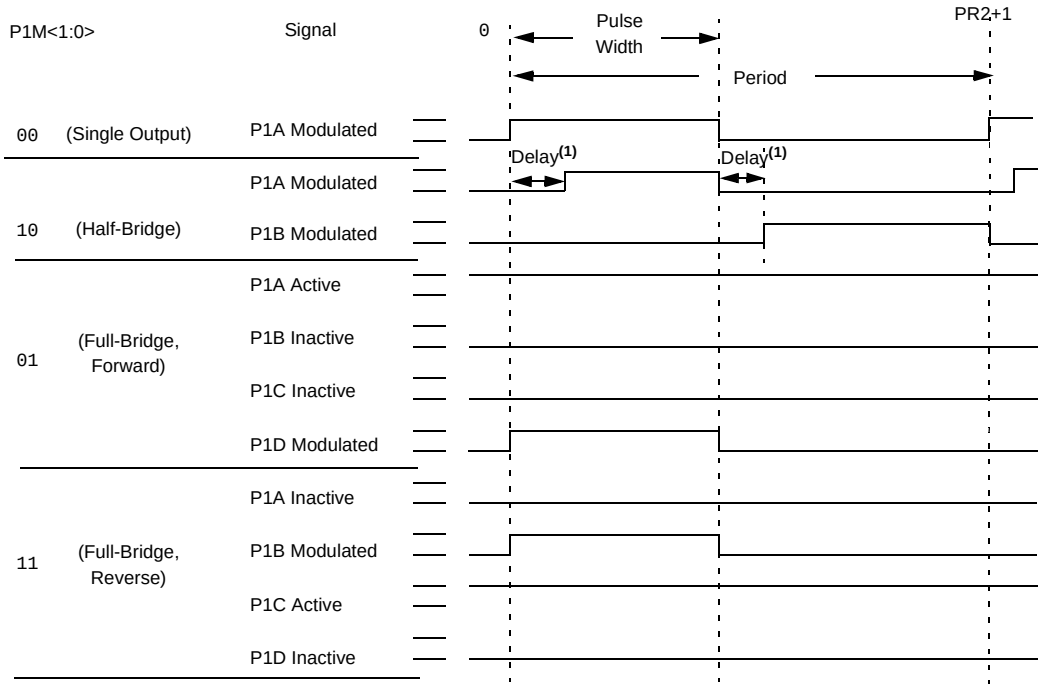
There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 10-1).

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCP1CON     ;Set Bank bits to point
                    ;to CCP1CON
CLRF    CCP1CON     ;Turn CCP module off
MOVLW   NEW_CAPT_PS;Load the W reg with
                    ; the new prescaler
                    ; move value and CCP ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ; value
```

FIGURE 10-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)



Relationships:

- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (PWM1CON<6:0>)

Note 1: Dead-band delay is programmed using the PWM1CON register (**Section 10.4.6 "Programmable Dead-Band Delay mode"**).

10.4.4 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the ECCPASx bits of the ECCPAS register. A shutdown event may be generated by:

- A logic '0' on the INT pin
- Comparator C1
- Comparator C2
- Setting the ECCPASE bit in firmware

A shutdown condition is indicated by the ECCPASE (Auto-Shutdown Event Status) bit of the ECCPAS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The ECCPASE bit is set to '1'. The ECCPASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 10.4.5 "Auto-Restart Mode"**).

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [P1A/P1C] and [P1B/P1D]. The state of each pin pair is determined by the PSSAC and PSSBD bits of the ECCPAS register. Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

REGISTER 10-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ECCPASE:** ECCP Auto-Shutdown Event Status bit
1 = A shutdown event has occurred; ECCP outputs are in shutdown state
0 = ECCP outputs are operating

bit 6-4 **ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits
000 = Auto-Shutdown is disabled
001 = Comparator C1 output high
010 = Comparator C2 output high(1)
011 = Either Comparators output is high
100 = VIL on INT pin
101 = VIL on INT pin or Comparator C1 output high
110 = VIL on INT pin or Comparator C2 output high
111 = VIL on INT pin or either Comparators output is high

bit 3-2 **PSSACn:** Pins P1A and P1C Shutdown State Control bits
00 = Drive pins P1A and P1C to '0'
01 = Drive pins P1A and P1C to '1'
1x = Pins P1A and P1C tri-state

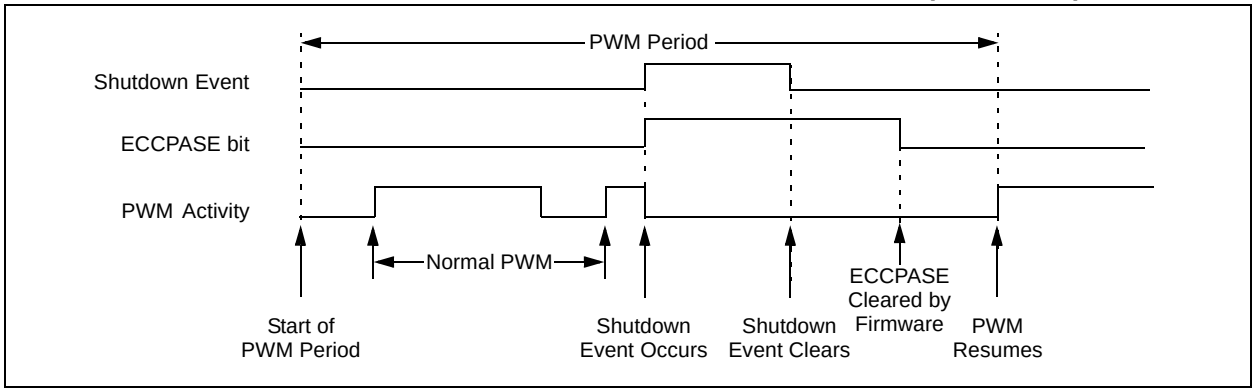
bit 1-0 **PSSBDn:** Pins P1B and P1D Shutdown State Control bits
00 = Drive pins P1B and P1D to '0'
01 = Drive pins P1B and P1D to '1'
1x = Pins P1B and P1D tri-state

Note 1: The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

2: Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

FIGURE 10-14: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)

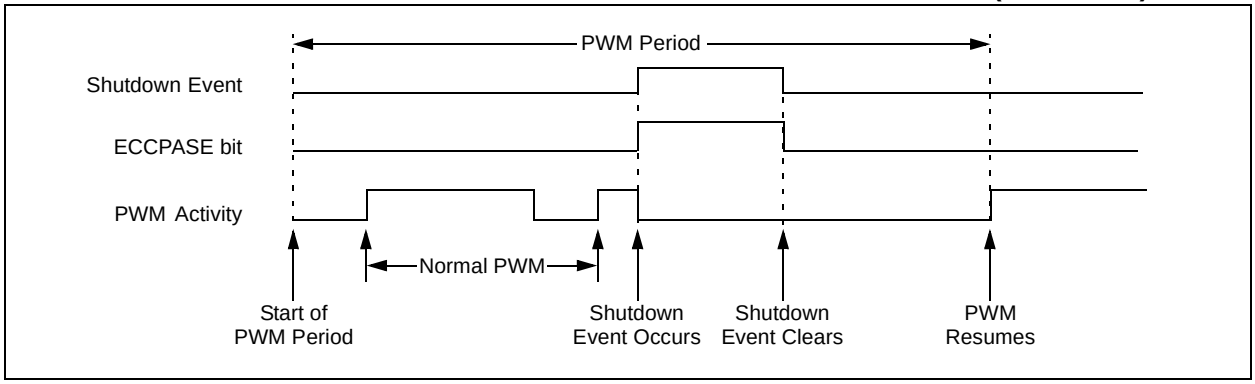


10.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

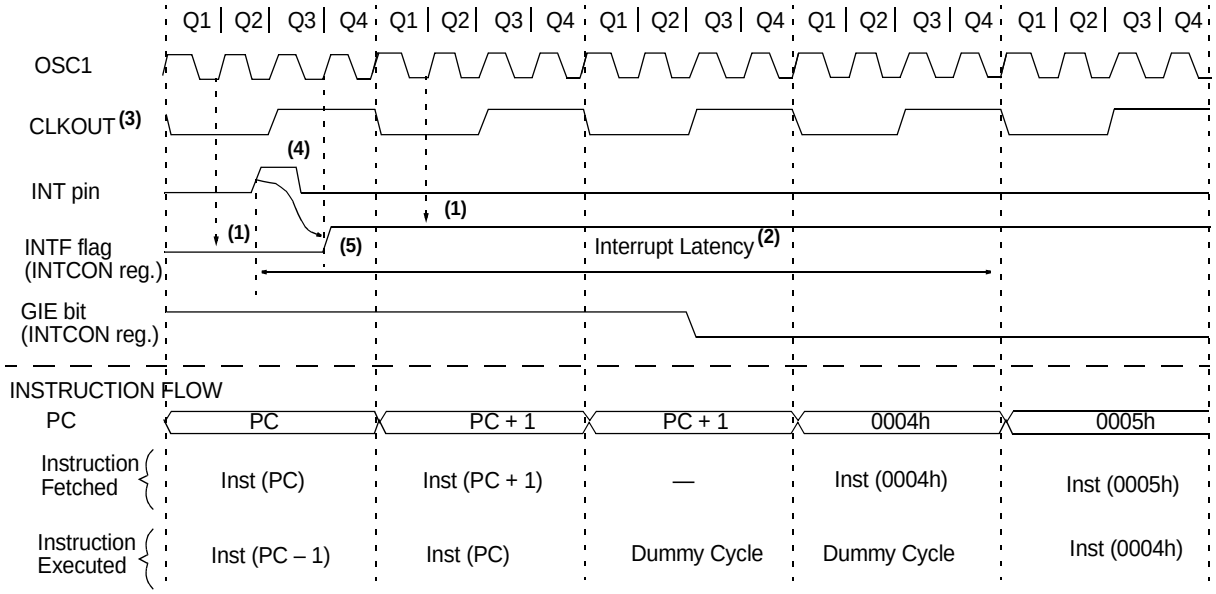
If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

FIGURE 10-15: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)



NOTES:

FIGURE 12-8: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 15.0 "Electrical Specifications"**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
PIR1	—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF	-000 0-00	-000 0-00
PIE1	—	ADIE(1)	CCP1IE(1)	C2IE	C1IE	—	TMR2IE(1)	TMR1IE	-000 0-00	-000 0-00

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the interrupt module.

Note 1: PIC16F616/16HV616 only.

15.5 DC Characteristics: PIC16F610/616-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020E	**Power-down Base Current (IPD)(2)** PIC16F610/616	—	0.05	4.0	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	5.0	µA	3.0	
		—	0.35	8.5	µA	5.0	
D021E		—	0.5	5.0	µA	2.0	WDT Current(1)
		—	2.5	8.0	µA	3.0	
		—	9.5	19	µA	5.0	
D022E		—	5.0	15	µA	3.0	BOR Current(1)
		—	6.0	19	µA	5.0	
D023E		—	105	130	µA	2.0	Comparator Current(1), both comparators enabled
		—	110	140	µA	3.0	
		—	116	150	µA	5.0	
D024E		—	50	70	µA	2.0	Comparator Current(1), single comparator enabled
		—	55	75	µA	3.0	
		—	60	80	µA	5.0	
D025E		—	30	40	µA	2.0	CVREF Current(1) (high range)
		—	45	60	µA	3.0	
		—	75	105	µA	5.0	
D026E*		—	39	50	µA	2.0	CVREF Current(1) (low range)
		—	59	80	µA	3.0	
		—	98	130	µA	5.0	
D027E		—	5.5	16	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	7.0	18	µA	3.0	
		—	8.5	22	µA	5.0	
D028E		—	0.2	6.5	µA	3.0	A/D Current(1), no conversion in progress
		—	0.36	10	µA	5.0	

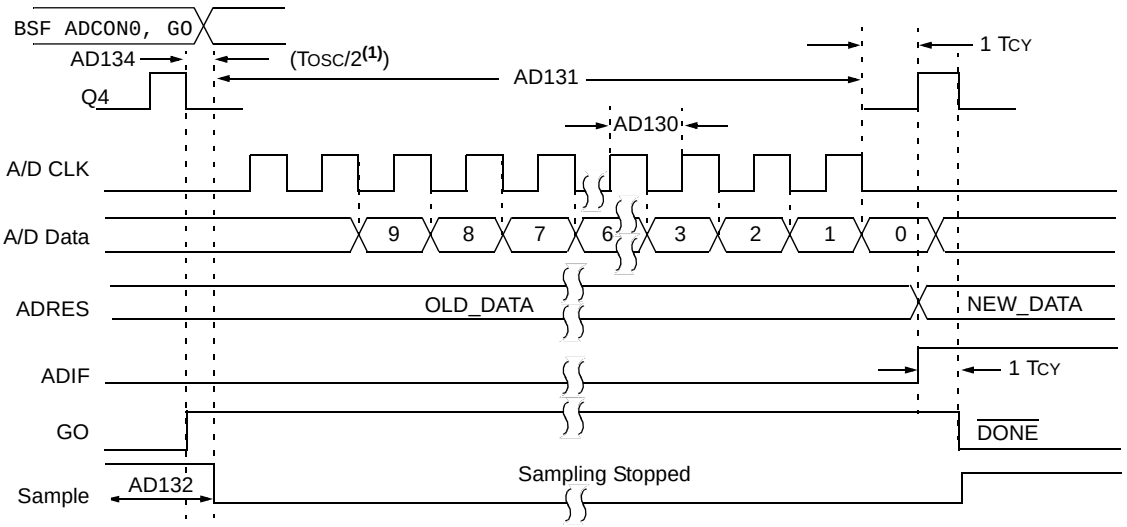
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

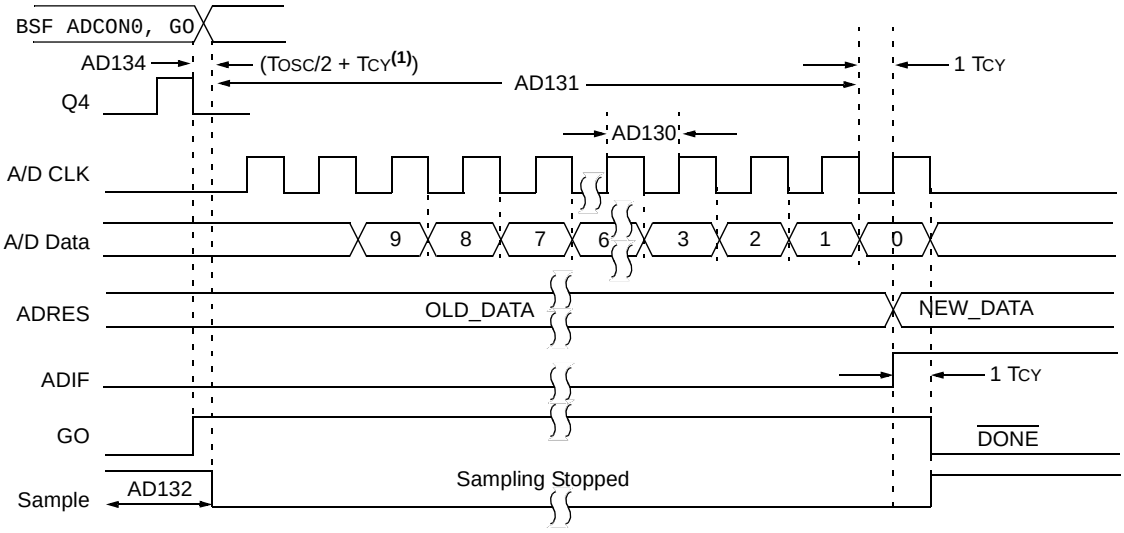
2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

FIGURE 15-12: PIC16F616/16HV616 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

FIGURE 15-13: PIC16F616/16HV616 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-15: DC CHARACTERISTICS FOR I_{PD} SPECIFICATIONS FOR PIC16F616 – H (High Temp.)

Param No.	Device Characteristics	Units	Min	Typ	Max	Condition	
						V_{DD}	Note
D020E	Power Down I_{PD}	µA	—	0.05	12	2.0	I_{PD} Base
			—	0.15	13	3.0	
			—	0.35	14	5.0	
D021E		µA	—	0.5	20	2.0	WDT Current
			—	2.5	25	3.0	
			—	9.5	36	5.0	
D022E		µA	—	5.0	28	3.0	BOR Current
			—	6.0	36	5.0	
D023E		µA	—	105	195	2.0	I_{PD} Current (Both Comparators Enabled)
			—	110	210	3.0	
			—	116	220	5.0	
		µA	—	50	105	2.0	I_{PD} Current (One Comparator Enabled)
			—	55	110	3.0	
			—	60	125	5.0	
D024E		µA	—	30	58	2.0	I_{PD} (C_{VREF}, High Range)
			—	45	85	3.0	
			—	75	142	5.0	
D025E		µA	—	39	76	2.0	I_{PD} (C_{VREF}, Low Range)
			—	59	114	3.0	
			—	98	190	5.0	
D026E		µA	—	5.5	30	2.0	I_{PD} (T1 OSC, 32 kHz)
			—	7.0	35	3.0	
			—	8.5	45	5.0	
D027E		µA	—	0.2	12	3.0	I_{PD} (A2D on, not converting)
			—	0.3	15	5.0	

TABLE 15-16: WATCHDOG TIMER SPECIFICATIONS FOR PIC16F616 – H (High Temp.)

Param No.	Sym	Characteristic	Units	Min	Typ	Max	Conditions
31	T_{WDT}	Watchdog Timer Time-out Period (No Prescaler)	ms	6	20	70	150°C Temperature

TABLE 15-17: LEAKAGE CURRENT SPECIFICATIONS FOR PIC16F616 – H (High Temp.)

Param No.	Sym	Characteristic	Units	Min	Typ	Max	Conditions
D061	I_{IL}	Input Leakage Current(1) (GP3/RA3/$\overline{MCLR}$)	µA	—	±0.5	±5.0	$V_{SS} \le V_{PIN} \le V_{DD}$
D062	I_{IL}	Input Leakage Current(2) (GP3/RA3/$\overline{MCLR}$)	µA	50	250	400	V_{DD} = 5.0V

Note 1: This specification applies when GP3/RA3/$\overline{MCLR}$ is configured as an input with the pull-up disabled. The leakage current for the GP3/RA3/$\overline{MCLR}$ pin is higher than for the standard I/O port pins.

2: This specification applies when GP3/RA3/$\overline{MCLR}$ is configured as the $\overline{MCLR}$ Reset pin function with the weak pull-up enabled.

FIGURE 16-8: PIC16F610/616 IDD EXTRC (4 MHz) vs. VDD

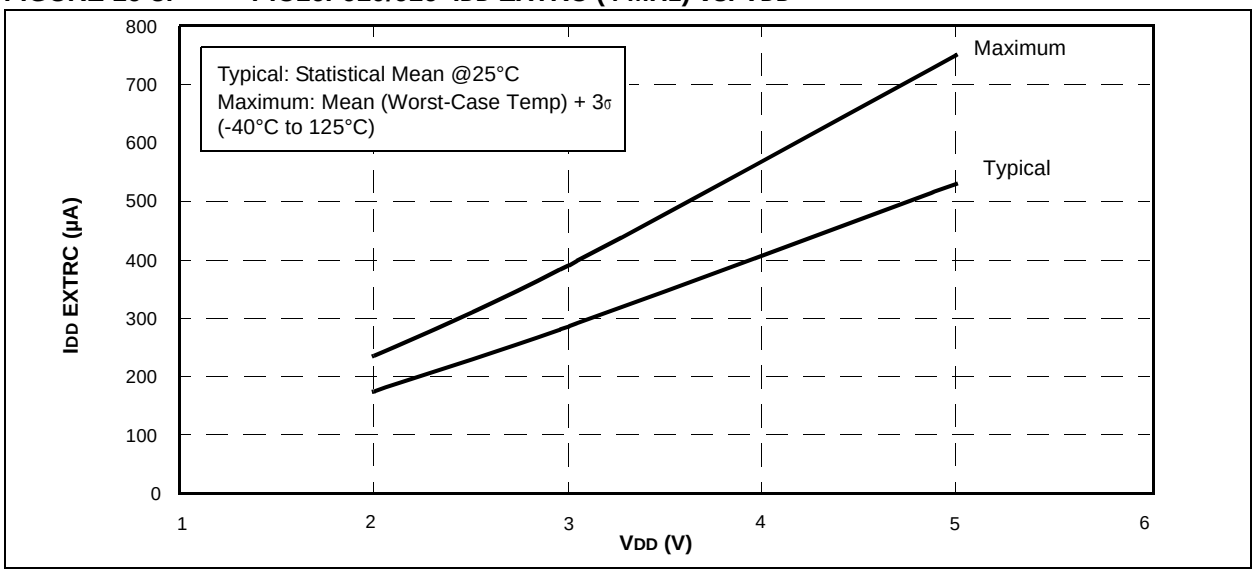


FIGURE 16-9: PIC16F610/616 IDD HS (20 MHz) vs. VDD

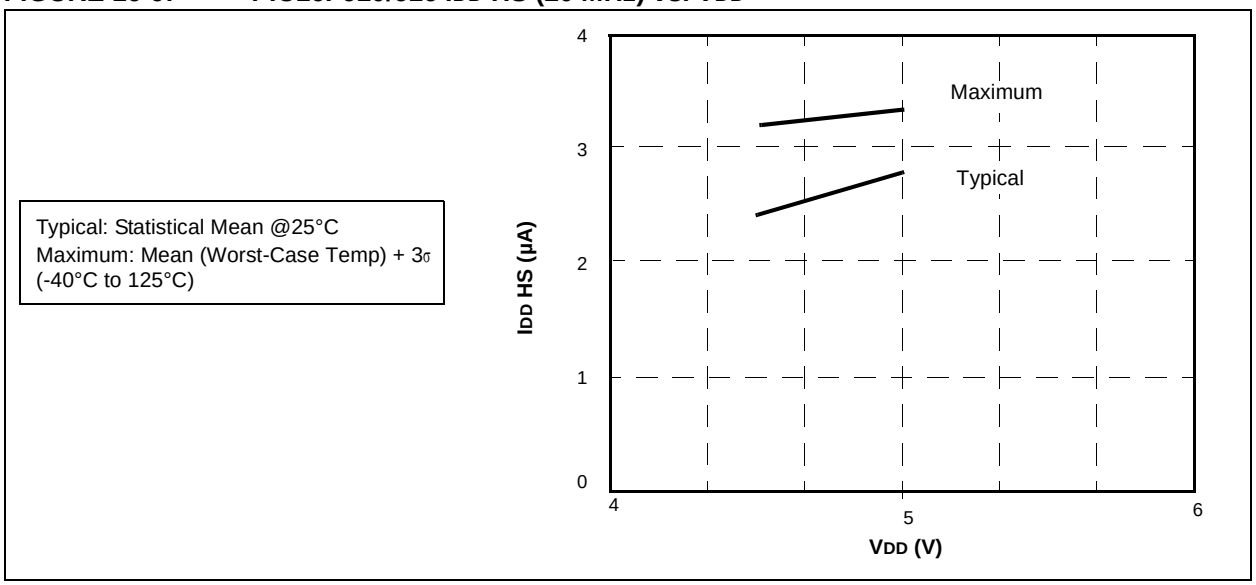


FIGURE 16-29: PIC16HV610/616 IPD COMPARATOR (BOTH ON) vs. VDD

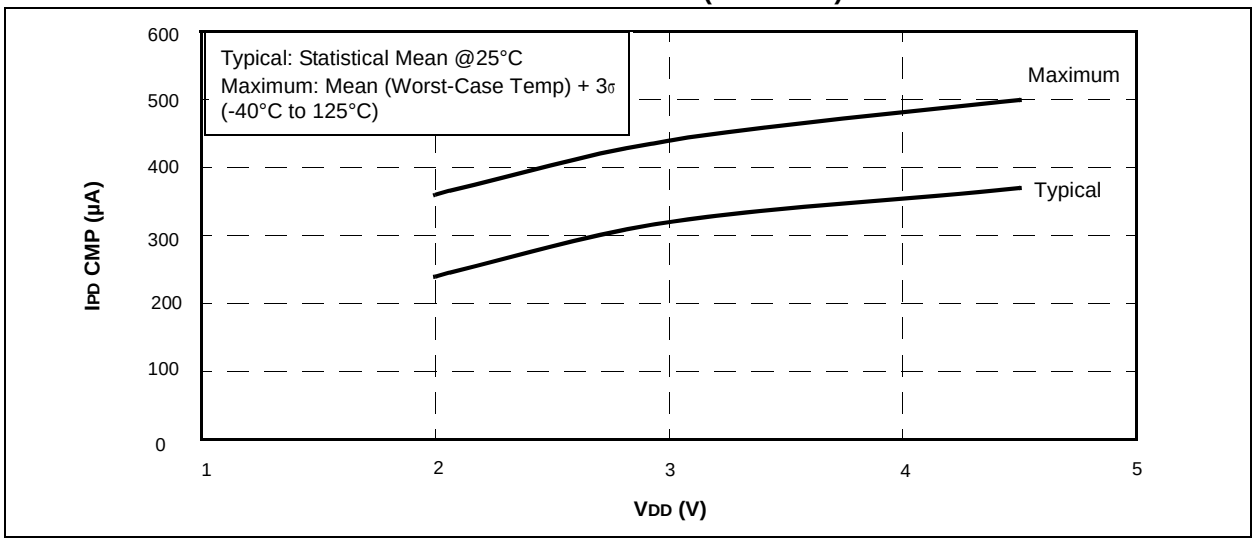


FIGURE 16-30: PIC16HV610/616 IPD WDT vs. VDD

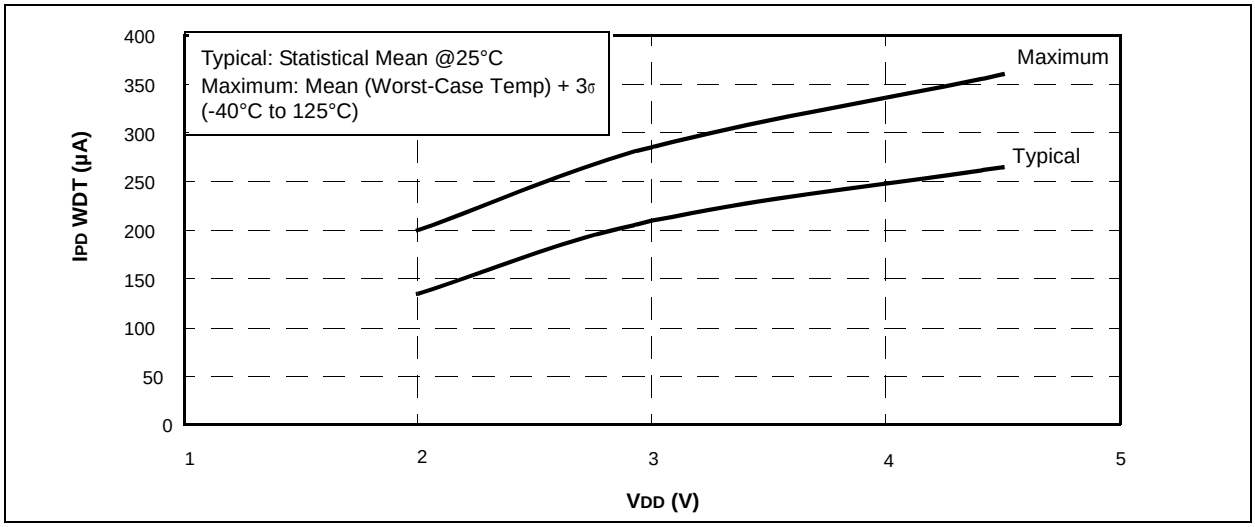


FIGURE 16-31: PIC16HV610/616 IPD BOR vs. VDD

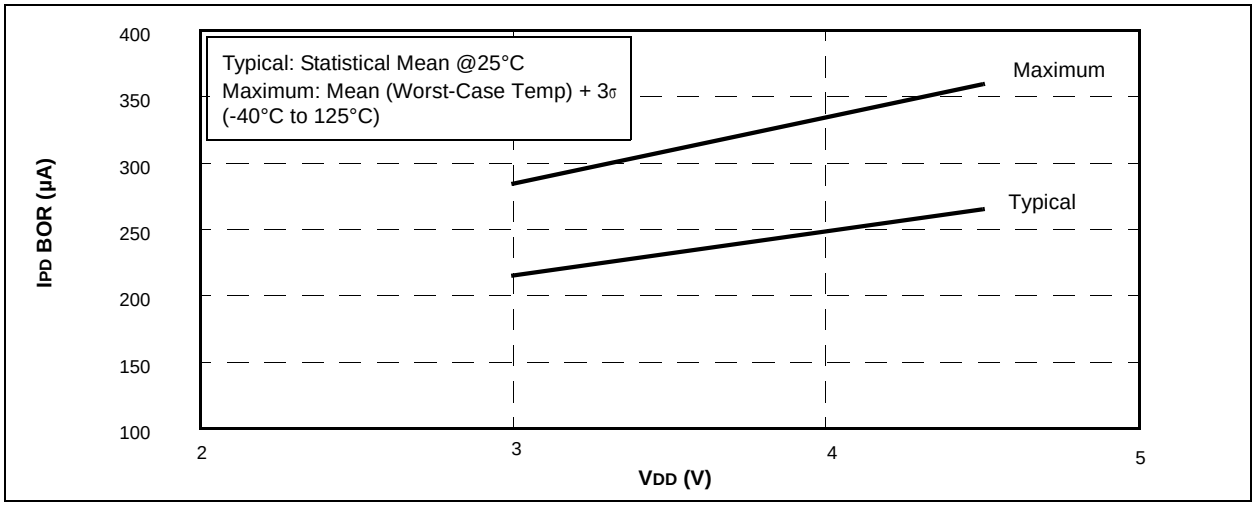


FIGURE 16-35: PIC16HV616 IPD A/D vs. VDD

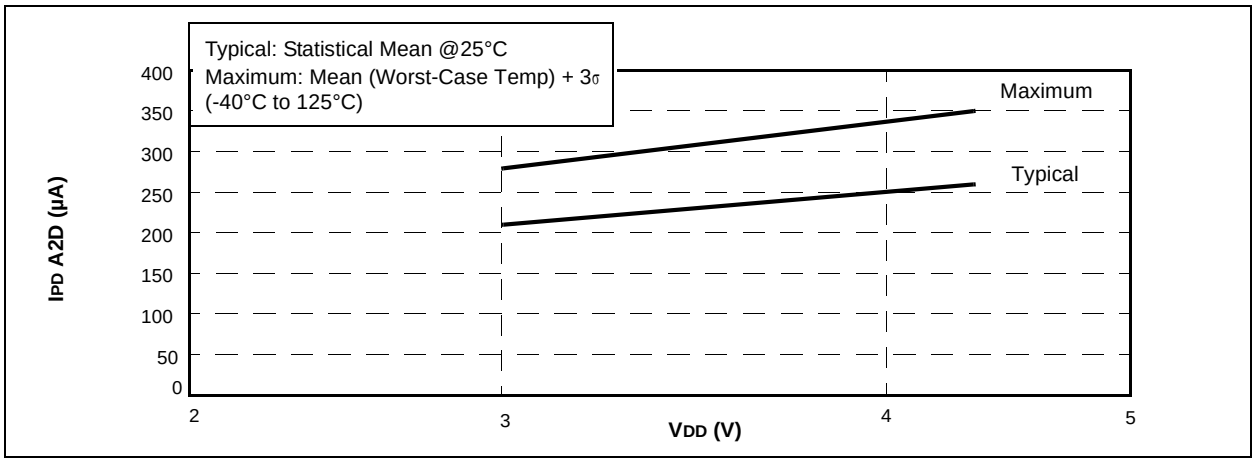
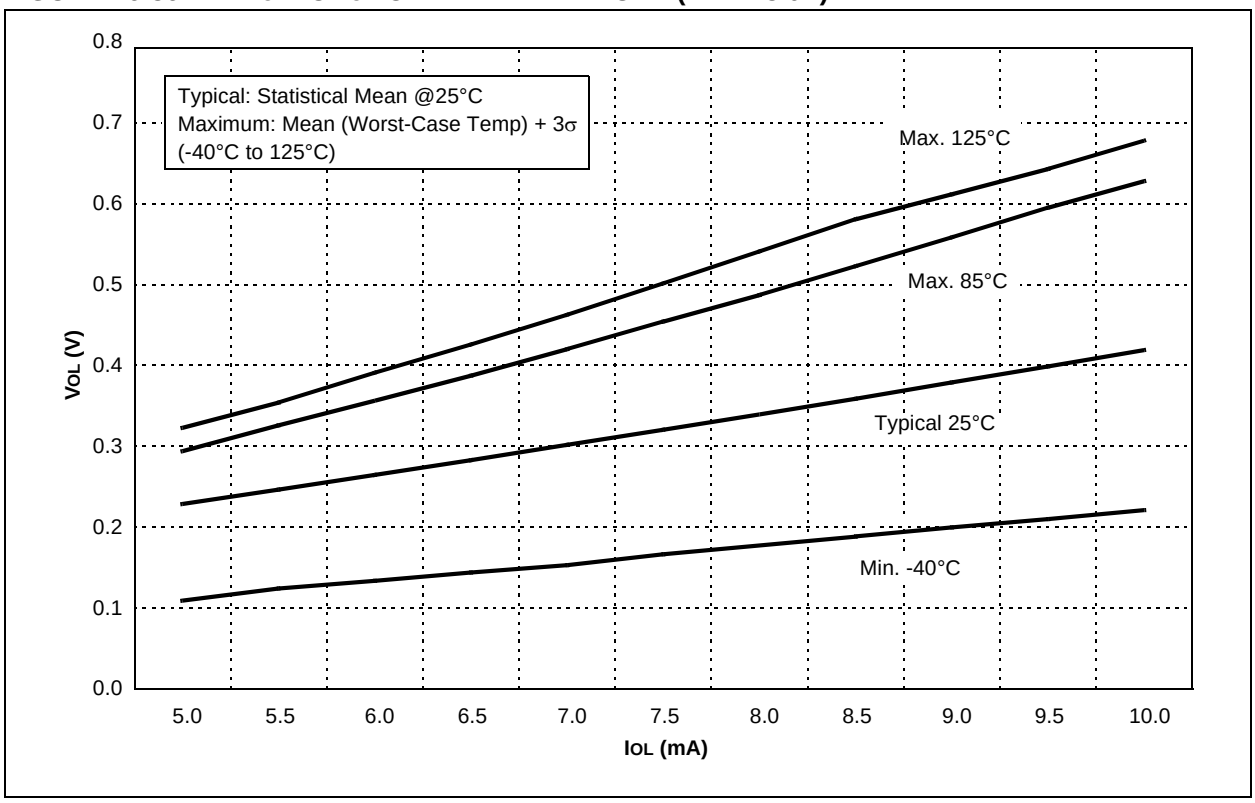
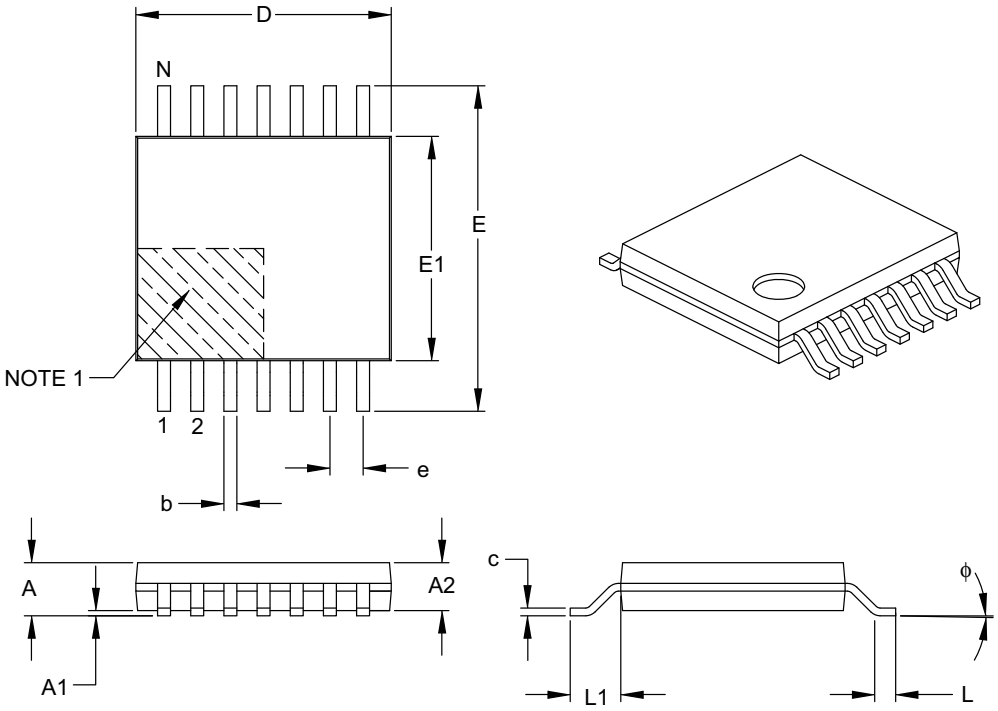


FIGURE 16-36: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)



14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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