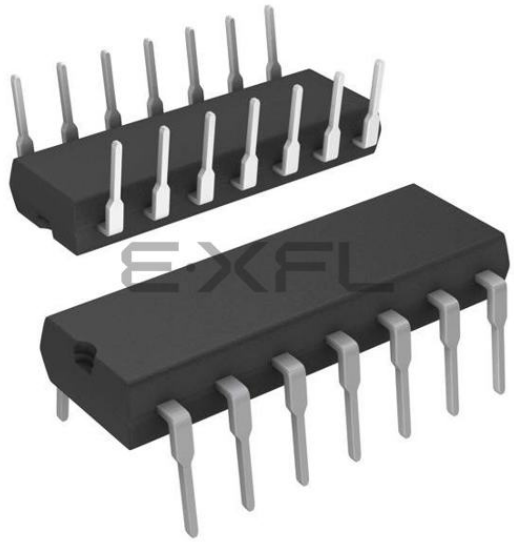

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f610-i-p

Device	Program Memory	Data Memory	I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit	Voltage Range
	Flash (words)	SRAM (bytes)					
PIC16F610	1024	64	11	—	2	1/1	2.0-5.5V
PIC16HV610	1024	64	11	—	2	1/1	2.0-user defined
PIC16F616	2048	128	11	8	2	2/1	2.0-5.5V
PIC16HV616	2048	128	11	8	2	2/1	2.0-user defined

PIC16F610/16HV610 14-Pin Diagram (PDIP, SOIC, TSSOP)

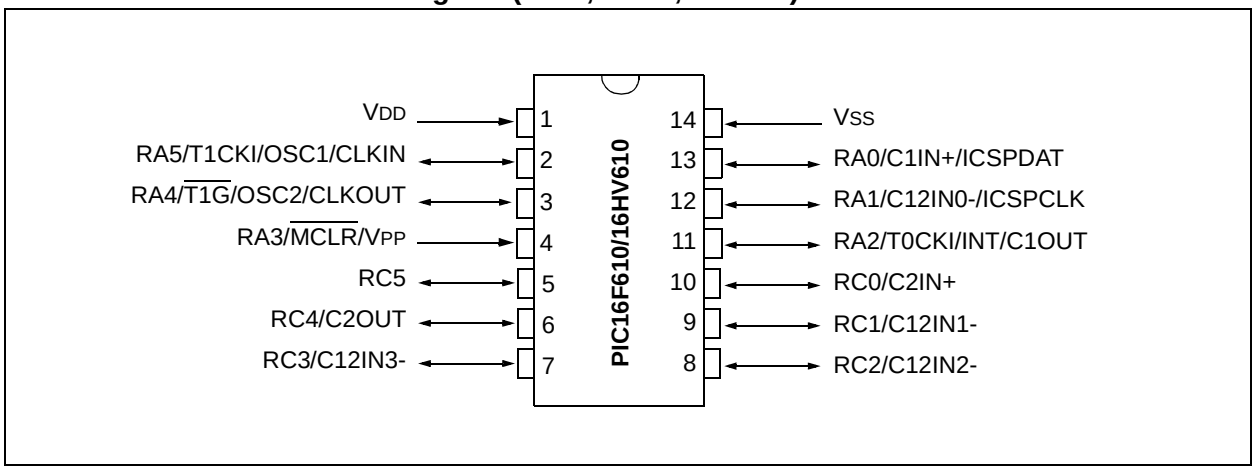


TABLE 1: PIC16F610/16HV610 14-PIN SUMMARY

I/O	Pin	Comparators	Timer	Interrupts	Pull-ups	Basic
RA0	13	C1IN+	—	IOC	Y	ICSPDAT
RA1	12	C12IN0-	—	IOC	Y	ICSPCLK
RA2	11	C1OUT	T0CKI	INT/IOC	Y	—
RA3(1)	4	—	—	IOC	Y(2)	MCLR/VPP
RA4	3	—	T1G	IOC	Y	OSC2/CLKOUT
RA5	2	—	T1CKI	IOC	Y	OSC1/CLKIN
RC0	10	C2IN+	—	—	—	—
RC1	9	C12IN1-	—	—	—	—
RC2	8	C12IN2-	—	—	—	—
RC3	7	C12IN3-	—	—	—	—
RC4	6	C2OUT	—	—	—	—
RC5	5	—	—	—	—	—
—	1	—	—	—	—	VDD
—	14	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS,` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `'000u u1uu'` (where u = unchanged).

It is recommended, therefore, that only `BCF, BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the **Section 13.0 "Instruction Set Summary"**.

Note 1:	Bits IRP and RP1 of the STATUS register are not used by the PIC16F610/616/16HV610/616 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
2:	The C and DC bits operate as a $\overline{Borrow}$ and Digit $\overline{Borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** This bit is reserved and should be maintained as '0'

bit 6 **RP1:** This bit is reserved and should be maintained as '0'

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)
1 = Bank 1 (80h – FFh)
0 = Bank 0 (00h – 7Fh)

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

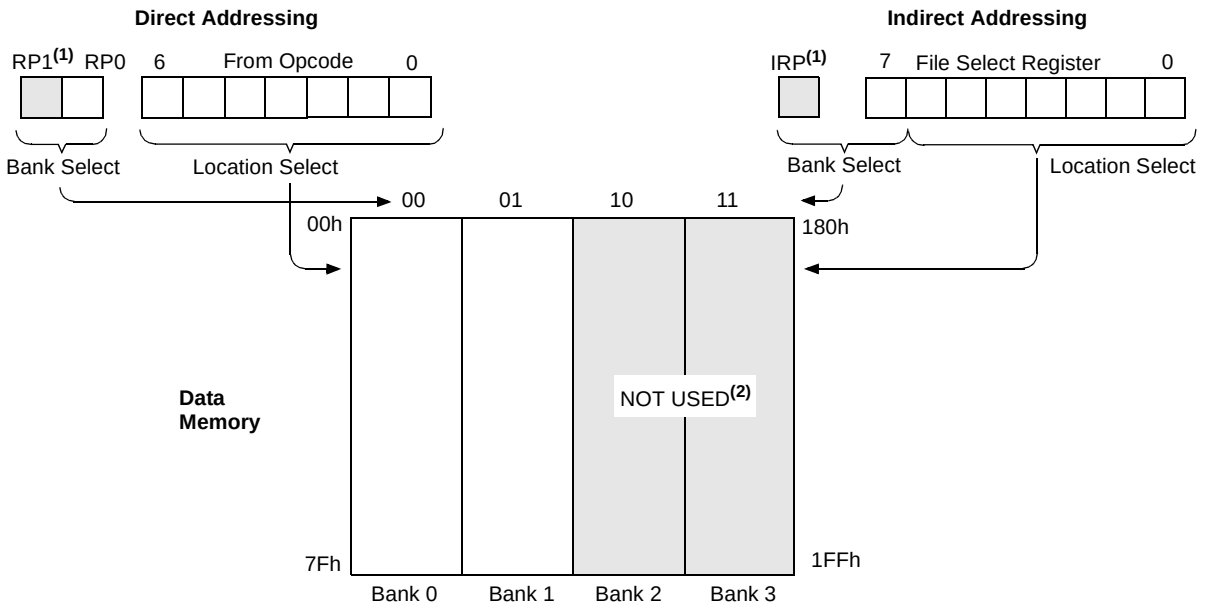
bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF, ADDLW, SUBLW, SUBWF` instructions), For $\overline{Borrow}$, the polarity is reversed.
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF, RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

FIGURE 2-6: DIRECT/INDIRECT ADDRESSING PIC16F610/16HV610



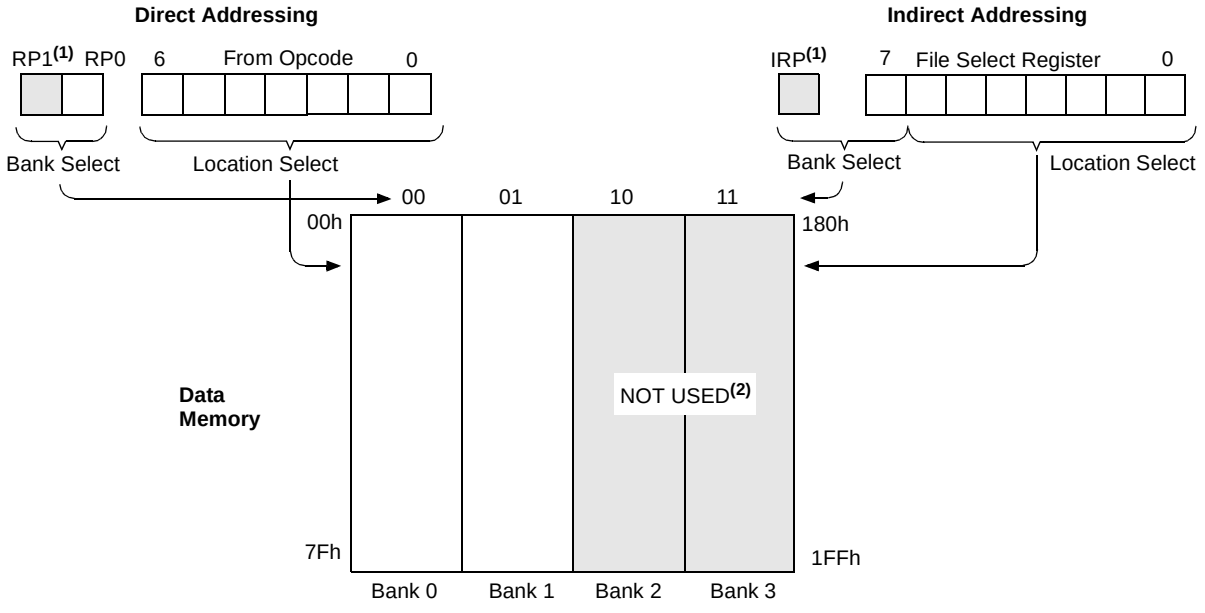
For memory map detail, see Figure 2-3.

Unimplemented data memory locations, read as '0'.

Note 1: The RP1 and IRP bits are reserved; always maintain these bits clear.

2: Accesses in Bank 2 and Bank 3 are mirrored back into Bank 0 and Bank 1, respectively.

FIGURE 2-7: DIRECT/INDIRECT ADDRESSING PIC16F616/16HV616



For memory map detail, see Figure 2-4.

Unimplemented data memory locations, read as '0'.

Note 1: The RP1 and IRP bits are reserved; always maintain these bits clear.

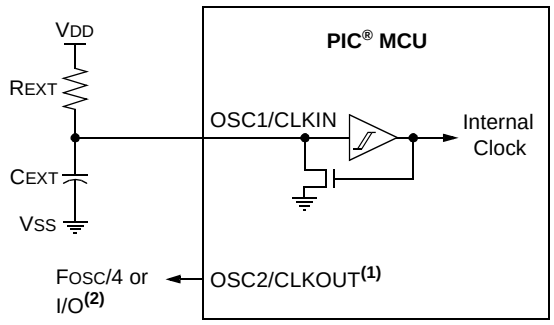
2: Accesses in Bank 2 and Bank 3 are mirrored back into Bank 0 and Bank 1, respectively.

3.3.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the external RC mode connections.

FIGURE 3-5: EXTERNAL RC MODES



Recommended values: 10 kΩ ≤ REXT ≤ 100 kΩ, <3V
3 kΩ ≤ REXT ≤ 100 kΩ, 3-5V
CEXT > 20 pF, 2-5V

Note 1: Alternate pin functions are listed in **Section 1.0 "Device Overview"**.

2: Output depends upon RC or RCIO Clock mode.

In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

3.4 Internal Clock Modes

The Oscillator module provides a selectable system clock source of either 4 MHz or 8 MHz. The selectable frequency is configured through the IOSCFS bit of the Configuration Word.

The frequency of the internal oscillator can be can be user-adjusted via software using the OSCTUNE register.

3.4.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See **Section 12.0 "Special Features of the CPU"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

NOTES:

4.3.1 RC0/AN4(1)/C2IN+

The RC0 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog non-inverting input to Comparator C2

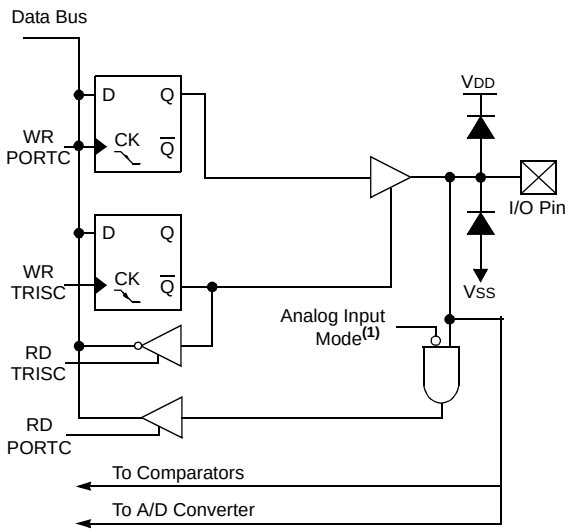
4.3.2 RC1/AN5(1)/C12IN1-

The RC1 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog inverting input to the comparator

Note 1: PIC16F616/16HV616 only.

FIGURE 4-6: BLOCK DIAGRAM OF RC0 AND RC1



Note 1: Analog Input mode comes from ANSEL or Comparator mode.

4.3.3 RC2/AN6(1)/C12IN2-/P1D(1)

The RC2 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog input to Comparators C1 and C2
- a digital output from the Enhanced CCP(1)

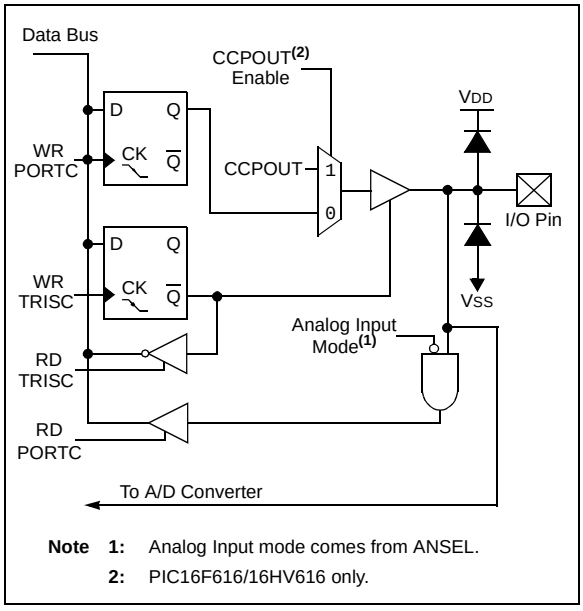
4.3.4 RC3/AN7(1)/C12IN3-/P1C(1)

The RC3 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog inverting input to Comparators C1 and C2
- a digital output from the Enhanced CCP(1)

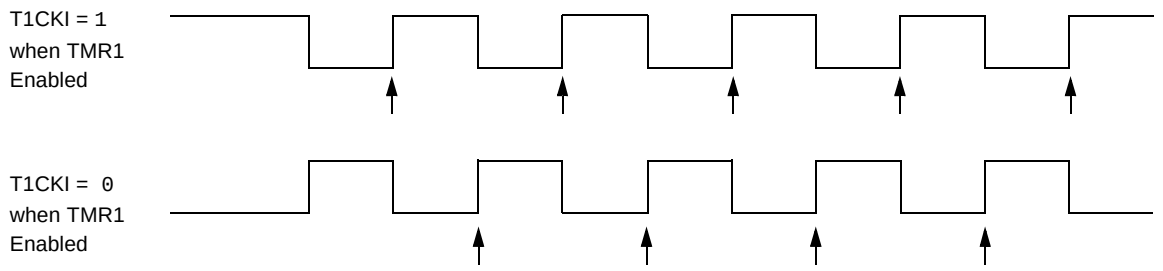
Note 1: PIC16F616/16HV616 only.

FIGURE 4-7: BLOCK DIAGRAM OF RC2 AND RC3



Note 1: Analog Input mode comes from ANSEL.
2: PIC16F616/16HV616 only.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

6.12 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit(1)
1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 6 **TMR1GE:** Timer1 Gate Enable bit(2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 Gate function
0 = Timer1 is always counting

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored

9.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 9-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ $5.0V$ V_{DD}

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 5\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \quad ;[1]\ V_{CHOLD}\ \text{charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad ;[2]\ V_{CHOLD}\ \text{charge response to}\ V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \quad ;\text{combining [1] and [2]}$$

Solving for T_C*:*

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/2047)$$
$$= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885)$$
$$= 1.37\mu s$$

Therefore:

$$T_{ACQ} = 5\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 7.67\mu s$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0(1)	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
ADCON1(1)	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	-000 ----
ANSEL	ANS	ANS6	ANS5	ANS4	ANS3(1)	ANS2(1)	ANS1	ANS0	1111 1111	1111 1111
ADRESH(1,2)	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL(1,2)	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	C2IE	C1IE	—	TMR2IE(1)	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF	-000 0-00	-000 0-00
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--u0 u000
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 00xx	--uu 00uu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

Note 1: PIC16F616/16HV616 only.

2: Read-only Register.

TABLE 10-2: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON(1)	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
CCPR1L(1)	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
CCPR1H(1)	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	C2IE	C1IE	—	TMR2IE(1)	TMR1IE	-000 0-00	0000 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF	-000 0-00	0000 0-00
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.
Note 1: PIC16F616/16HV616 only.

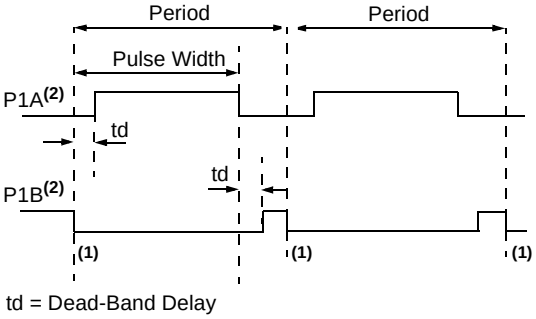
10.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCP1/P1A pin, while the complementary PWM output signal is output on the P1B pin (see Figure 10-8). This mode can be used for half-bridge applications, as shown in Figure 10-9, or for full-bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in half-bridge power devices. The value of the PDC<6:0> bits of the PWM1CON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **10.4.6 "Programmable Dead-Band Delay mode"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure P1A and P1B as outputs.

FIGURE 10-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

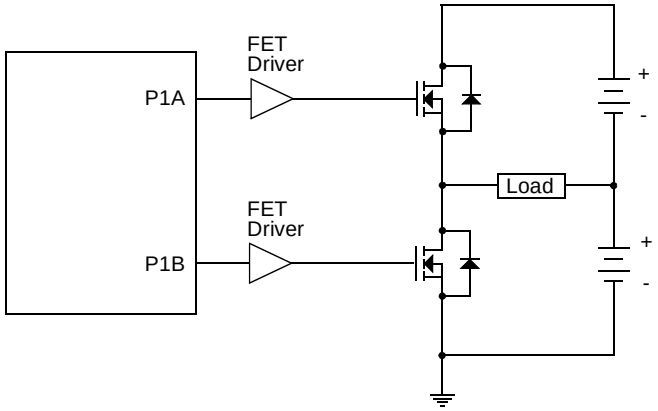


Note 1: At this time, the TMR2 register is equal to the PR2 register.

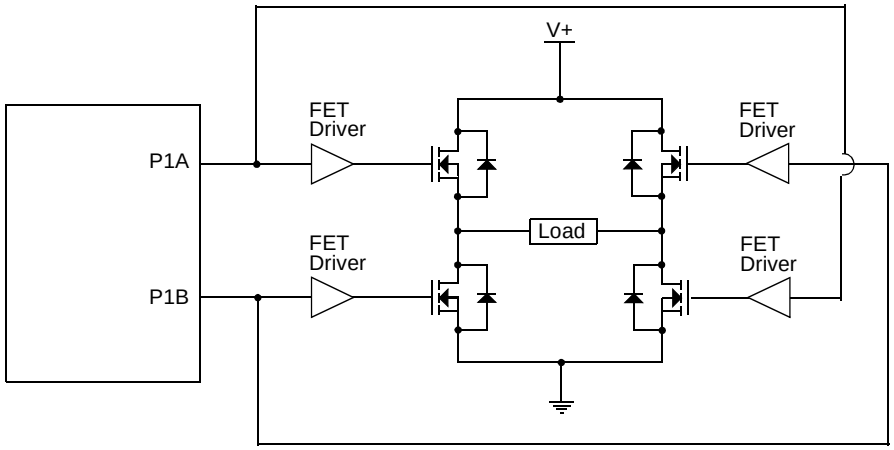
2: Output signals are shown as active-high.

FIGURE 10-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS

Standard Half-Bridge Circuit ("Push-Pull")



Half-Bridge Output Driving a Full-Bridge Circuit



15.0 ELECTRICAL SPECIFICATIONS

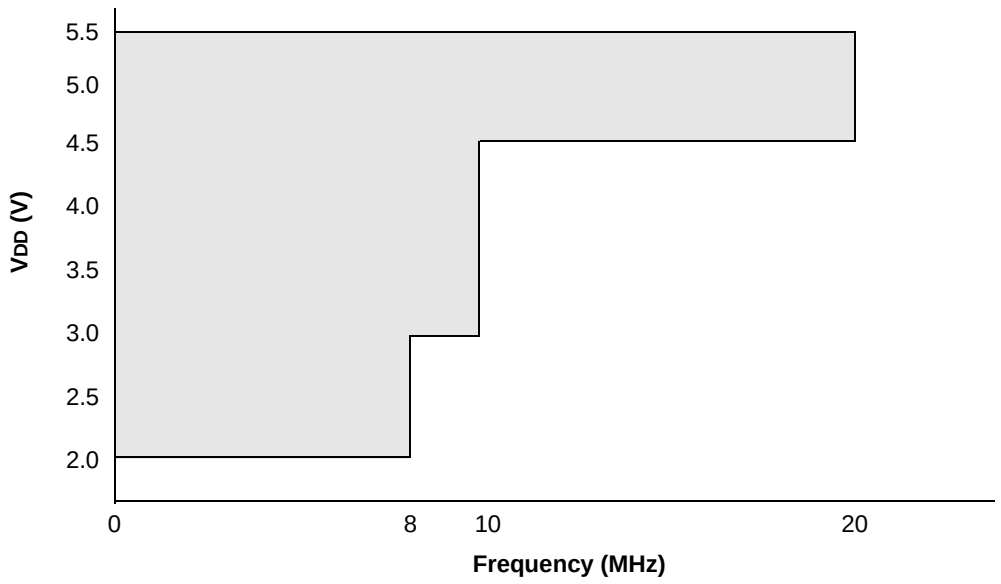
Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40° to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss ..... -0.3V to +13.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 800 mW
Maximum current out of V_{SS} pin ..... 95 mA
Maximum current into V_{DD} pin ..... 95 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ± 20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD}) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA and PORTC (combined) ..... 90 mA
Maximum current sourced PORTA and PORTC (combined) ..... 90 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(Vol \times I_{OL})$.

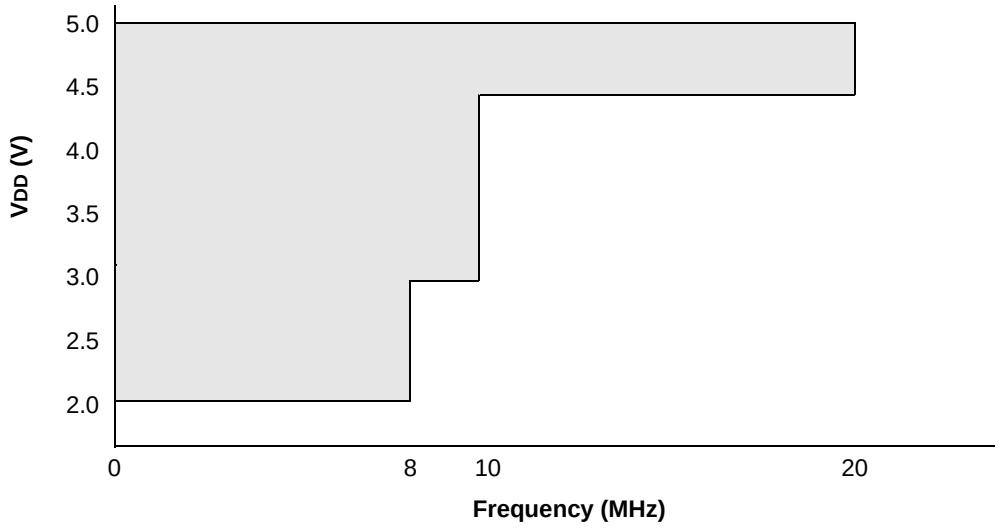
† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

FIGURE 15-1: PIC16F610/616 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-2: PIC16HV610/616 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-3: PIC16F610/616 FREQUENCY TOLERANCE GRAPH, -40°C ≤ TA ≤ +125°C

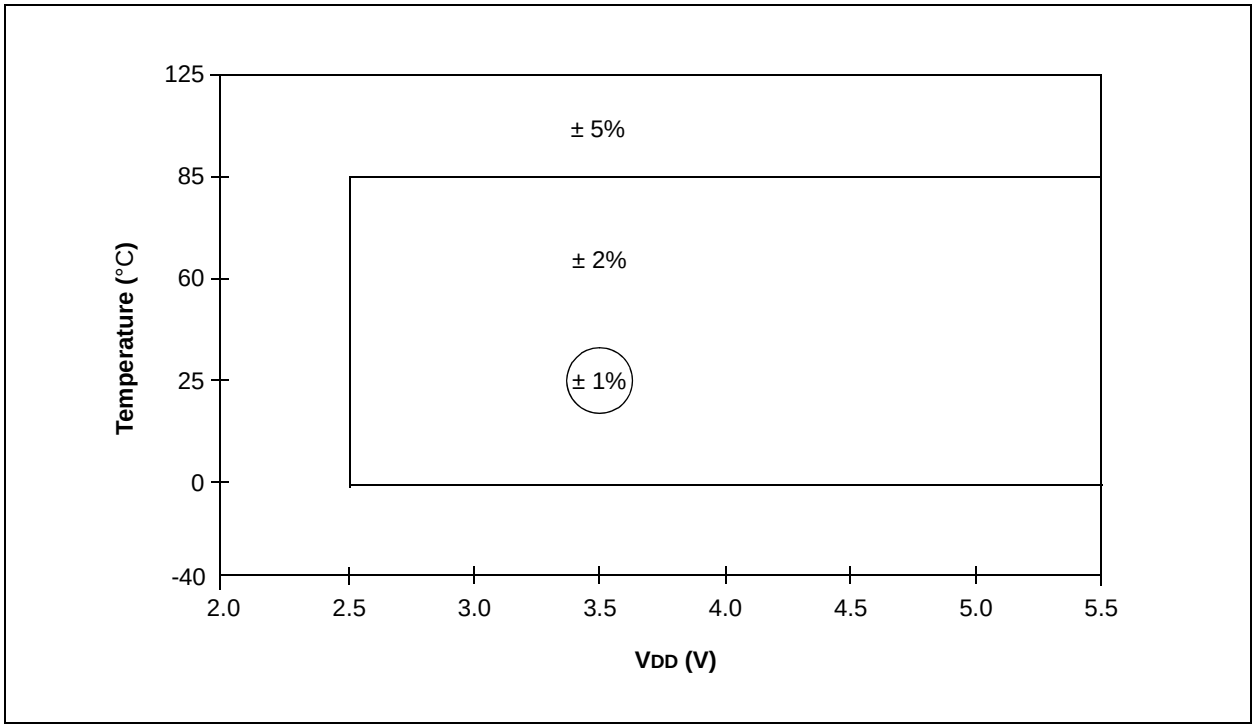
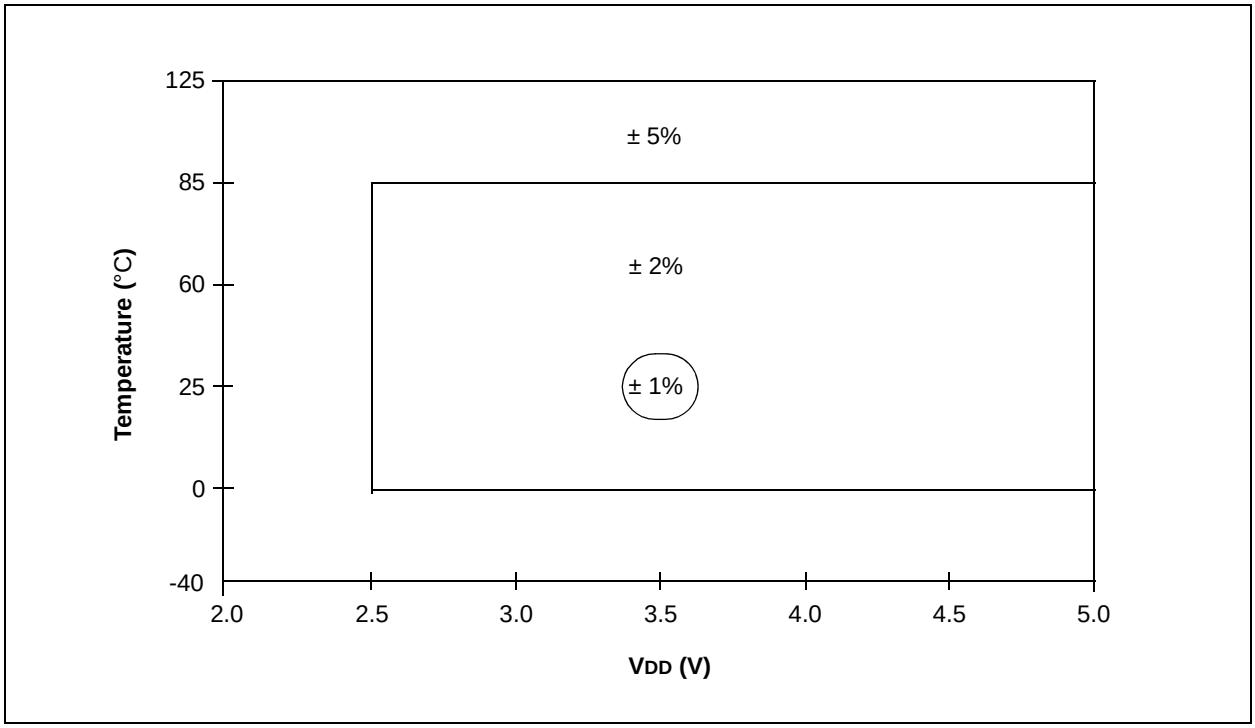


FIGURE 15-4: PIC16HV610/616 FREQUENCY TOLERANCE GRAPH, -40°C ≤ TA ≤ +125°C



15.5 DC Characteristics: PIC16F610/616-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020E	**Power-down Base Current (IPD)(2)** PIC16F610/616	—	0.05	4.0	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	5.0	µA	3.0	
		—	0.35	8.5	µA	5.0	
D021E		—	0.5	5.0	µA	2.0	WDT Current(1)
		—	2.5	8.0	µA	3.0	
		—	9.5	19	µA	5.0	
D022E		—	5.0	15	µA	3.0	BOR Current(1)
		—	6.0	19	µA	5.0	
D023E		—	105	130	µA	2.0	Comparator Current(1), both comparators enabled
		—	110	140	µA	3.0	
		—	116	150	µA	5.0	
D024E		—	50	70	µA	2.0	Comparator Current(1), single comparator enabled
		—	55	75	µA	3.0	
		—	60	80	µA	5.0	
D025E		—	30	40	µA	2.0	CVREF Current(1) (high range)
		—	45	60	µA	3.0	
		—	75	105	µA	5.0	
D026E*		—	39	50	µA	2.0	CVREF Current(1) (low range)
		—	59	80	µA	3.0	
		—	98	130	µA	5.0	
D027E		—	5.5	16	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	7.0	18	µA	3.0	
		—	8.5	22	µA	5.0	
D028E		—	0.2	6.5	µA	3.0	A/D Current(1), no conversion in progress
		—	0.36	10	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

15.6 DC Characteristics: PIC16HV610/616- I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020	**Power-down Base Current(IPD)(2,3)**	—	135	200	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	210	280	µA	3.0	
	PIC16HV610/616	—	260	350	µA	4.5	
D021		—	135	200	µA	2.0	WDT Current(1)
		—	210	285	µA	3.0	
		—	265	360	µA	4.5	
D022		—	215	285	µA	3.0	BOR Current(1)
		—	265	360	µA	4.5	
D023		—	240	340	µA	2.0	Comparator Current(1), both comparators enabled
		—	320	420	µA	3.0	
		—	370	500	µA	4.5	
D024		—	185	270	µA	2.0	Comparator Current(1), single comparator enabled
		—	265	350	µA	3.0	
		—	320	430	µA	4.5	
D025		—	165	235	µA	2.0	CVREF Current(1) (high range)
		—	255	330	µA	3.0	
		—	330	430	µA	4.5	
D026*		—	175	245	µA	2.0	CVREF Current(1) (low range)
		—	275	350	µA	3.0	
		—	355	450	µA	4.5	
D027		—	140	205	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	220	290	µA	3.0	
		—	270	360	µA	4.5	
D028		—	210	280	µA	3.0	A/D Current(1), no conversion in progress
		—	260	350	µA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: Shunt regulator is always enabled and always draws operating current.

TABLE 15-14: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC16F616 – H (High Temp.)

Param No.	Device Characteristics	Units	Min	Typ	Max	Condition	
						VDD	Note
D010	Supply Current (IDD)	μA	—	13	58	2.0	IDD LP OSC (32 kHz)
			—	19	67	3.0	
			—	32	92	5.0	
D011		μA	—	135	316	2.0	IDD XT OSC (1 MHz)
			—	185	400	3.0	
			—	300	537	5.0	
D012		μA	—	240	495	2.0	IDD XT OSC (4 MHz)
			—	360	680	3.0	
		mA	—	0.660	1.20	5.0	
D013		μA	—	75	158	2.0	IDD EC OSC (1 MHz)
			—	155	338	3.0	
			—	345	792	5.0	
D014		μA	—	185	357	2.0	IDD EC OSC (4 MHz)
			—	325	625	3.0	
		mA	—	0.665	1.30	5.0	
D016		μA	—	245	476	2.0	IDD INTOSC (4 MHz)
			—	360	672	3.0	
			—	620	1.10	5.0	
D017		μA	—	395	757	2.0	IDD INTOSC (8 MHz)
		mA	—	0.620	1.20	3.0	
			—	1.20	2.20	5.0	
D018		μA	—	175	332	2.0	IDD EXTRC (4 MHz)
			—	285	518	3.0	
			—	530	972	5.0	
D019		mA	—	2.20	4.10	4.5	IDD HS OSC (20 MHz)
			—	2.80	4.80	5.0	

FIGURE 16-49: 0.6V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

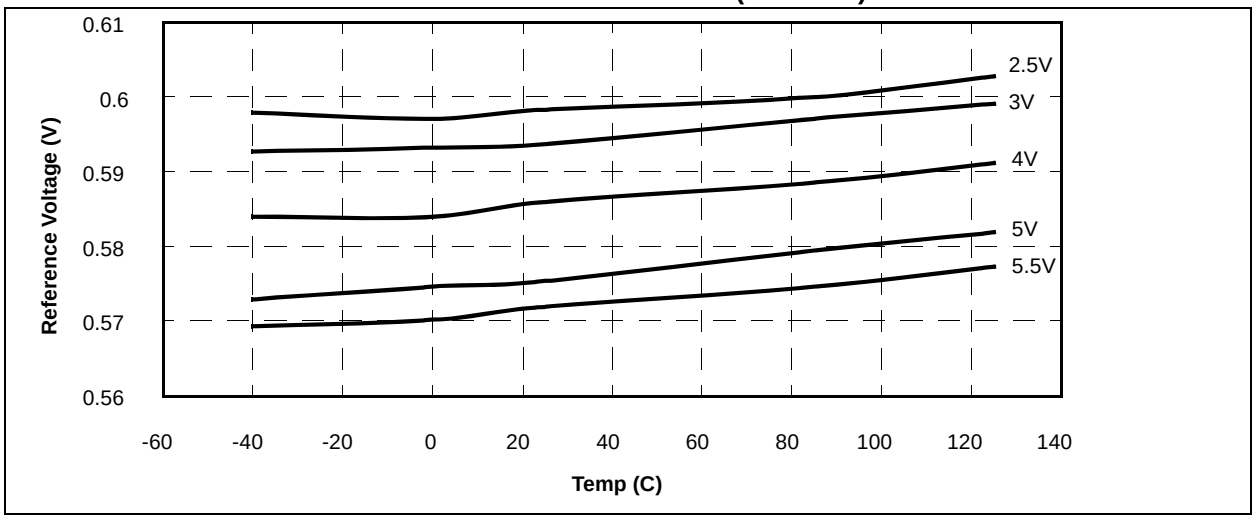


FIGURE 16-50: 1.2V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

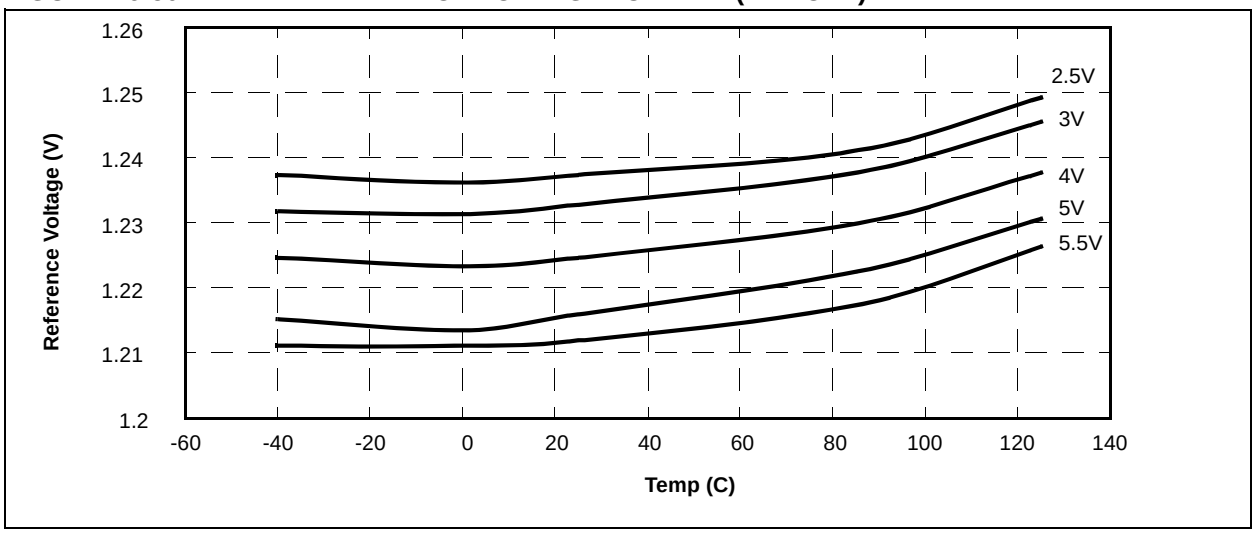
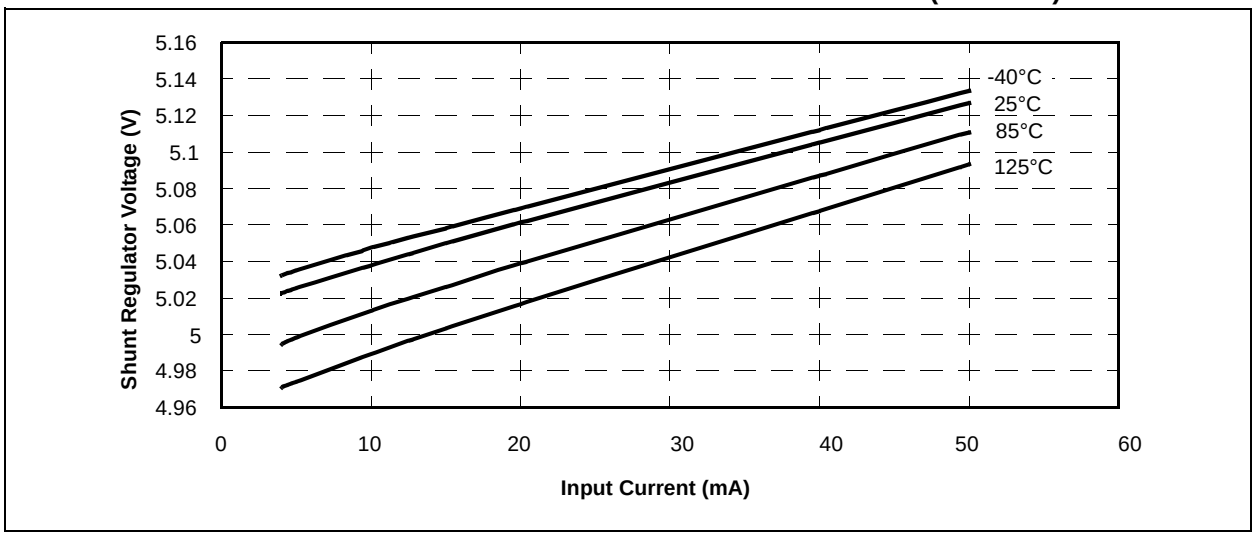
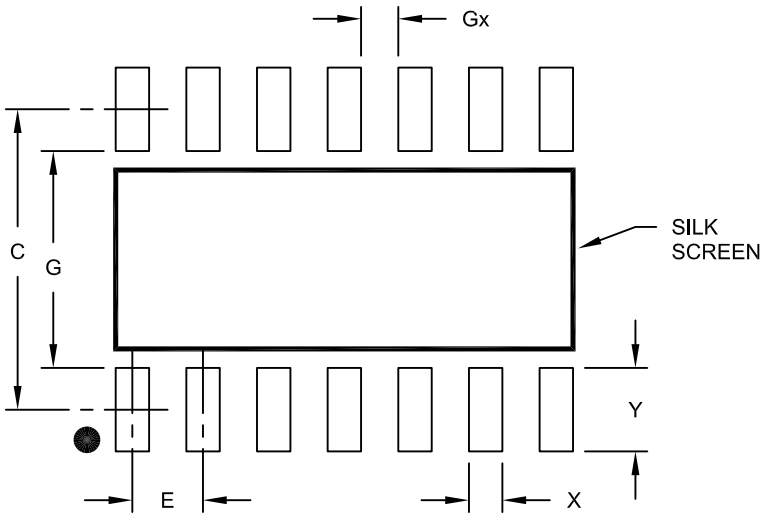


FIGURE 16-51: SHUNT REGULATOR VOLTAGE vs. INPUT CURRENT (TYPICAL)



14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

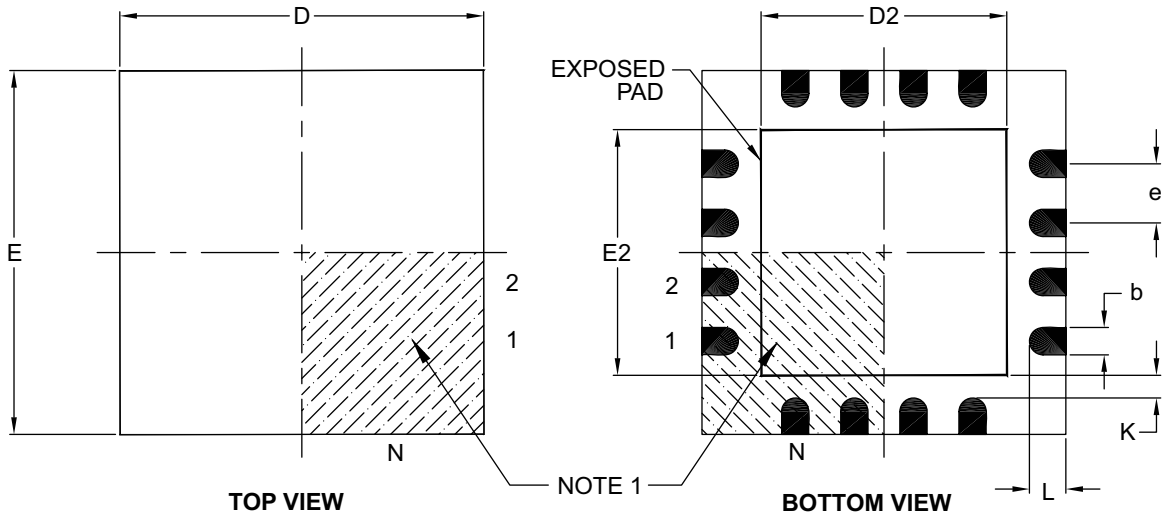
1. Dimensioning and tolerancing per ASME Y14.5M

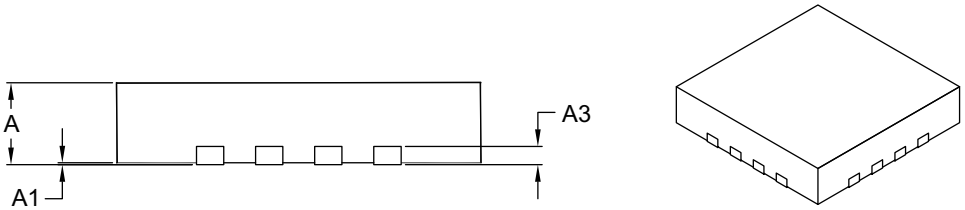
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B