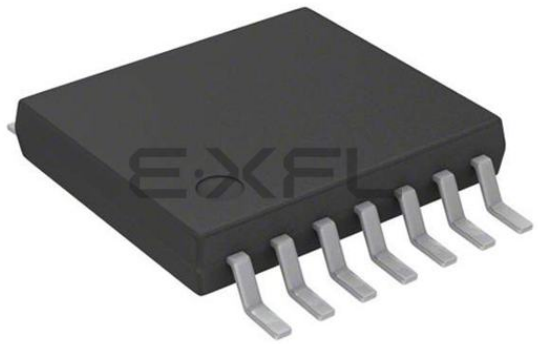

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f616-h-st

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS,` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `'000u u1uu'` (where u = unchanged).

It is recommended, therefore, that only `BCF, BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the **Section 13.0 "Instruction Set Summary"**.

Note 1:	Bits IRP and RP1 of the STATUS register are not used by the PIC16F610/616/16HV610/616 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
2:	The C and DC bits operate as a $\overline{Borrow}$ and Digit $\overline{Borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** This bit is reserved and should be maintained as '0'

bit 6 **RP1:** This bit is reserved and should be maintained as '0'

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)
1 = Bank 1 (80h – FFh)
0 = Bank 0 (00h – 7Fh)

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF, ADDLW, SUBLW, SUBWF` instructions), For $\overline{Borrow}$, the polarity is reversed.
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF, RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

2.2.2.5 PIR1 Register

The PIR1 register contains the peripheral interrupt flag bits, as shown in Register 2-5.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIF:** A/D Interrupt Flag bit(1)
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit(1)
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 4 **C2IF:** Comparator C2 Interrupt Flag bit
1 = Comparator C2 output has changed (must be cleared in software)
0 = Comparator C2 output has not changed

bit 3 **C1IF:** Comparator C1 Interrupt Flag bit
1 = Comparator C1 output has changed (must be cleared in software)
0 = Comparator C1 output has not changed

bit 2 **Unimplemented:** Read as '0'

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit(1)
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed

Note 1: PIC16F616/16HV616 only. PIC16F610/16HV610 unimplemented, read as '0'.

2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-2) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the $\overline{BOR}$.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0(1)
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: Reads as '0' if Brown-out Reset is disabled.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3(1)	ANS2(1)	ANS1	ANS0	1111 1111	1111 1111
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0	0000 -000	0000 -000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	0000 -000	0000 -000
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--u0 u000
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
WPUA	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	--11 -111

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: For PIC16F616/HV616 only.

4.3 PORTC and the TRISC Registers

PORTC is a general purpose I/O port consisting of 6 bidirectional pins. The pins can be configured for either digital I/O or analog input to A/D Converter (ADC) or Comparator. For specific information about individual functions such as the Enhanced CCP or the ADC, refer to the appropriate section in this data sheet.

Note:	The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

EXAMPLE 4-2: INITIALIZING PORTC

```
BCF     STATUS,RP0      ;Bank 0
CLRF    PORTC           ;Init PORTC
BSF     STATUS,RP0      ;Bank 1
CLRF    ANSEL           ;digital I/O
MOVLW   0Ch             ;Set RC<3:2> as inputs
MOVWF   TRISC           ;and set RC<5:4,1:0>
                        ;as outputs
BCF     STATUS,RP0      ;Bank 0
```

REGISTER 4-6: PORTC: PORTC REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-0	R/W-0	R/W-x	R/W-x
—	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **RC<5:0>**: PORTC I/O Pin bit
1 = PORTC pin is > V_{IH}
0 = PORTC pin is < V_{IL}

REGISTER 4-7: TRISC: PORTC TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **TRISC<5:0>:** PORTC Tri-State Control bit
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

Note:	TMR1GE bit of the T1CON register must be set to use either T1G or C2OUT as the Timer1 gate source. See the CM2CON1 register (Register 8-3) for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the T1G pin or Comparator C2 output. This configures Timer1 to measure either the active-high or active-low time between events.

6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register
- T1SYNC bit of the T1CON register
- TMR1CS bit of the T1CON register
- T1OSCEN bit of the T1CON register (can be set)

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

6.9 ECCP Capture/Compare Time Base (PIC16F616/16HV616 Only)

The ECCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see **Section 10.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC16F616/16HV616 Only)"**.

6.10 ECCP Special Event Trigger (PIC16F616/16HV616 Only)

When the ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see **Section 10.2.4 "Special Event Trigger"**.

6.11 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 8.8.2 "Synchronizing Comparator C2 Output to Timer1"**.

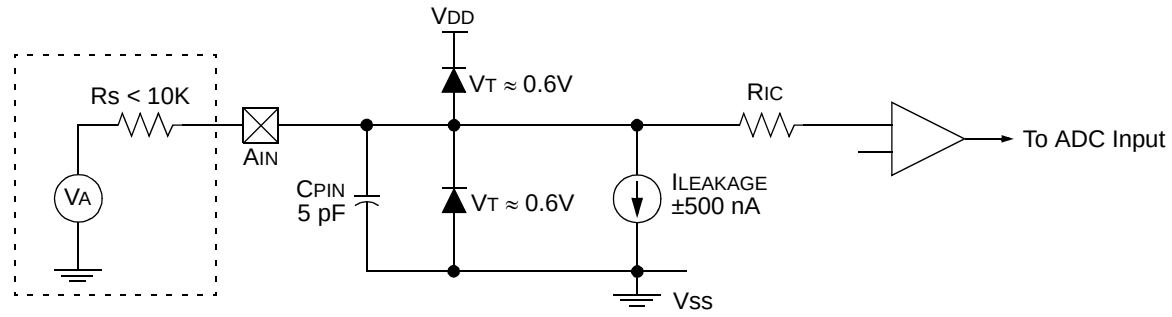
8.7 Comparator Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 8-6. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

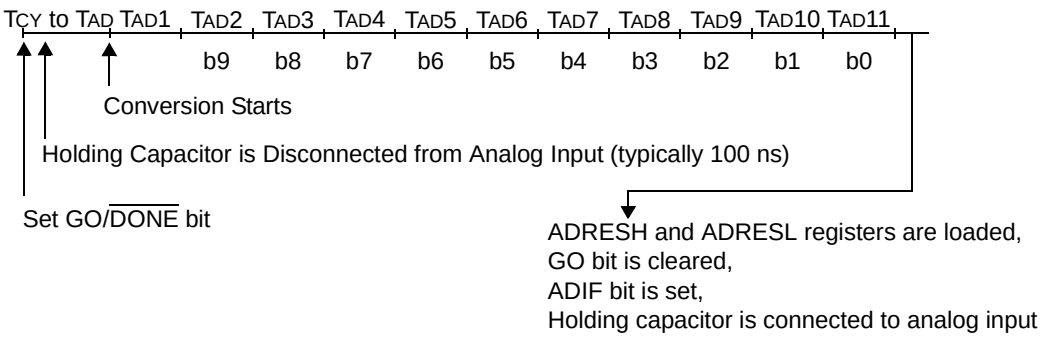
Note 1:	When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.
2:	Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 8-6: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



9.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an analog-to-digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note:	The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the interrupt service routine.

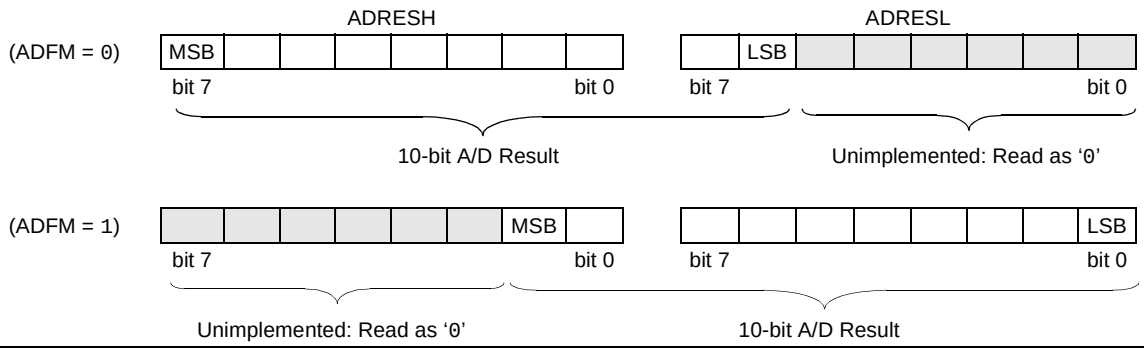
Please see **Section 9.1.5 "Interrupts"** for more information.

9.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 9-4 shows the two output formats.

FIGURE 9-3: 10-BIT A/D CONVERSION RESULT FORMAT



REGISTER 9-3: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES9	ADRES8	ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 9-4: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

bit 5-0 **Reserved**: Do not use.

REGISTER 9-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Reserved**: Do not use.

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper 2 bits of 10-bit conversion result

REGISTER 9-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower 8 bits of 10-bit conversion result

10.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to make the CCP1 pin an output.

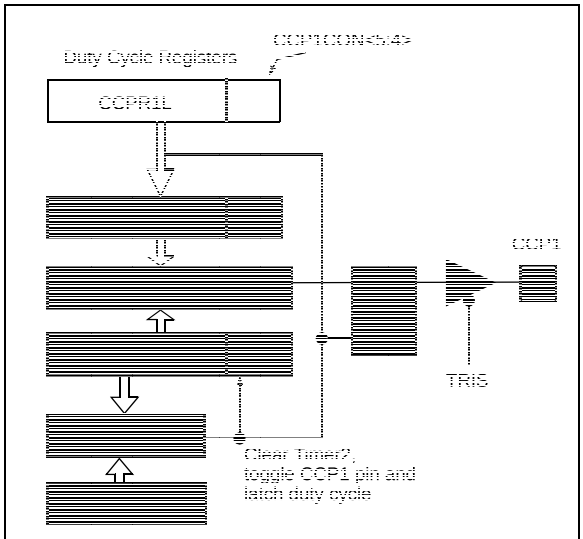
Note:	Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

Figure 10-3 shows a simplified block diagram of PWM operation.

Figure 10-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 10.3.7 "Setup for PWM Operation"**.

FIGURE 10-3: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (F_{OSC}), or 2 bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPR1H is a read only register.

The PWM output (Figure 10-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 10-4: CCP PWM OUTPUT

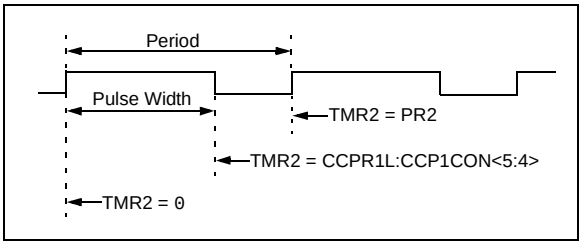
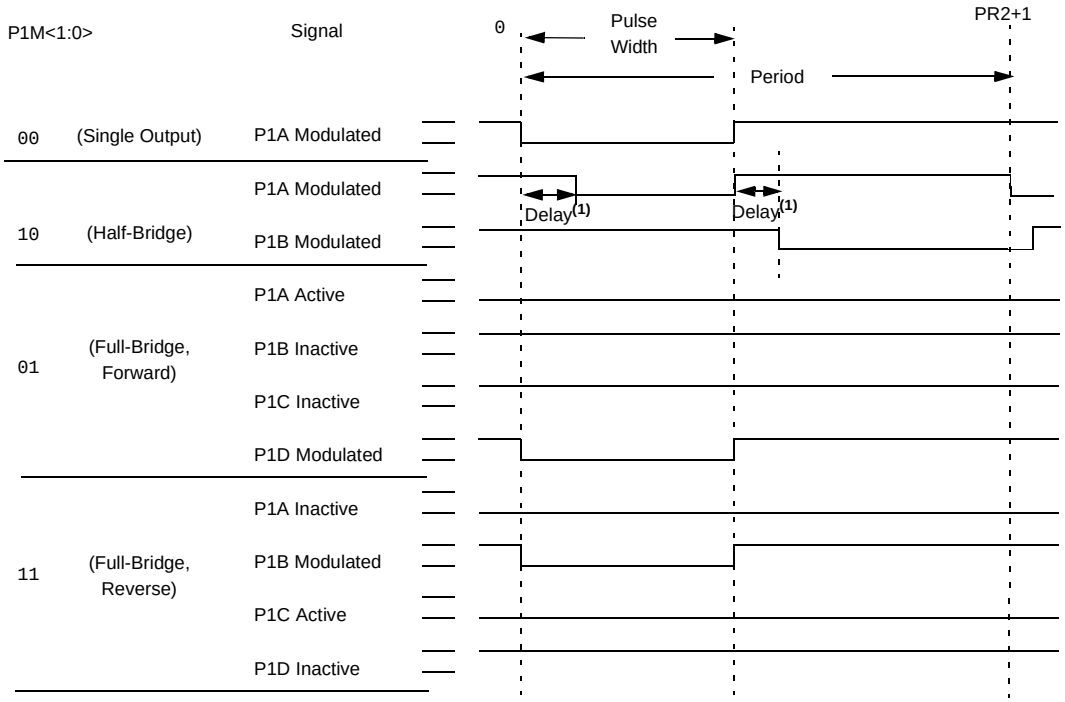


FIGURE 10-7: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)



Relationships:

- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (PWM1CON<6:0>)

Note 1: Dead-band delay is programmed using the PWM1CON register (**Section 10.4.6 "Programmable Dead-Band Delay mode"**).

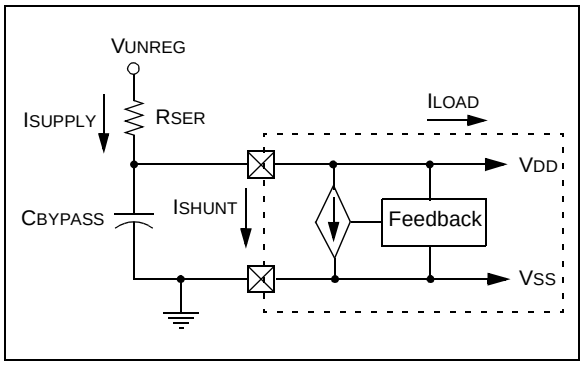
11.0 VOLTAGE REGULATOR

The PIC16HV610/16HV616 include a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (ILOAD).

11.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor RSER. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage VUNREG and the VDD of the microcontroller. See Figure 11-1 for voltage regulator schematic.

FIGURE 11-1: VOLTAGE REGULATOR



An external current limiting resistor, RSER, located between the unregulated supply, VUNREG, and the VDD pin, drops the difference in voltage between VUNREG and VDD. RSER must be between RMAX and RMIN as defined by Equation 11-1.

EQUATION 11-1: RSER LIMITING RESISTOR

$$R_{MAX} = \frac{(VU_{MIN} - 5V)}{1.05 \bullet (4\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(VU_{MAX} - 5V)}{0.95 \bullet (50\ mA)}$$

Where:

RMAX = maximum value of RSER (ohms)

RMIN = minimum value of RSER (ohms)

VUMIN = minimum value of VUNREG

VUMAX = maximum value of VUNREG

VDD = regulated voltage (5V nominal)

ILOAD = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of RSER

0.95 = compensation for -5% tolerance of RSER

11.2 Regulator Considerations

The supply voltage VUNREG and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for RSER must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC16HV610/16HV616 devices.

TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Reset(1)	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--x0 x000	--u0 u000	--uu uuuu
PORTC	07h	--xx xx00	--uu 00uu	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu(2)
PIR1	0Ch	-000 0-00	-000 0-00	-uuu u-uu(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
TMR2(6)	11h	0000 0000	0000 0000	uuuu uuuu
T2CON(6)	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L(6)	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H(6)	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON(6)	15h	0000 0000	0000 0000	uuuu uuuu
PWM1CON(6)	16h	0000 0000	0000 0000	uuuu uuuu
ECCPAS(6)	17h	0000 0000	0000 0000	uuuu uuuu
VRCON	19h	0000 0000	0000 0000	uuuu uuuu
CM1CON0	1Ah	0000 -000	0000 -000	uuuu -uuu
CM2CON0	1Bh	0000 -000	0000 -000	uuuu -uuu
CM2CON1	1Ch	00-0 0000	00-0 0000	uu-u uuuu
ADRESH(6)	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0(6)	1Fh	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISC	87h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	-000 0-00	-000 0-00	-uuu u-uu
PCON	8Eh	---- --0x	---- --uu(1, 5)	---- --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F616/16HV616 only.

7: ANSEL <3:2> For PIC16F616/HV616 only.

15.3 DC Characteristics: PIC16HV610/616-I (Industrial) PIC16HV610/616-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	**Supply Current (IDD)(1, 2)** PIC16HV610/616	—	160	230	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	240	310	µA	3.0	
		—	280	400	µA	4.5	
D011*		—	270	380	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	400	560	µA	3.0	
		—	520	780	µA	4.5	
D012		—	380	540	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	575	810	µA	3.0	
		—	0.875	1.3	mA	4.5	
D013*		—	215	310	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	375	565	µA	3.0	
		—	570	870	µA	4.5	
D014		—	330	475	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	550	800	µA	3.0	
		—	0.85	1.2	mA	4.5	
D016*		—	310	435	µA	2.0	FOSC = 4 MHz INTOSC mode
		—	500	700	µA	3.0	
		—	0.74	1.1	mA	4.5	
D017		—	460	650	µA	2.0	FOSC = 8 MHz INTOSC mode
		—	0.75	1.1	mA	3.0	
		—	1.2	1.6	mA	4.5	
D018		—	320	465	µA	2.0	FOSC = 4 MHz EXTRC mode(3)
		—	510	750	µA	3.0	
		—	0.770	1.0	mA	4.5	
D019		—	2.5	3.4	mA	4.5	FOSC = 20 MHz HS Oscillator mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

15.13 High Temperature Operation

This section outlines the specifications for the PIC16F616 device operating in a temperature range between -40°C and 150°C.(4) The specifications between -40°C and 150°C(4) are identical to those shown in DS41302 and DS80329.

Note 1: Writes are **not allowed** for Flash Program Memory above 125°C.

2: All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.

3: The temperature range indicator in the part number is "H" for -40°C to 150°C.(4)

Example: PIC16F616T-H/ST indicates the device is shipped in a tAPE and reel configuration, in the TSSOP package, and is rated for operation from -40°C to 150°C.(4)

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

TABLE 15-13: ABSOLUTE MAXIMUM RATINGS

Parameter	Source/Sink	Value	Units
Max. Current: VDD	Source	20	mA
Max. Current: VSS	Sink	50	mA
Max. Current: PIN	Source	5	mA
Max. Current: PIN	Sink	10	mA
Pin Current: at VOH	Source	3	mA
Pin Current: at VOL	Sink	8.5	mA
Port Current: A and C	Source	20	mA
Port Current: A and C	Sink	50	mA
Maximum Junction Temperature		155	°C

Note: Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

FIGURE 16-18: PIC16F616 IPD A/D vs. VDD

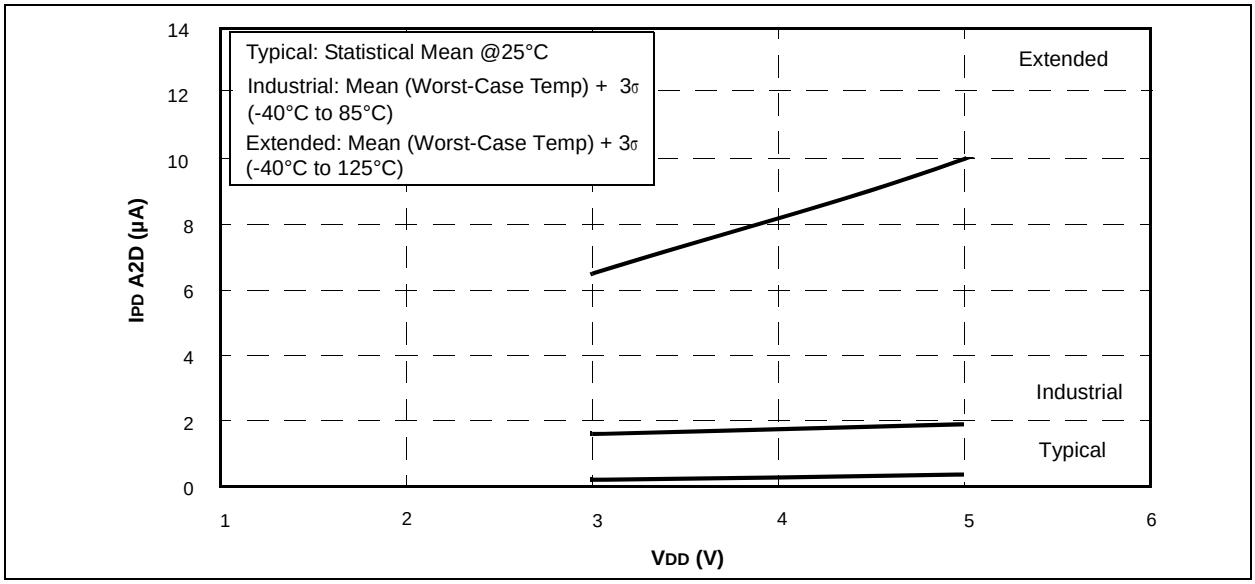


FIGURE 16-19: PIC16HV610/616 IDD LP (32 kHz) vs. VDD

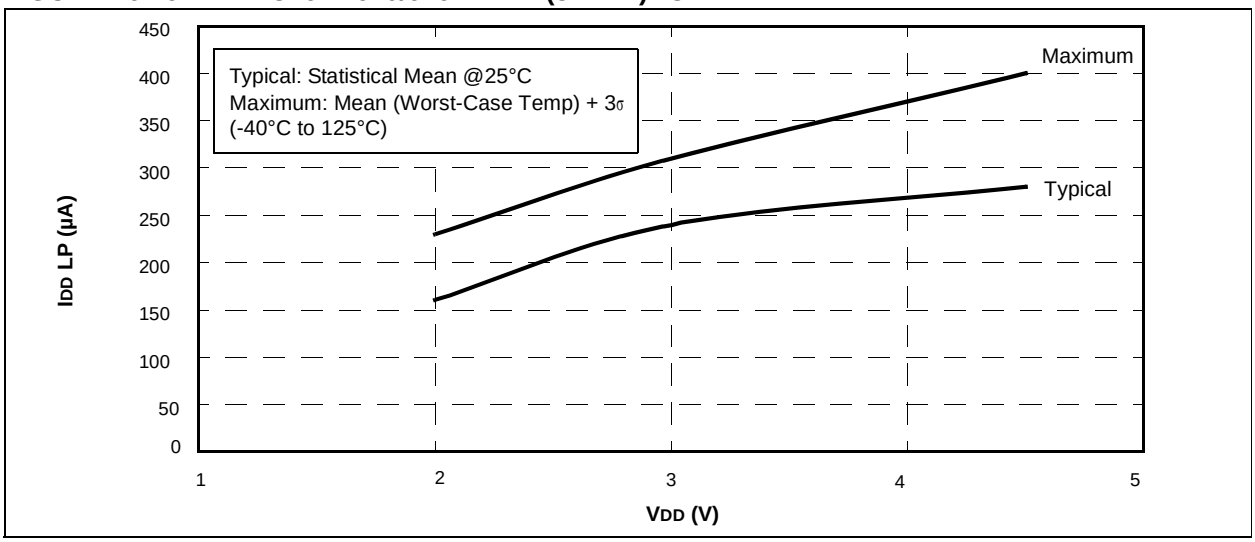


FIGURE 16-23: PIC16HV610/616 IDD XT (4 MHz) vs. VDD

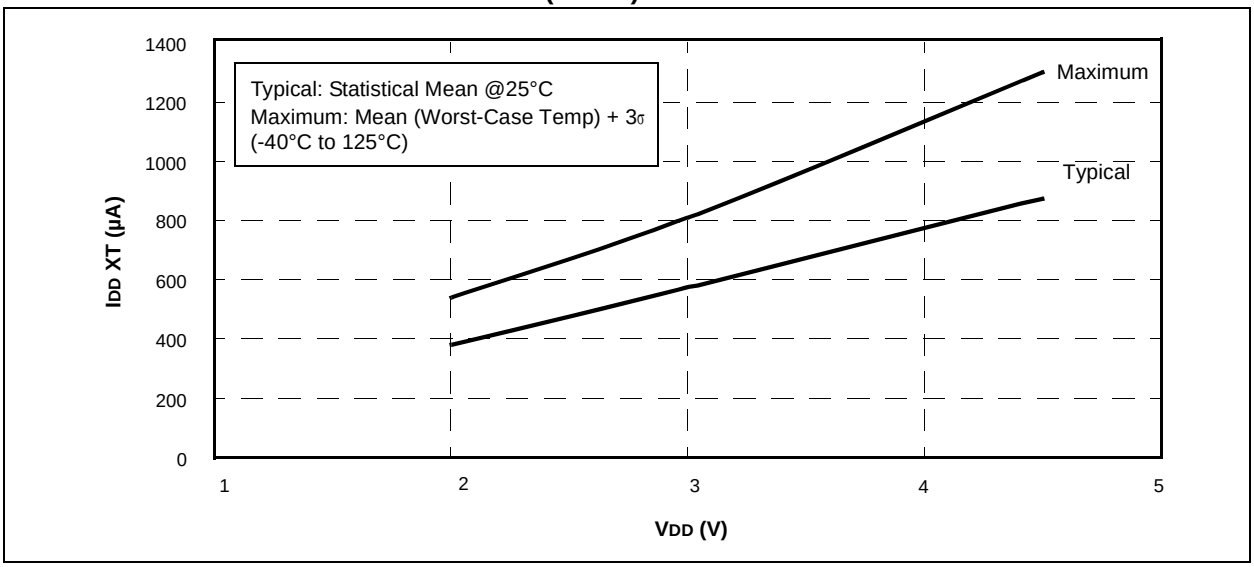


FIGURE 16-24: PIC16HV610/616 IDD INTOSC (4 MHz) vs. VDD

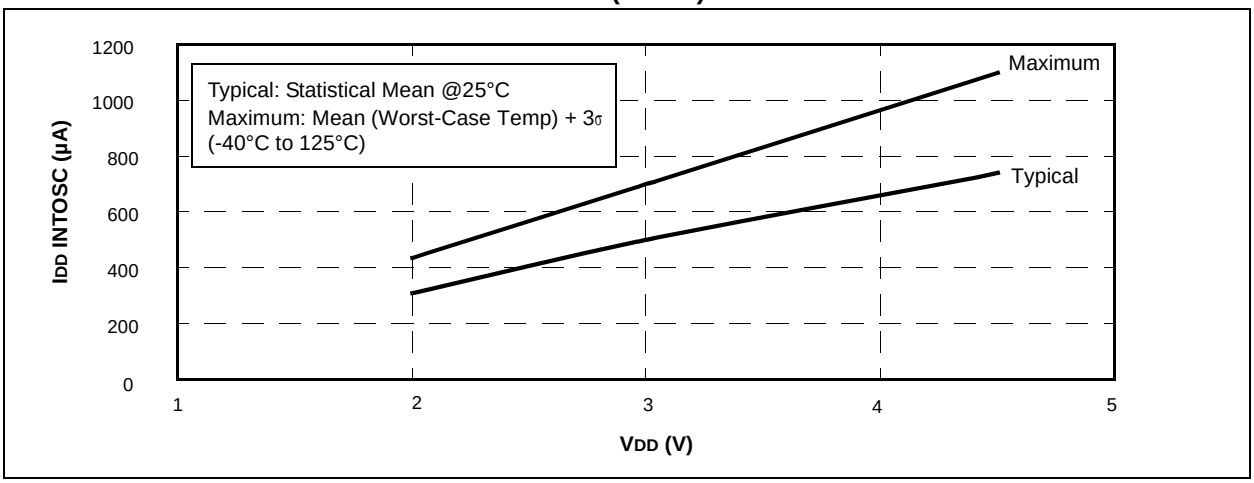


FIGURE 16-25: PIC16HV610/616 IDD INTOSC (8 MHz) vs. VDD

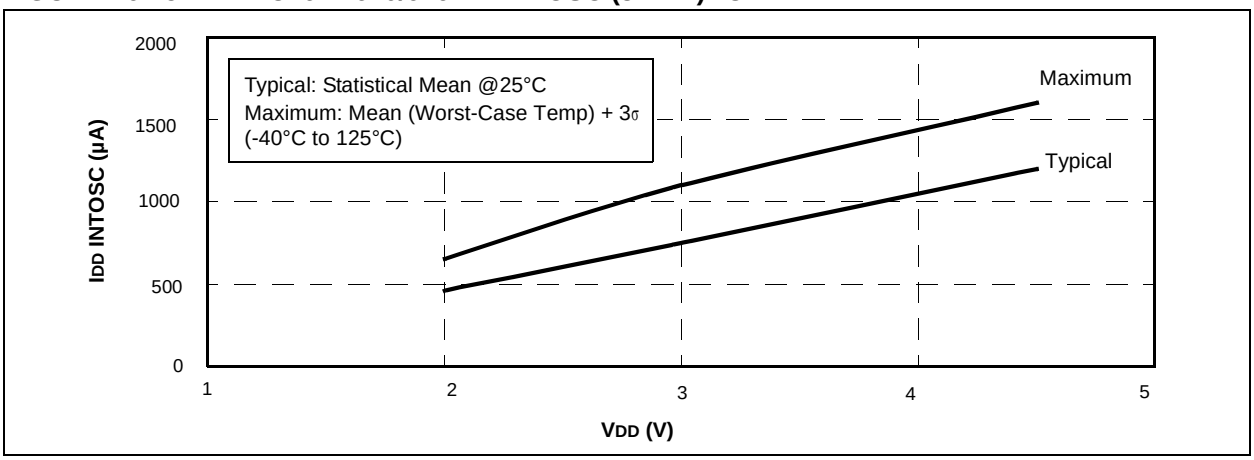


FIGURE 16-29: PIC16HV610/616 IPD COMPARATOR (BOTH ON) vs. VDD

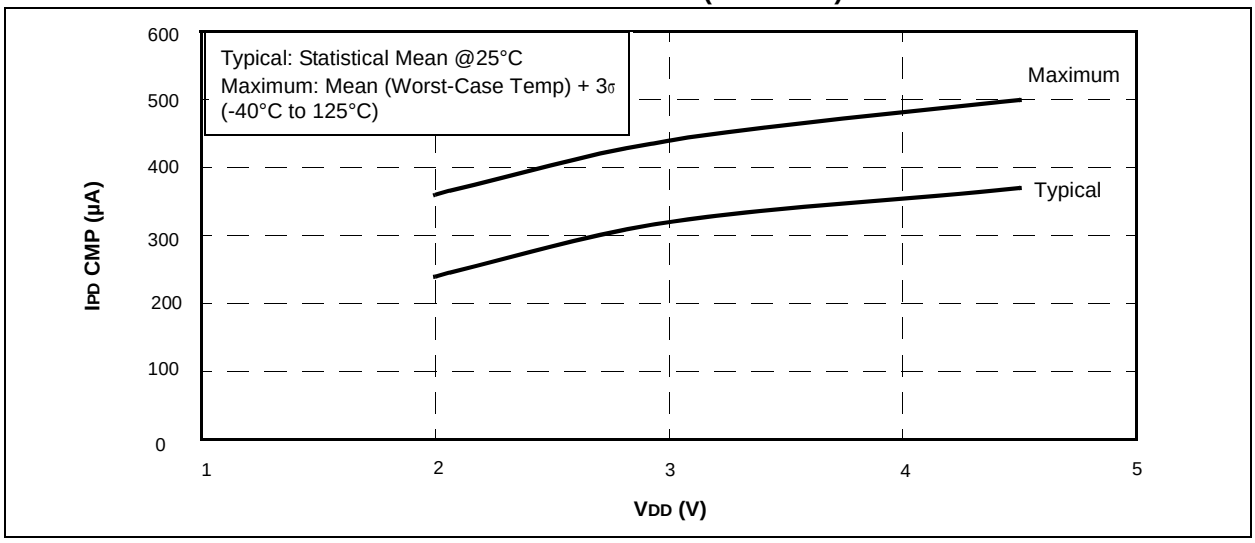


FIGURE 16-30: PIC16HV610/616 IPD WDT vs. VDD

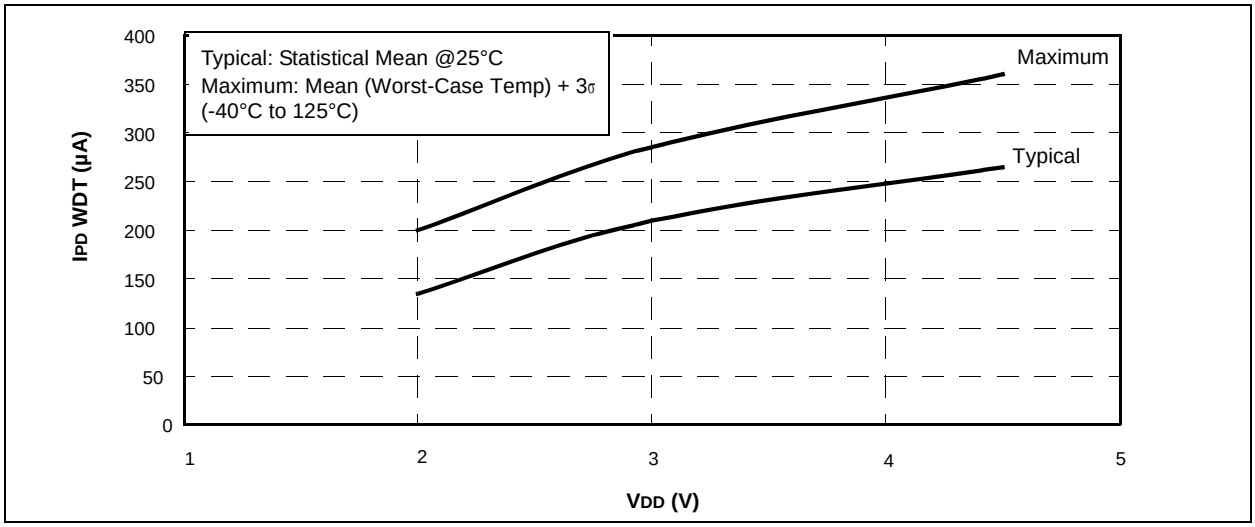
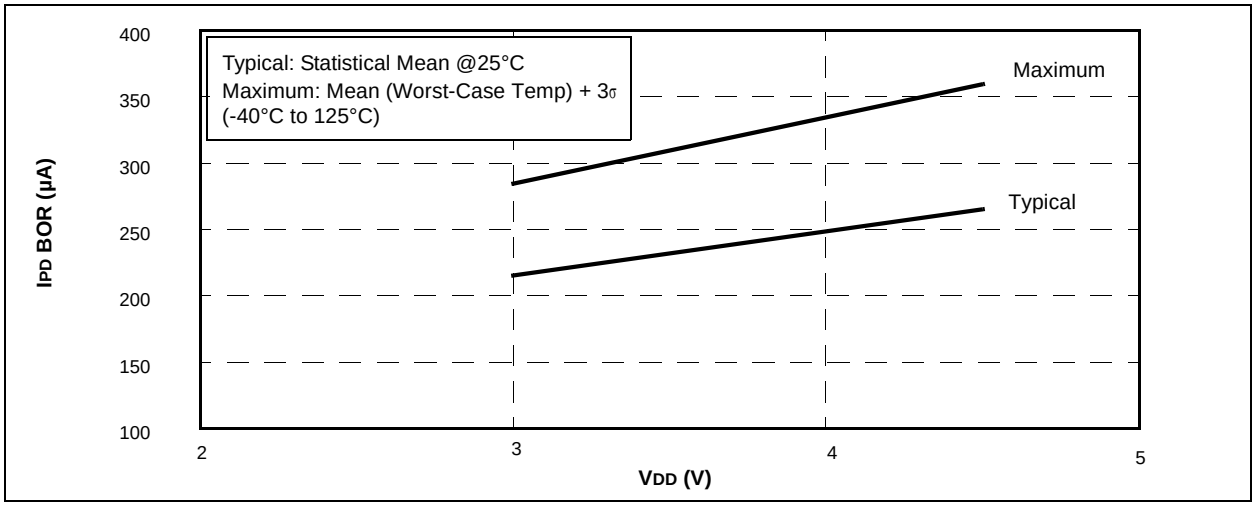


FIGURE 16-31: PIC16HV610/616 IPD BOR vs. VDD

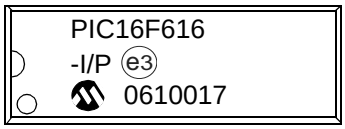


17.0 PACKAGING INFORMATION

17.1 Package Marking Information

14-Lead PDIP

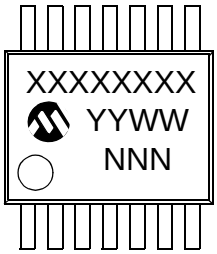
Example



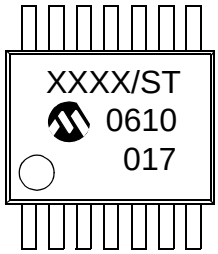
14-Lead SOIC (.150”)

Example

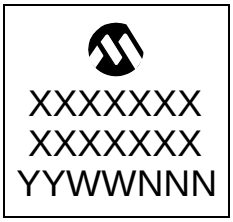
14-Lead TSSOP



Example



16-Lead QFN



Example

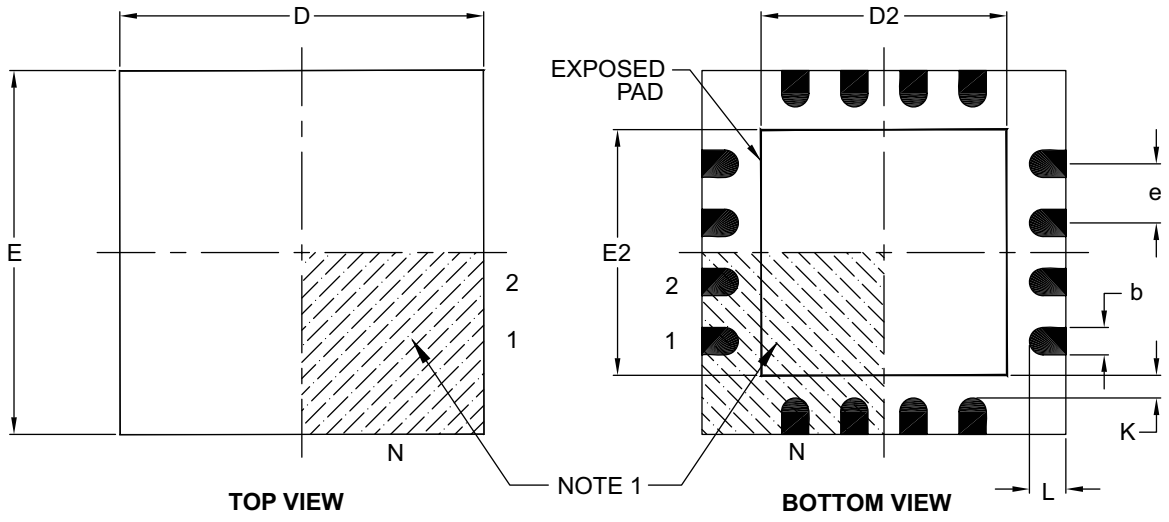
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

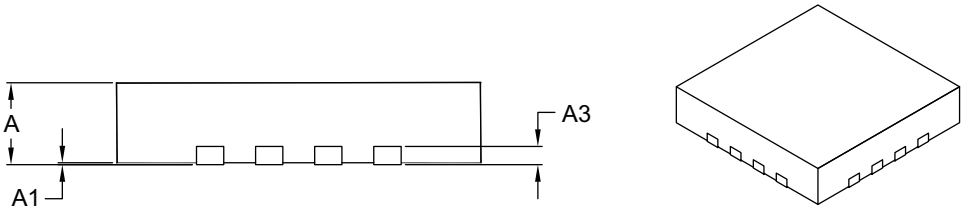
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC® device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B