Microchip Technology - PIC16F616T-I/SL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f616t-i-sl

TABLE 1-1: PIC16F610/16HV610 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/C1IN+/ICSPDAT	RA0	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	C1IN+	AN	—	Comparator C1 non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
RA1/C12IN0-/ICSPCLK	RA1	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	C12IN0-	AN	—	Comparators C1 and C2 inverting input
	ICSPCLK	ST	—	Serial Programming Clock
RA2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator C1 output
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	PORTA input with interrupt-on-change
	$\overline{\text{MCLR}}$	ST	—	Master Clear w/internal pull-up
	VPP	HV	—	Programming voltage
RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	$\overline{\text{T1G}}$	ST	—	Timer1 gate (count enable)
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock input
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RC0/C2IN+	RC0	TTL	CMOS	PORTC I/O
	C2IN+	AN	—	Comparator C2 non-inverting input
RC1/C12IN1-	RC1	TTL	CMOS	PORTC I/O
	C12IN1-	AN	—	Comparators C1 and C2 inverting input
RC2/C12IN2-	RC2	TTL	CMOS	PORTC I/O
	C12IN2-	AN	—	Comparators C1 and C2 inverting input
RC3/C12IN3-	RC3	TTL	CMOS	PORTC I/O
	C12IN3-	AN	—	Comparators C1 and C2 inverting input
RC4/C2OUT	RC4	TTL	CMOS	PORTC I/O
	C2OUT	—	CMOS	Comparator C2 output
RC5	RC5	TTL	CMOS	PORTC I/O
VDD	VDD	Power	—	Positive supply
VSS	VSS	Power	—	Ground reference

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; HV = High Voltage; ST = Schmitt Trigger input with CMOS levels; TTL = TTL compatible input; XTAL = Crystal

3.2 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two selectable clock frequencies: 4 MHz and 8 MHz

The system clock can be selected between external or internal clock sources via the FOSC<2:0> bits of the Configuration Word register.

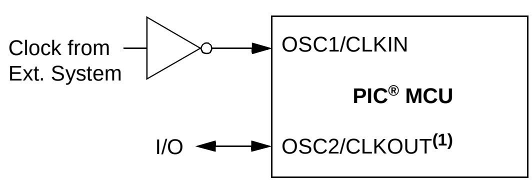
3.3 External Clock Modes

3.3.1 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 3-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Alternate pin functions are listed in the **Section 1.0 "Device Overview"**.

3.3.2 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

TABLE 3-1: OSCILLATOR DELAY EXAMPLES

Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	INTOSC	4 MHz to 8 MHz	Oscillator Warm-Up Delay (T_{WARM})
Sleep/POR	EC, RC	DC – 20 MHz	2 Instruction Cycles
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)

4.3 PORTC and the TRISC Registers

PORTC is a general purpose I/O port consisting of 6 bidirectional pins. The pins can be configured for either digital I/O or analog input to A/D Converter (ADC) or Comparator. For specific information about individual functions such as the Enhanced CCP or the ADC, refer to the appropriate section in this data sheet.

Note:	The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’ and cannot generate an interrupt.

EXAMPLE 4-2: INITIALIZING PORTC

```
BCF     STATUS,RP0    ;Bank 0
CLRF    PORTC         ;Init PORTC
BSF     STATUS,RP0    ;Bank 1
CLRF    ANSEL         ;digital I/O
MOVLW   0Ch           ;Set RC<3:2> as inputs
MOVWF   TRISC         ;and set RC<5:4,1:0>
                      ;as outputs
BCF     STATUS,RP0    ;Bank 0
```

REGISTER 4-6: PORTC: PORTC REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-0	R/W-0	R/W-x	R/W-x
—	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **RC<5:0>**: PORTC I/O Pin bit
1 = PORTC pin is > V_{IH}
0 = PORTC pin is < V_{IL}

REGISTER 4-7: TRISC: PORTC TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **TRISC<5:0>:** PORTC Tri-State Control bit
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

NOTES:

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or T1G pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with ECCP)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

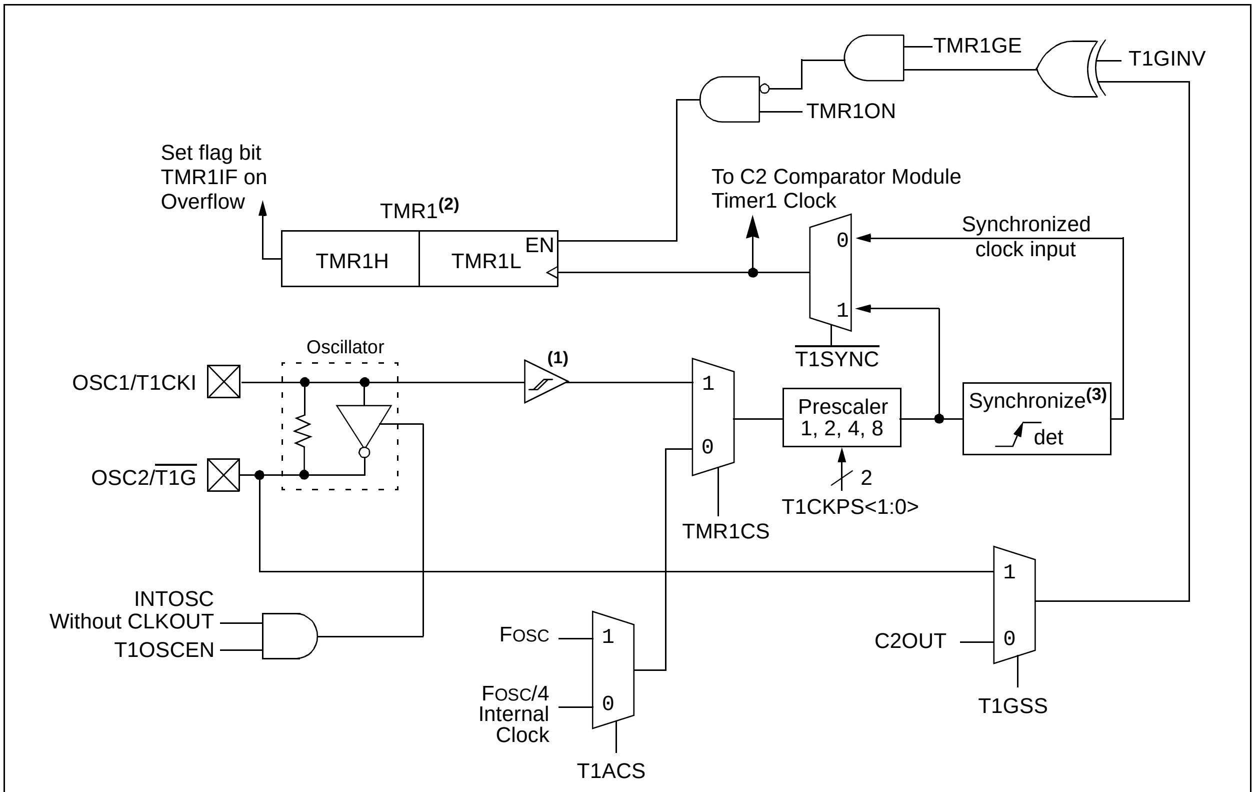
When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is FOSC/4. When TMR1CS = 1, the clock source is supplied externally.

Clock Source	TMR1CS	T1ACS
FOSC/4	0	0
FOSC	0	1
T1CKI pin	1	x

FIGURE 6-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is low power type when using LP osc, or high speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.

8.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the device. The Analog Comparator module includes the following features:

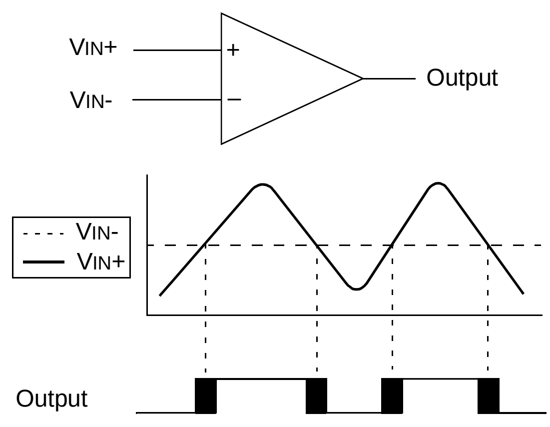
- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- PWM shutdown
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- SR Latch
- Programmable and fixed voltage reference
- User-enable Comparator Hysteresis

Note:	Only Comparator C2 can be linked to Timer1.

8.1 Comparator Overview

A single comparator is shown in Figure 8-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 8-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

8.4 Comparator Interrupt Operation

The comparator interrupt flag can be set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 8-2 and Figure 8-3). One latch is updated with the comparator output level when the CMxCON0 register is read. This latch retains the value until the next read of the CMxCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. At this point the two mismatch latches have opposite output levels which is detected by the exclusive-or gate and fed to the interrupt circuitry. The mismatch condition persists until either the CMxCON0 register is read or the comparator output returns to the previous state.

Note 1:	A write operation to the CMxCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.
2:	Comparator interrupts will operate correctly regardless of the state of CxOE.

The comparator interrupt is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMxCON0 register to clear the mismatch registers. When the mismatch registers are cleared, an interrupt will occur upon the comparator's return to the previous state, otherwise no interrupt will be generated.

Software will need to maintain information about the status of the comparator output, as read from the CMxCON0 register, or CM2CON1 register, to determine the actual change that has occurred.

The CxIF bit of the PIR1 register is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, an interrupt can be generated.

The CxIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR1 register will still be set if an interrupt condition occurs.

FIGURE 8-4: COMPARATOR INTERRUPT TIMING W/O CMxCON0 READ

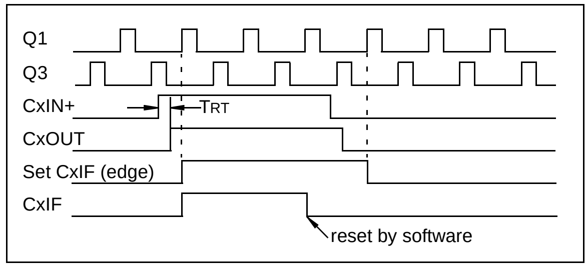
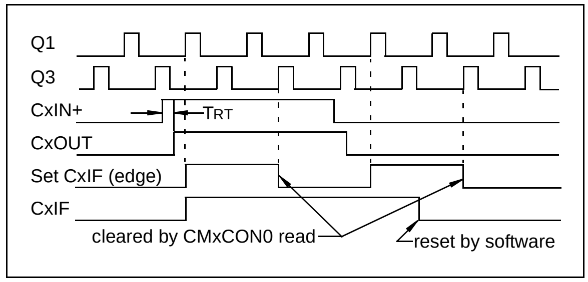


FIGURE 8-5: COMPARATOR INTERRUPT TIMING WITH CMxCON0 READ



Note 1:	If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF of the PIR1 register interrupt flag may not get set.
2:	When either comparator is first enabled, bias circuitry in the comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

9.1 ADC Configuration

When configuring and using the ADC, the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

9.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding Port section for more information.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 9.2 "ADC Operation"** for more information.

9.1.3 ADC VOLTAGE REFERENCE

The VCFG bit of the ADCON0 register provides control of the positive voltage reference. The positive voltage reference can be either VDD or an external voltage source. The negative voltage reference is always connected to the ground reference.

9.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 9-3.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in **Section 15.0 "Electrical Specifications"** for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note:	Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

TABLE 9-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES (VDD ≥ 3.0V)

ADC Clock Period (TAD)		Device Frequency (FOSC)			
ADC Clock Source	**ADCS<2:0>**	**20 MHz**	**8 MHz**	**4 MHz**	**1 MHz**
FOSC/2	000	100 ns(2)	250 ns(2)	500 ns(2)	2.0 μs
FOSC/4	100	200 ns(2)	500 ns(2)	1.0 μs(2)	4.0 μs
FOSC/8	001	400 ns(2)	1.0 μs(2)	2.0 μs	8.0 μs(3)
FOSC/16	101	800 ns(2)	2.0 μs	4.0 μs	16.0 μs(3)
FOSC/32	010	1.6 μs	4.0 μs	8.0 μs(3)	32.0 μs(3)
FOSC/64	110	3.2 μs	8.0 μs(3)	16.0 μs(3)	64.0 μs(3)
FRC	x11	2-6 μs(1,4)	2-6 μs(1,4)	2-6 μs(1,4)	2-6 μs(1,4)

Legend: Shaded cells are outside of recommended range.

Note 1: The FRC source has a typical TAD time of 4 μs for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

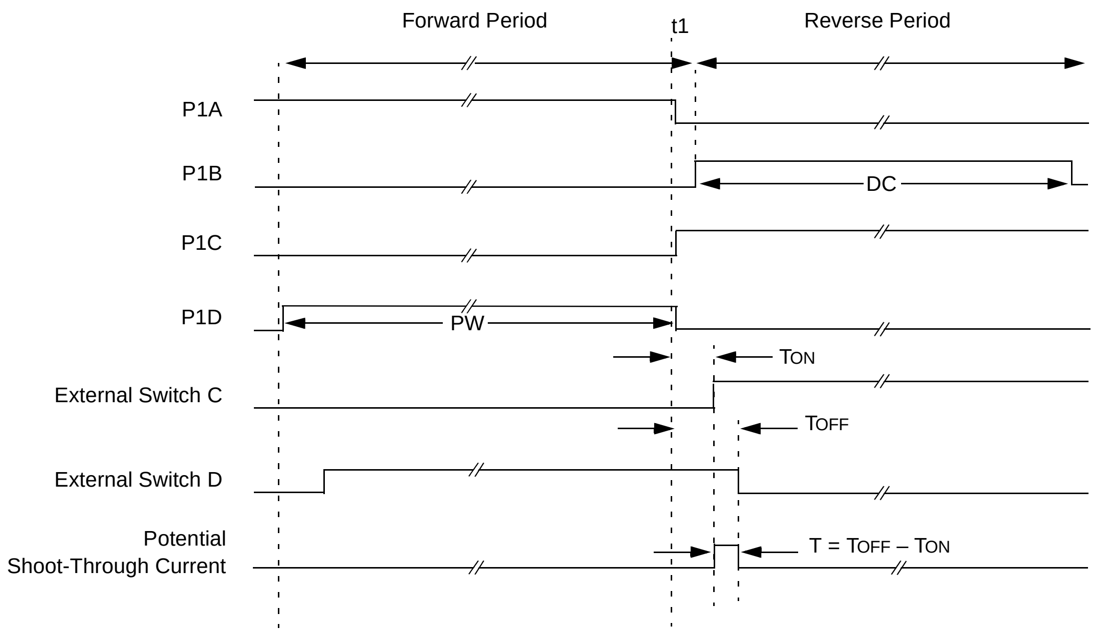
4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

TABLE 10-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON(1)	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
CCPR1L(1)	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
CCPR1H(1)	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	C2IE	C1IE	—	TMR2IE(1)	TMR1IE	-000 0-00	0000 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF	-000 0-00	0000 0-00
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.
Note 1: PIC16F616/16HV616 only.

FIGURE 10-13: EXAMPLE OF PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE



Note 1: All signals are shown as active-high.

2: TON is the turn on delay of power switch QC and its driver.

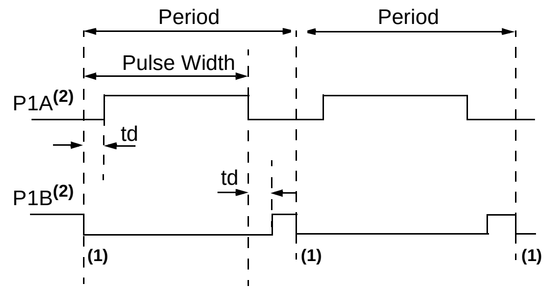
3: TOFF is the turn off delay of power switch QD and its driver.

10.4.6 PROGRAMMABLE DEAD-BAND DELAY MODE

In half-bridge applications where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (*shoot-through current*) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 10-16 for illustration. The lower seven bits of the associated PWM1CON register (Register 10-3) sets the delay period in terms of microcontroller instruction cycles (TCY or 4 TOSC).

FIGURE 10-16: EXAMPLE OF HALF-BRIDGE PWM OUTPUT



td = Dead-Band Delay

Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: Output signals are shown as active-high.

FIGURE 10-17: EXAMPLE OF HALF-BRIDGE APPLICATIONS

Standard Half-Bridge Circuit (“Push-Pull”)

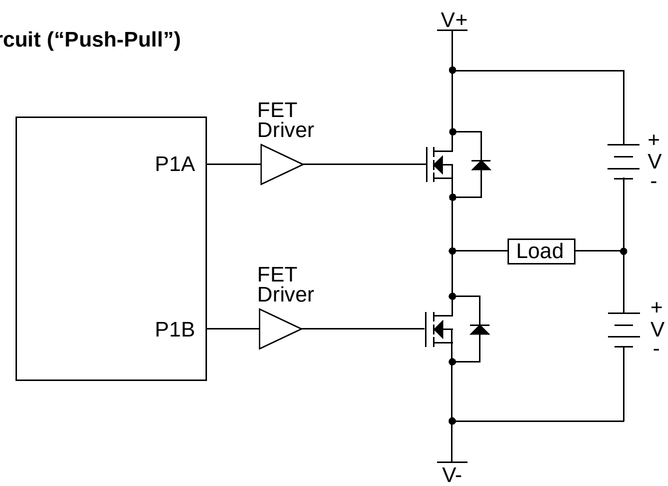


TABLE 13-2: PIC16F610/616/16HV610/616 INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	**1, 2**
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	**1, 2**
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	**2**
CLRW	–	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	**1, 2**
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	**1, 2**
DECFSZ	f, d	Decrement f, Skip if 0	1**(2)**	00	1011	dfff	ffff		**1, 2, 3**
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	**1, 2**
INCFSZ	f, d	Increment f, Skip if 0	1**(2)**	00	1111	dfff	ffff		**1, 2, 3**
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	**1, 2**
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	**1, 2**
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	–	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	**1, 2**
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	**1, 2**
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	**1, 2**
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		**1, 2**
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	**1, 2**
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		**1, 2**
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		**1, 2**
BTFSC	f, b	Bit Test f, Skip if Clear	1 **(2)**	01	10bb	bfff	ffff		**3**
BTFSS	f, b	Bit Test f, Skip if Set	1 **(2)**	01	11bb	bfff	ffff		**3**
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	–	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	–	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	–	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	–	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTA, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is ‘`1`’ for a pin configured as input and is driven low by an external device, the data will be written back with a ‘`0`’.

2: If this instruction is executed on the TMR0 register (and where applicable, d = `1`), the prescaler will be cleared if assigned to the Timer0 module.

3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

MOVF — Move f

Syntax: [*label*] MOVF f,d

Operands: $0 \leq f \leq 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Description: The contents of register ‘f’ is moved to a destination dependent upon the status of ‘d’. If d = 0, destination is W register. If d = 1, the destination is file register ‘f’ itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:

```
MOVF    FSR, 0
```

After Instruction
W = value in FSR register
Z = 1

MOVWF — Move W to f

Syntax: [*label*] MOVWF f

Operands: $0 \leq f \leq 127$

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register ‘f’.

Words: 1

Cycles: 1

Example:

```
MOVW   OPTION
F
```

Before Instruction
OPTION = 0xFF
W = 0x4F
After Instruction
OPTION = 0x4F
W = 0x4F

MOVLW — Move literal to W

Syntax: [*label*] MOVLW k

Operands: $0 \leq k \leq 255$

Operation: k → (W)

Status Affected: None

Description: The eight-bit literal ‘k’ is loaded into W register. The “don’t cares” will assemble as ‘0’s.

Words: 1

Cycles: 1

Example:

```
MOVLW   0x5A
```

After Instruction
W = 0x5A

NOP — No Operation

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Words: 1

Cycles: 1

Example:

```
NOP
```

15.1 DC Characteristics: PIC16F610/616/16HV610/616-I (Industrial) PIC16F610/616/16HV610/616-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		PIC16F610/616	2.0	—	5.5	V	FOSC < = 4 MHz
D001		PIC16HV610/616	2.0	—	—(2)	V	FOSC < = 4 MHz
D001B		PIC16F610/616	2.0	—	5.5	V	FOSC < = 8 MHz
D001B		PIC16HV610/616	2.0	—	—(2)	V	FOSC < = 8 MHz
D001C		PIC16F610/616	3.0	—	5.5	V	FOSC < = 10 MHz
D001C		PIC16HV610/616	3.0	—	—(2)	V	FOSC < = 10 MHz
D001D		PIC16F610/616	4.5	—	5.5	V	FOSC < = 20 MHz
D001D		PIC16HV610/616	4.5	—	—(2)	V	FOSC < = 20 MHz
D002*	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3.1 "Power-on Reset (POR)"** for details.
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 12.3.1 "Power-on Reset (POR)"** for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: User defined. Voltage across the shunt regulator should not exceed 5V.

15.11 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O Port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 15-5: LOAD CONDITIONS

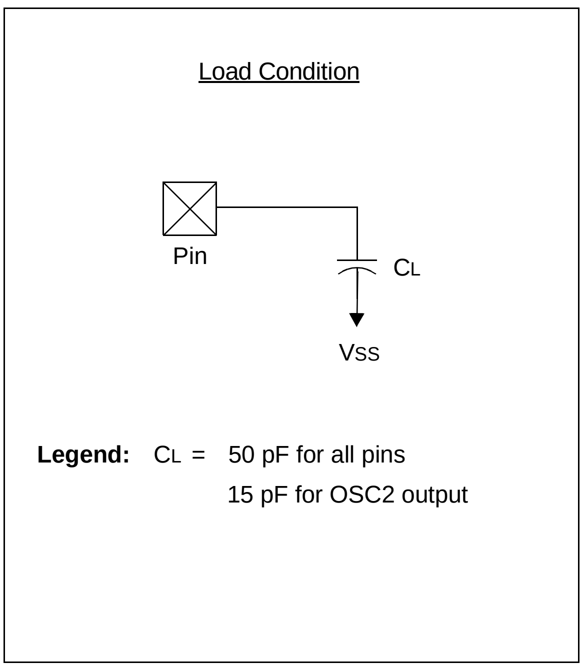


FIGURE 15-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

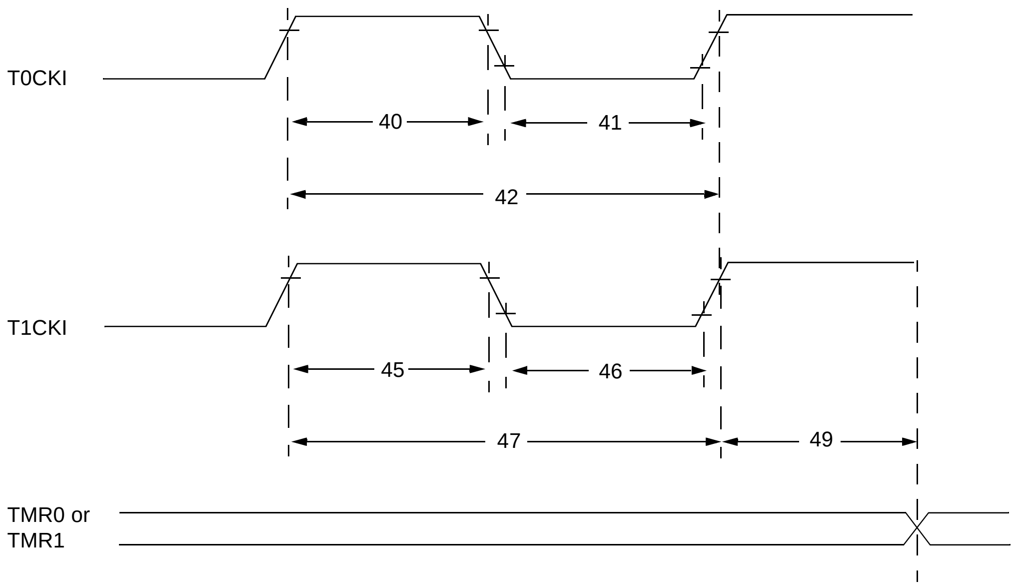


TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)
Operating Temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or (TCY + 40)/N	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or (TCY + 40)/N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		—	32.768	—	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 TOSC	—	7 TOSC	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-18: PIC16F616 IPD A/D vs. VDD

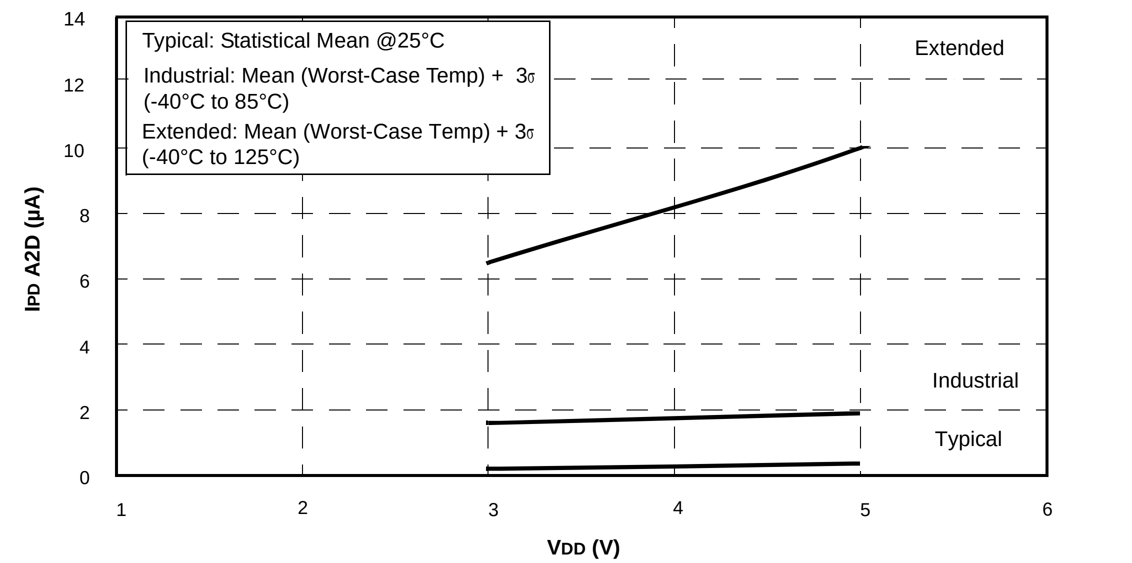


FIGURE 16-19: PIC16HV610/616 IDD LP (32 kHz) vs. VDD

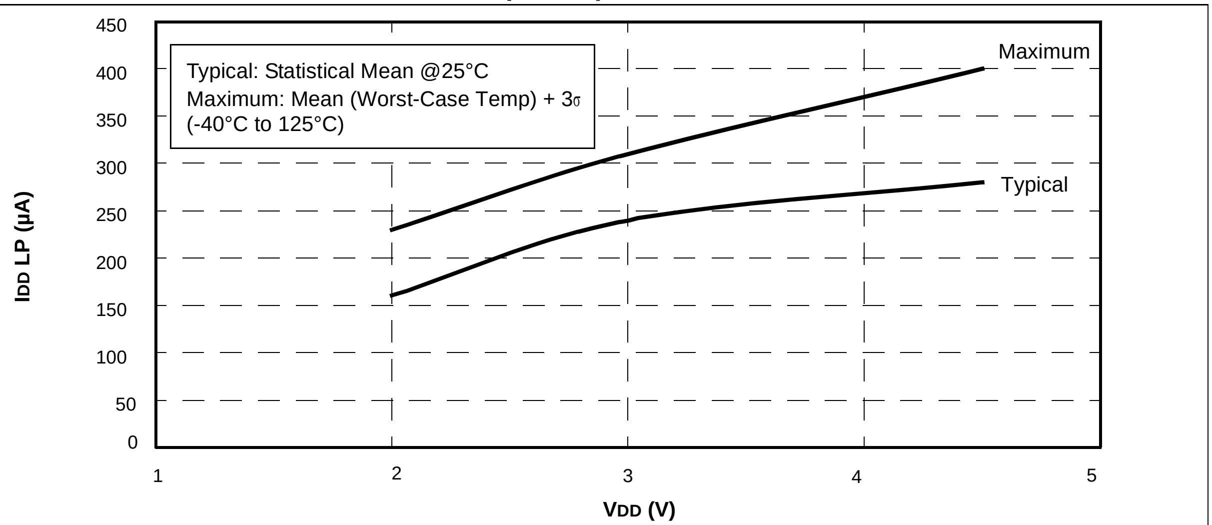


FIGURE 16-20: PIC16HV610/616 IDD EC (1 MHz) vs. VDD

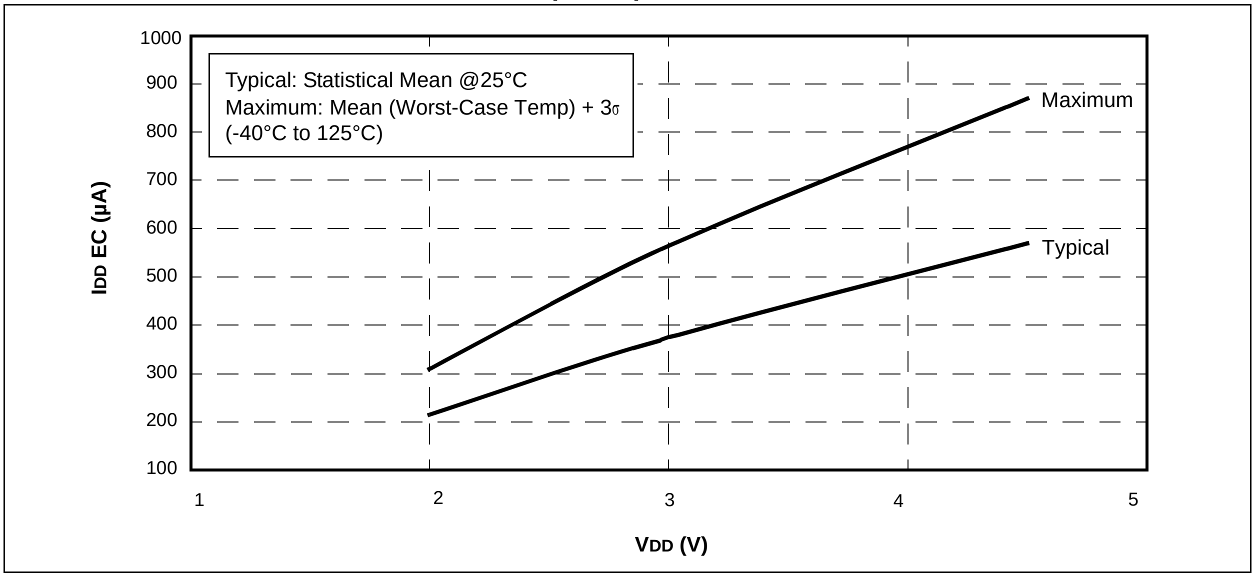


FIGURE 16-21: PIC16HV610/616 IDD EC (4 MHz) vs. VDD

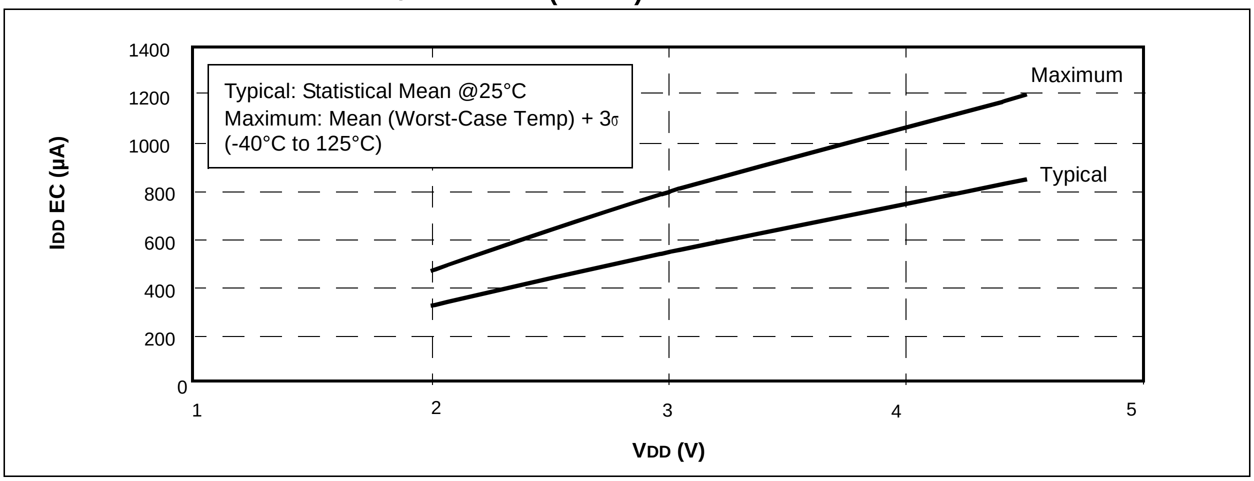


FIGURE 16-22: PIC16HV610/616 IDD XT (1 MHz) vs. VDD

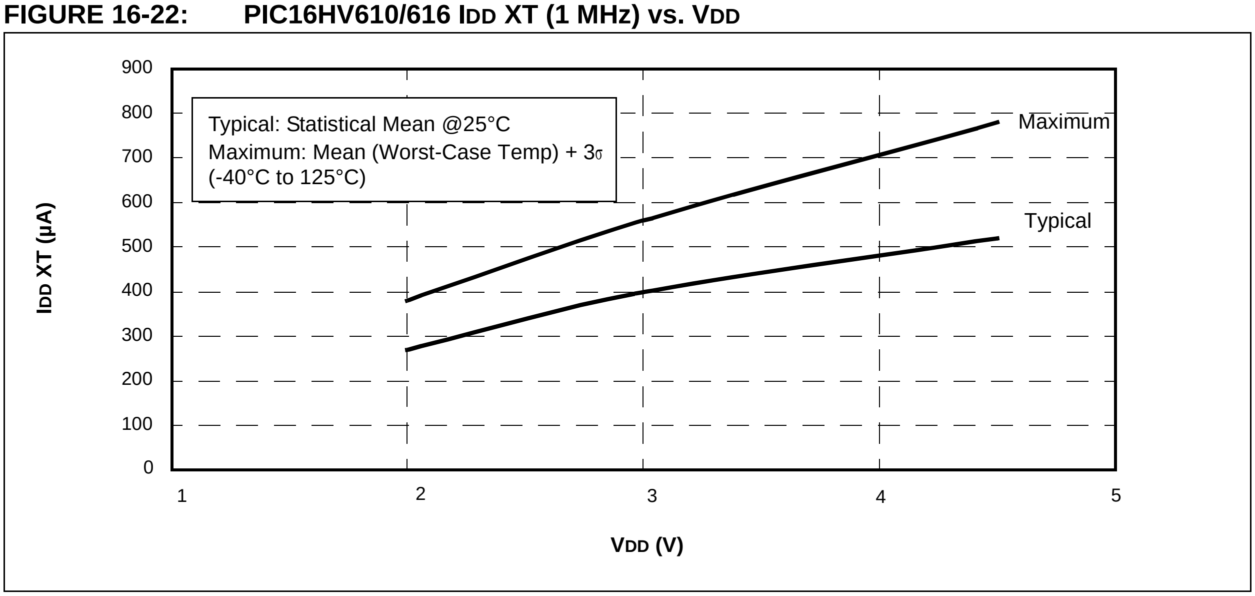


FIGURE 16-45: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)

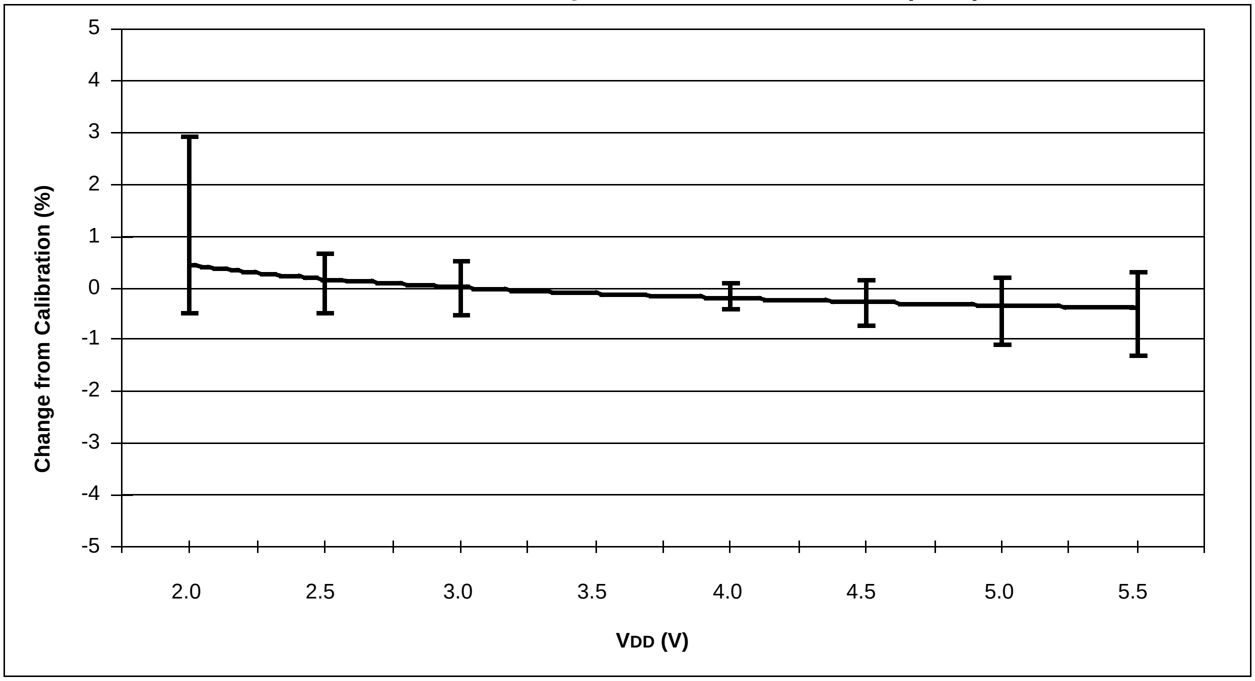


FIGURE 16-46: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (85°C)

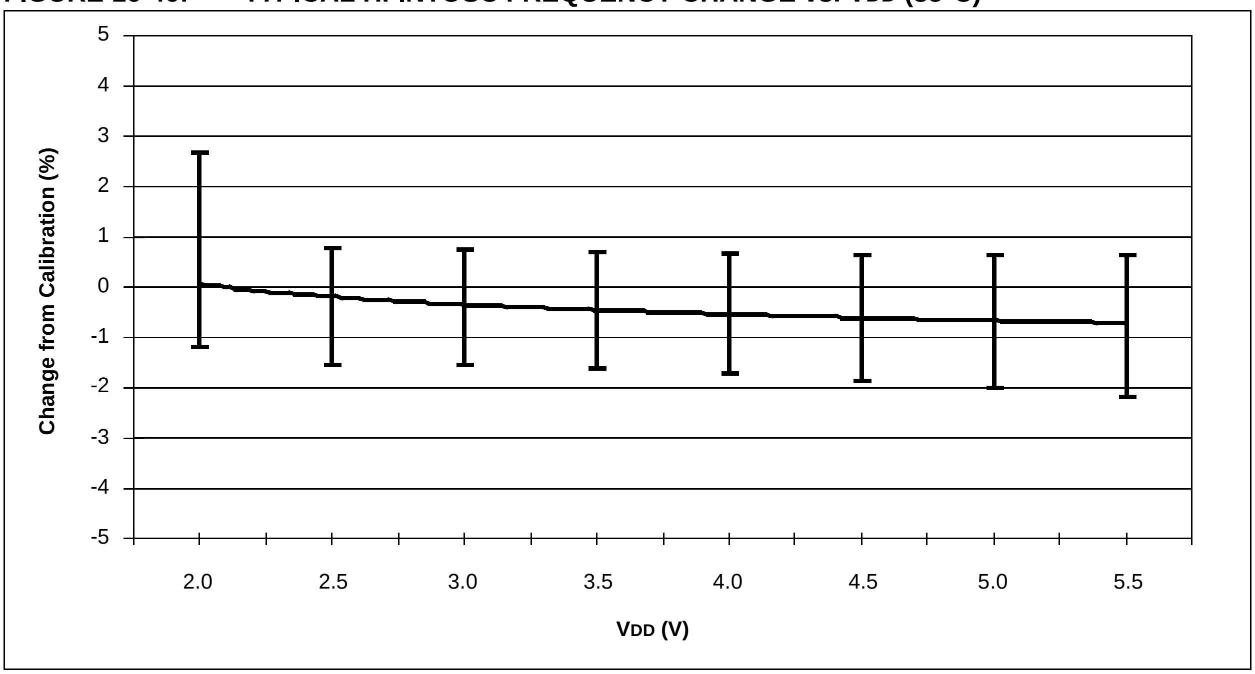


FIGURE 16-47: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (125°C)

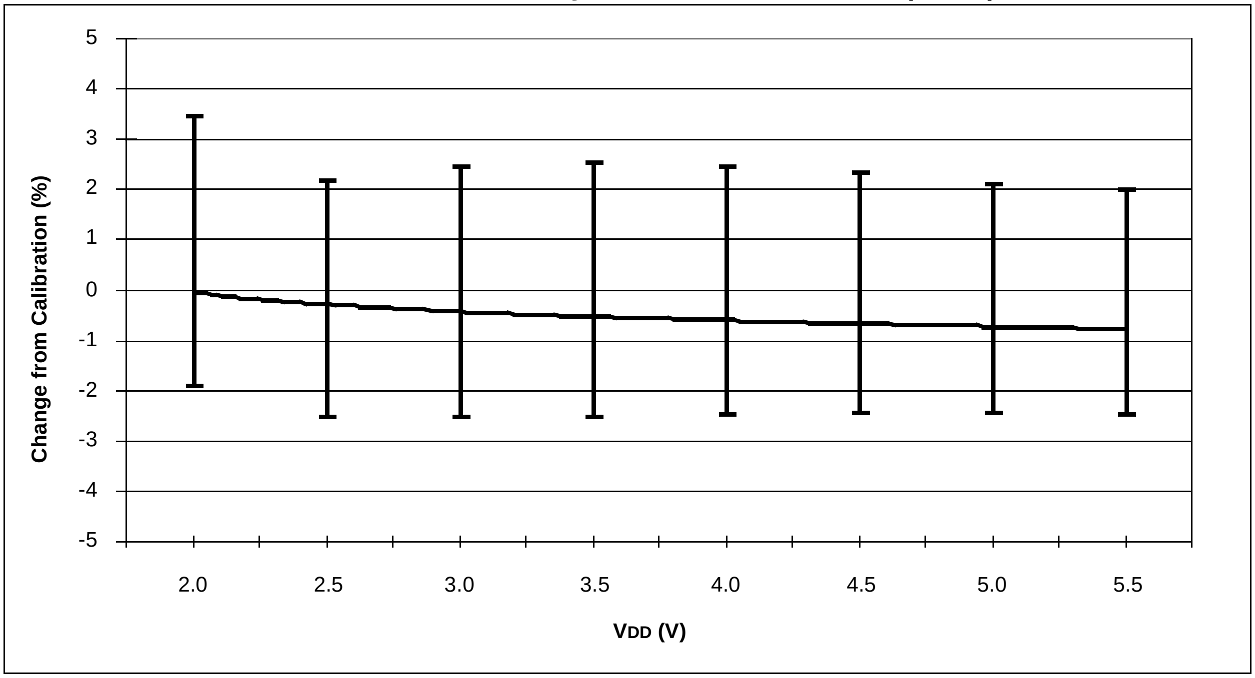


FIGURE 16-48: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)