



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	11
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv610-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-5 shows the two situations for the loading of the PC. The upper example in Figure 2-5 shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in Figure 2-5 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).

FIGURE 2-5: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register.

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 STACK

The PIC16F610/616/16HV610/616 Family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1: There are no Status bits to indicate stack overflow or stack underflow conditions.
 - 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-7.

A simple program to clear RAM location 40h-4Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1:	INDIRECT ADDRESSING

	MOVLW	0x40	;initialize pointer
	MOVWF	FSR	;to RAM
NEXT	CLRF	INDF	;clear INDF register
	INCF	FSR, F	;inc pointer
	BTFSS	FSR,4	;all done?
	GOTO	NEXT	;no clear next
CONTINU	JE		;yes continue

3.3.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/ CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the external RC mode connections.



FIGURE 3-5: EXTERNAL RC MODES

In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

3.4 Internal Clock Modes

The Oscillator module provides a selectable system clock source of either 4 MHz or 8 MHz. The selectable frequency is configured through the IOSCFS bit of the Configuration Word.

The frequency of the internal oscillator can be can be user-adjusted via software using the OSCTUNE register.

3.4.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See Section 12.0 "Special Features of the CPU" for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

3.4.1.1 OSCTUNE Register

The oscillator is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1). The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

REGISTER 3-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented: Read as '0'

bit 4-0

TUN<4:0>: Frequency Tuning bits
01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the manufacturer calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
CONFIG ⁽²⁾	IOSCFS	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCTUNE	_		_	TUN4	TUN3	TUN2	TUN1	TUN0	0 0000	u uuuu

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 12-1) for operation of all register bits.

4.2.4.5 RA4/AN3⁽¹⁾/T1G/OSC2/CLKOUT

Figure 4-4 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC⁽¹⁾

- a Timer1 gate (count enable)
- a crystal/resonator connection
- · a clock output
 - Note 1: PIC16F616/16HV616 only.



FIGURE 4-4: BLOCK DIAGRAM OF RA4

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CM2CON0	C2ON	C2OUT	C2OE	C2POL	_	C2R	C2CH1	C2CH0	0000 -000	0000 -000
CM2CON1	MC1OUT	MC2OUT	_	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC	00-0 0010	00-0 0010
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	_	ADIE ⁽¹⁾	CCP1IE ⁽¹⁾	C2IE	C1IE	_	TMR2IE ⁽¹⁾	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF ⁽¹⁾	CCP1IF ⁽¹⁾	C2IF	C1IF	_	TMR2IF ⁽¹⁾	TMR1IF	-000 0-00	-000 0-00
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register xxxx xxxx uuuu uuuu									
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: PIC16F616/16HV616 only.

8.8 Additional Comparator Features

There are three additional comparator features:

- Timer1 count enable (gate)
- Synchronizing output with Timer1
- Simultaneous read of comparator outputs

8.8.1 COMPARATOR C2 GATING TIMER1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CM2CON1 register will enable Timer1 to increment based on the output of Comparator C2. This requires that Timer1 is on and gating is enabled. See **Section 6.0 "Timer1 Module with Gate Control"** for details.

It is recommended to synchronize the comparator with Timer1 by setting the C2SYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

8.8.2 SYNCHRONIZING COMPARATOR C2 OUTPUT TO TIMER1

The Comparator C2 output can be synchronized with Timer1 by setting the C2SYNC bit of the CM2CON1 register. When enabled, the C2 output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 8-3) and the Timer1 Block Diagram (Figure 6-1) for more information.

8.8.3 SIMULTANEOUS COMPARATOR OUTPUT READ

The MC1OUT and MC2OUT bits of the CM2CON1 register are mirror copies of both comparator outputs. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note 1: Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

REGISTER 8-3: CM2CON1: COMPARATOR 2 CONTROL REGISTER 1

R-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0		
MC1OUT	MC2OUT	_	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC		
bit 7							bit (
Legend:									
R = Readable b	oit	W = Writable bi	t	U = Unimplem	ented bit, read as	s 'O'			
-n = Value at PC	DR	'1' = Bit is set		'0' = Bit is clea	red	x = Bit is unkno	own		
bit 7	MC1OUT: Mirro	or Copy of C1OU	T bit						
bit 6	MC2OUT: Mirro	or Copy of C2OU	T bit						
bit 5	Unimplemente	ed: Read as '0'							
bit 4	T1ACS: Timer1	1 Alternate Clock	Select bit						
	1 = Timer1 cloc	= Timer1 clock source is the system clock (Fosc)							
	0 = Timer1 cloc	ck source is the ir	nternal clock Fo	osc/4)					
bit 3	C1HYS: Comp	arator C1 Hyster	esis Enable bit						
	1 = Comparator C1 Hysteresis enabled								
	0 = Comparato	r C1 Hysteresis o	lisabled						
bit 2	C2HYS: Comp	arator C2 Hyster	esis Enable bit						
	$\perp = \text{Comparator C2 Hysteresis enabled}$								
bit 1		1 Cata Source Sc	loct bit						
$1 - \text{Timer1 date source is } \overline{\text{TIG}}$									
	0 = Timer1 gate	e source is SYNC	C2OUT.						
bit 0	C2SYNC: Com	parator C2 Outp	ut Synchronizat	ion bit					
	1 = C2 Output	is synchronous to	falling edge of	Timer1 clock					
	0 = C2 Output	is asynchronous							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1VREN	C2VREN	VRR	FVREN	VR3	VR2	VR1	VR0
bit 7							bit 0
1							
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 7	C1VREN: Co	mparator 1 Vol	tage Referenc	e Enable bit			
	1 = CVREF cir	cuit powered o	n and routed	to C1VREF inpu	ut of Comparato	or C1	
	0 = 0.6 Volt c	onstant referer	ice routed to C	1VREF input of	f Comparator C	:1	
bit 6	C2VREN: Co	mparator 2 Vol	tage Referenc	e Enable bit			
	1 = CVREF cir	cuit powered o	n and routed	to C2VREF inpu	ut of Comparato	or C2	
	0 = 0.6 Volt c	onstant referer	ice routed to C	2VREF input of	f Comparator C	2	
bit 5	VRR: CVREF	Range Selection	on bit				
	1 = Low range	e					
	0 = High rang	le					
bit 4	FVREN: Fixe	d Voltage Refe	rence (0.6V) E	Enable bit			
	1 = Enabled						
	0 = Disabled						
bit 3-0	VR<3:0>: Co	mparator Volta	ge Reference	CVREF Value S	Selection bits (C	\leq VR<3:0> \leq	15)
	<u>When VRR =</u>	<u>1</u> : CVREF = (V	R<3:0>/24) * \	VDD			
	When VRR =	<u>0</u> : CVREF = VD	0D/4 + (VR<3:0	0>/32) * Vdd			

REGISTER 8-6: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

9.2 ADC Operation

9.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/ DONE bit of the ADCON0 register to a '1' will start the analog-to-digital conversion.

Note:	The GO/DONE bit should not be set in the
	same instruction that turns on the ADC.
	Refer to Section 9.2.6 "A/D Conversion
	Procedure".

9.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

9.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete analog-to-digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note:	A device Reset forces all registers to their
	Reset state. Thus, the ADC module is
	turned off and any pending conversion is
	terminated.

9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The ECCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not ensure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See Section 10.0 "Enhanced Capture/Compare/ PWM (With Auto-Shutdown and Dead Band) Module (PIC16F616/16HV616 Only)" for more information.

9.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an analog-to-digital conversion:

- 1. Configure Port:
 - Disable pin output driver (See TRIS register)
 - Configure pin as analog
- 2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Select result format
 - Turn on ADC module
- 3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - · Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
- 4. Wait the required acquisition time⁽²⁾.
- 5. Start conversion by setting the GO/DONE bit.
- 6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
- 7. Read ADC Result
- 8. Clear the ADC interrupt flag (required if interrupt is enabled).
 - **Note 1:** The global interrupt may be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.
 - 2: See Section 9.3 "A/D Acquisition Requirements".

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0 ⁽¹⁾	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000	0000 0000
ADCON1 ⁽¹⁾	_	ADCS2	ADCS1	ADCS0	—	_			-000	-000
ANSEL	ANS ANS6 ANS5 ANS4 ANS3 ⁽¹⁾ ANS2 ⁽¹⁾ ANS1 ANS0						1111 1111	1111 1111		
ADRESH ^(1,2)	A/D Result Register High Byte						xxxx xxxx	uuuu uuuu		
ADRESL ^(1,2)	A/D Result Register Low Byte							xxxx xxxx	uuuu uuuu	
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	- ADIE ⁽¹⁾ CCP1IE ⁽¹⁾ C2IE C1IE - TMR2IE ⁽¹⁾ TMR1IE						TMR1IE	-000 0-00	-000 0-00	
PIR1	- ADIF ⁽¹⁾ CCP1IF ⁽¹⁾ C2IF C1IF - TMR2IF ⁽¹⁾ TMR1IF						-000 0-00	-000 0-00		
PORTA	— — RA5 RA4 RA3 RA2 RA1 RA0							x0 x000	u0 u000	
PORTC	_	_	RC5	RC4	RC3	RC2	RC1	RC0	xx 00xx	uu 00uu
TRISA	—	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111
TRISC	_	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	11 1111	11 1111

TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for ADC module. Legend:

Note 1:

PIC16F616/16HV616 only. 2: Read-only Register.

10.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- · Every falling edge
- · Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 10-1).

10.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCP1 pin is configured as an output,							
	a write to the port can cause a capture							
	condition.							

FIGURE 10-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

10.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

10.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 10-1).

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

BANKSEI	CCP1CON	;Set Bank bits to point
		;to CCP1CON
CLRF	CCP1CON	;Turn CCP module off
MOVLW	NEW_CAPT_PS	G;Load the W reg with
		; the new prescaler
MOVWF	CCP1CON	; move value and CCP ON ;Load CCP1CON with this
		; value

FIGURE 10-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)

			-	Period	
00	(Single Output)	P1A Modulated			Ì
		P1A Modulated			
10	(Half-Bridge)	P1B Modulated	_ ! !		
		P1A Active	- !		 :
01	(Full-Bridge, Forward)	P1B Inactive	- ;		
		P1C Inactive	_ ; 		
		P1D Modulated		i	
		P1A Inactive	- :		
11	(Full-Bridge,	P1B Modulated			
	Reverse)	P1C Active			
		P1D Inactive —	_ ' _ '	1	<u> </u>

Note 1: Dead-band delay is programmed using the PWM1CON register (Section 10.4.6 "Programmable Dead-Band Delay mode").

10.4.2 FULL-BRIDGE MODE

In Full-Bridge mode, all four pins are used as outputs. An example of full-bridge application is shown in Figure 10-10.

In the Forward mode, pin CCP1/P1A is driven to its active state, pin P1D is modulated, while P1B and P1C will be driven to their inactive state as shown in Figure 10-11.

In the Reverse mode, P1C is driven to its active state, pin P1B is modulated, while P1A and P1D will be driven to their inactive state as shown Figure 10-11. P1A, P1B, P1C and P1D outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the P1A, P1B, P1C and P1D pins as outputs.

FIGURE 10-10: EXAMPLE OF FULL-BRIDGE APPLICATION



DECFSZ	Decrement f, Skip if 0
Syntax:	[label] DECFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) - 1 \rightarrow (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a two-cycle instruction.

INCFSZ	Increment f, Skip if 0				
Syntax:	[label] INCFSZ f,d				
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$				
Operation:	(f) + 1 \rightarrow (destination), skip if result = 0				
Status Affected:	None				
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a two-cycle instruction.				

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	$k \rightarrow PC<10:0>$ PCLATH<4:3> \rightarrow PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

IORLW	Inclusive OR literal with W					
Syntax:	[<i>label</i>] IORLW k					
Operands:	$0 \leq k \leq 255$					
Operation:	(W) .OR. $k \rightarrow$ (W)					
Status Affected:	Z					
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.					

INCF	Increment f				
Syntax:	[label] INCF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$				
Operation:	(f) + 1 \rightarrow (destination)				
Status Affected:	Z				
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.				

IORWF	Inclusive OR W with f				
Syntax:	[<i>label</i>] IORWF f,d				
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$				
Operation:	(W) .OR. (f) \rightarrow (destination)				
Status Affected:	Z				
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.				

NOTES:

15.10 Thermal Considerations

Standard Operating	Operating (temperature	Conditions (unless otherwise $-40^{\circ}C \le TA \le +125^{\circ}C$	e stated)		
Param No.	Sym	Characteristic	Тур	Units	Conditions
TH01	θJA	Thermal Resistance	70*	C/W	14-pin PDIP package
		Junction to Ambient	85.0*	C/W	14-pin SOIC package
			100*	C/W	14-pin TSSOP package
			37*	C/W	16-pin QFN 4x4mm package
TH02	θJC	Thermal Resistance	32.5*	C/W	14-pin PDIP package
		Junction to Case	31.0*	C/W	14-pin SOIC package
			31.7*	C/W	14-pin TSSOP package
			2.6*	C/W	16-pin QFN 4x4mm package
TH03	TDIE	Die Temperature	150*	С	
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD (NOTE 1)
TH06	Pi/o	I/O Power Dissipation	—	W	$PI/O = \Sigma (IOL * VOL) + \Sigma (IOH * (VDD - VOH))$
TH07	Pder	Derated Power	_	W	Pder = PDmax (Tdie - Ta)/θja (NOTE 2)
*	These para	meters are characterized but n	ot tested		

These parameters are characterized but not tested.

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

15.13 High Temperature Operation

This section outlines the specifications for <u>the</u> <u>PIC16F616 device operating in a temperature range</u> <u>between -40°C and 150°C.⁽⁴⁾</u> The specifications between -40°C and 150°C⁽⁴⁾ are identical to those shown in DS41302 and DS80329.

Note 1:	Writes	are	<u>not</u>	allowed	for	Flash	
	Program Memory above 125°C.						
э.	All AC timing specifications are increased						

- All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.
- **3:** The temperature range indicator in the part number is "H" for -40°C to 150°C.⁽⁴⁾

Example: PIC16F616T-H/ST indicates the device is shipped in a tAPE and reel configuration, in the TSSOP package, and is rated for operation from -40°C to 150°C.⁽⁴⁾

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

TABLE 15-13: ABSOLUTE MAXIMUM RATINGS

Parameter	Source/Sink	Value	Units
Max. Current: VDD	Source	20	mA
Max. Current: Vss	Sink	50	mA
Max. Current: PIN	Source	5	mA
Max. Current: PIN	Sink	10	mA
Pin Current: at Voн	Source	3	mA
Pin Current: at VoL	Sink	8.5	mA
Port Current: A and C	Source	20	mA
Port Current: A and C	Sink	50	mA
Maximum Junction Temperature		155	°C

Note: Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Param No.	Sym	Characteristic	Frequency Tolerance	Units	Min	Тур	Max	Conditions
OS08	INTosc	Int. Calibrated INTOSC Freq. ⁽¹⁾	±10%	MHz	7.2	8.0	8.8	$\begin{array}{l} 2.0V \leq V \text{DD} \leq 5.5 \text{V} \\ \text{-40}^{\circ}\text{C} \leq \text{TA} \leq 150^{\circ}\text{C} \end{array}$

TABLE 15-18: OSCILLATOR PARAMETERS FOR PIC16F616 - H (High Temp.)

Note 1: To ensure these oscillator frequency tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

TABLE 15-19: COMPARATOR SPECIFICATIONS FOR PIC16F616 – H (High Temp.)

Param No.	Sym	Characteristic	Units	Min	Тур	Max	Conditions
CM01	Vos	Input Offset Voltage	mV		±5	±20	(Vdd - 1.5)/2



FIGURE 16-16: PIC16F610/616 IPD CVREF (HI RANGE) vs. VDD





14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS				
Dimension	Dimension Limits		NOM	MAX		
Contact Pitch	E	1.27 BSC				
Contact Pad Spacing	С		5.40			
Contact Pad Width	Х			0.60		
Contact Pad Length	Y			1.50		
Distance Between Pads	Gx	0.67				
Distance Between Pads	G	3.90				

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A