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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	11
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv610t-i-sl

PIC16F616/16HV616 16-Pin Diagram (QFN)

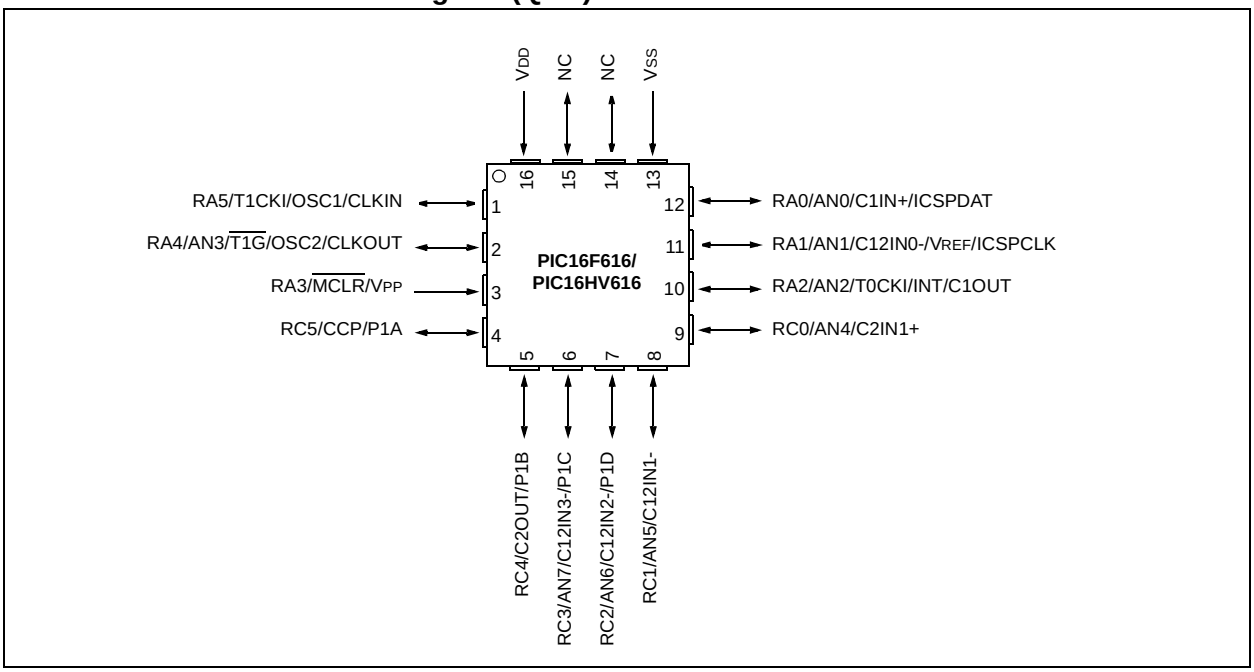

TABLE 4: PIC16F616/16HV616 16-PIN SUMMARY

I/O	Pin	Analog	Comparators	Timers	CCP	Interrupts	Pull-ups	Basic
RA0	12	AN0	C1IN+	—	—	IOC	Y	ICSPDAT
RA1	11	AN1/VREF	C12IN0-	—	—	IOC	Y	ICSPCLK
RA2	10	AN2	C1OUT	T0CKI	—	INT/IOC	Y	—
RA3(1)	3	—	—	—	—	IOC	Y(2)	MCLR/VPP
RA4	2	AN3	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	1	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RC0	9	AN4	C2IN+	—	—	—	—	—
RC1	8	AN5	C12IN1-	—	—	—	—	—
RC2	7	AN6	C12IN2-	—	P1D	—	—	—
RC3	6	AN7	C12IN3-	—	P1C	—	—	—
RC4	5	—	C2OUT	—	P1B	—	—	—
RC5	4	—	—	—	CCP1/P1A	—	—	—
—	16	—	—	—	—	—	—	VDD
—	13	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

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TABLE 1-2: PIC16F616/16HV616 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT	RA0	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	C1IN+	AN	—	Comparator C1 non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
RA1/AN1/C12IN0-/VREF/ICSPCLK	RA1	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	C12IN0-	AN	—	Comparators C1 and C2 inverting input
	VREF	AN	—	External Voltage Reference for A/D
	ICSPCLK	ST	—	Serial Programming Clock
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator C1 output
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	PORTA input with interrupt-on-change
	$\overline{\text{MCLR}}$	ST	—	Master Clear w/internal pull-up
	VPP	HV	—	Programming voltage
RA4/AN3/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	$\overline{\text{T1G}}$	ST	—	Timer1 gate (count enable)
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock input
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RC0/AN4/C2IN+	RC0	TTL	CMOS	PORTC I/O
	AN4	AN	—	A/D Channel 4 input
	C2IN+	AN	—	Comparator C2 non-inverting input
RC1/AN5/C12IN1-	RC1	TTL	CMOS	PORTC I/O
	AN5	AN	—	A/D Channel 5 input
	C12IN1-	AN	—	Comparators C1 and C2 inverting input
RC2/AN6/C12IN2-/P1D	RC2	TTL	CMOS	PORTC I/O
	AN6	AN	—	A/D Channel 6 input
	C12IN2-	AN	—	Comparators C1 and C2 inverting input
	P1D	—	CMOS	PWM output
RC3/AN7/C12IN3-/P1C	RC3	TTL	CMOS	PORTC I/O
	AN7	AN	—	A/D Channel 7 input
	C12IN3-	AN	—	Comparators C1 and C2 inverting input
	P1C	—	CMOS	PWM output
RC4/C2OUT/P1B	RC4	TTL	CMOS	PORTC I/O
	C2OUT	—	CMOS	Comparator C2 output
	P1B	—	CMOS	PWM output
RC5/CCP1/P1A	RC5	TTL	CMOS	PORTC I/O
	CCP1	ST	CMOS	Capture input/Compare output
	P1A	—	CMOS	PWM output
VDD	VDD	Power	—	Positive supply
VSS	VSS	Power	—	Ground reference

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; HV = High Voltage
ST = Schmitt Trigger input with CMOS levels; TTL = TTL compatible input; XTAL = Crystal

2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-2) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the $\overline{BOR}$.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0(1)
—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: Reads as '0' if Brown-out Reset is disabled.

3.4.1.1 OSCTUNE Register

The oscillator is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

REGISTER 3-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the manufacturer calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets(1)
CONFIG(2)	IOSCFS	$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by oscillators.
Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.
2: See Configuration Word register (Register 12-1) for operation of all register bits.

NOTES:

8.10 Comparator SR Latch

The SR latch module provides additional control of the comparator outputs. The module consists of a single SR latch and output multiplexers. The SR latch can be set, reset or toggled by the comparator outputs. The SR latch may also be set or reset, independent of comparator output, by control bits in the SRCON0 control register. The SR latch output multiplexers select whether the latch outputs or the comparator outputs are directed to the I/O port logic for eventual output to a pin.

The SR latch also has a variable clock, which is connected to the set input of the latch. The SRCLKEN bit of SRCON0 enables the SR latch set clock. The clock will periodically pulse the set input of the latch. Control over the frequency of the SR latch set clock is provided by the SRCS<1:0> bits of SRCON1 register.

8.10.1 LATCH OPERATION

The latch is a Set-Reset latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. Each latch input is connected to a comparator output and a software controlled pulse generator. The latch can be set by C1OUT or the PULSS bit of the SRCON0 register. The latch can be reset by C2OUT or the PULSR bit of the SRCON0 register. The latch is reset-dominant, therefore, if both Set and Reset inputs are high the latch will go to the Reset state. Both the PULSS and PULSR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

8.10.2 LATCH OUTPUT

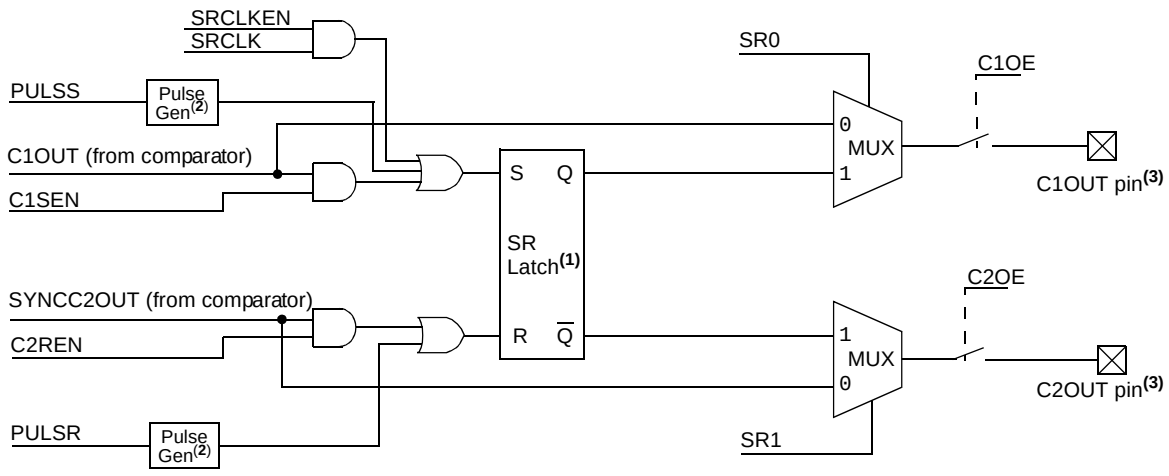
The SR<1:0> bits of the SRCON0 register control the latch output multiplexers and determine four possible output configurations. In these four configurations, the CxOUT I/O port logic is connected to:

- C1OUT and C2OUT
- C1OUT and SR latch $\overline{Q}$
- C2OUT and SR latch Q
- SR latch Q and $\overline{Q}$

After any Reset, the default output configuration is the unlatched C1OUT and C2OUT mode. This maintains compatibility with devices that do not have the SR latch feature.

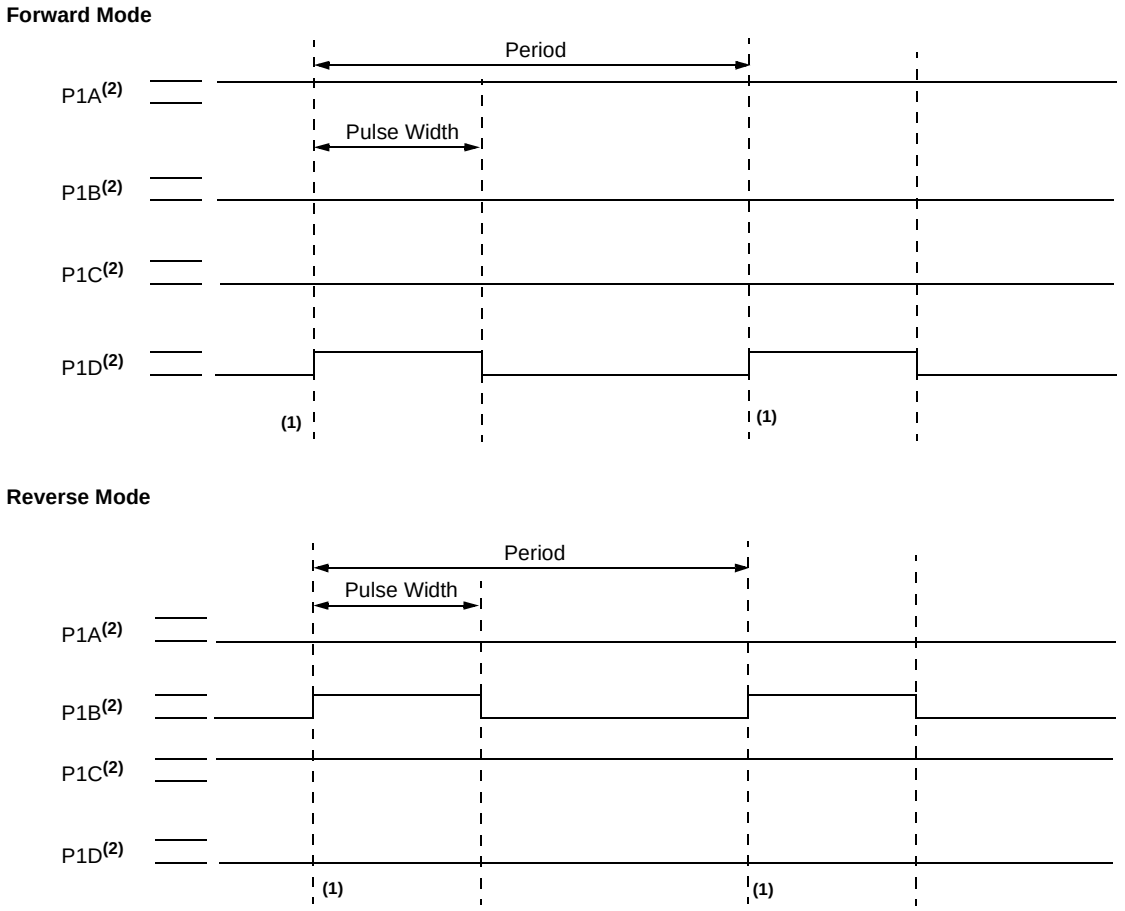
The applicable TRIS bits of the corresponding ports must be cleared to enable the port pin output drivers. Additionally, the CxOE comparator output enable bits of the CMxCON0 registers must be set in order to make the comparator or latch outputs available on the output pins. The latch configuration enable states are completely independent of the enable states for the comparators.

FIGURE 8-8: SR LATCH SIMPLIFIED BLOCK DIAGRAM



Note 1: If R = 1 and S = 1 simultaneously, Q = 0, $\overline{Q}$ = 1
2: Pulse generator causes a 1 TOSC pulse width.
3: Output shown for reference only. See I/O port pin block diagram for more detail.

FIGURE 10-11: EXAMPLE OF FULL-BRIDGE PWM OUTPUT



Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: Output signal is shown as active-high.

12.3.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC16F610/616/16HV610/616 device operating in parallel.

Table 12-5 shows the Reset conditions for some special registers, while Table 12-4 shows the Reset conditions for all the registers.

12.3.6 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ = 0, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., V_{DD} may have gone too low).

For more information, see **Section 12.3.4 "Brown-out Reset (BOR)"**.

TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	
XT, HS, LP	T_{PWRT} + 1024 • T_{OSC}	1024 • T_{OSC}	T_{PWRT} + 1024 • T_{OSC}	1024 • T_{OSC}	1024 • T_{OSC}
RC, EC, INTOSC	T_{PWRT}	—	T_{PWRT}	—	—

TABLE 12-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	x	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	1	0	$\overline{\text{MCLR}}$ Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets(1)
PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---- --qq	---- --uu
STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

12.10 In-Circuit Serial Programming™

The PIC16F610/616/16HV610/616 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five connections for:

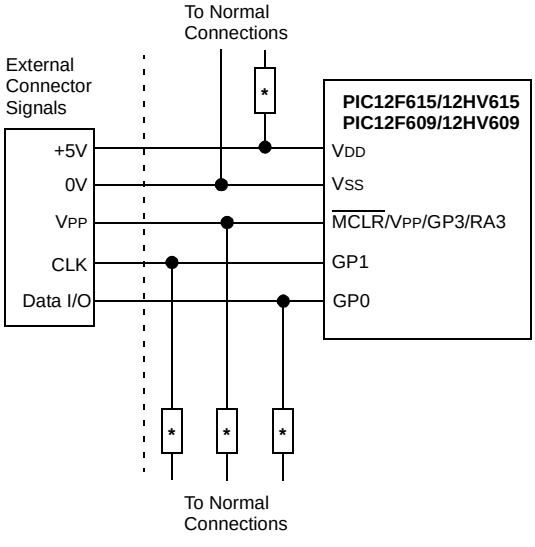
- clock
- data
- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the MCLR (V_{PP}) pin from V_{IL} to V_{IHH}. See the *Memory Programming Specification* (DS41284) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in Program/Verify mode.

A typical In-Circuit Serial Programming connection is shown in Figure 12-10.

FIGURE 12-10: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING™ CONNECTION



* Isolation devices (as required)

Note:	To erase the device V_{DD} must be above the Bulk Erase V_{DD} minimum given in the *Memory Programming Specification* (DS41284)

12.11 In-Circuit Debugger

Since in-circuit debugging requires access to three pins, MPLAB® ICD 2 development with an 14-pin device is not practical. A special 28-pin PIC16F610/616/16HV610/616 ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC16F610/616/16HV610/616 device. The debugging adapter is the only source of the ICD device.

When the ICD pin on the PIC16F610/616/16HV610/616 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-9 shows which features are consumed by the background debugger.

TABLE 12-9: DEBUGGER RESOURCES

Resource	Description
I/O pins	ICDCLK, ICDDATA
Stack	1 level
Program Memory	Address 0h must be NOP 700h-7FFh

For more information, see "*MPLAB® ICD 2 In-Circuit Debugger User's Guide*" (DS51331), available on Microchip's web site (www.microchip.com).

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (F.) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

15.3 DC Characteristics: PIC16HV610/616-I (Industrial) PIC16HV610/616-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	**Supply Current (IDD)(1, 2)** PIC16HV610/616	—	160	230	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	240	310	µA	3.0	
		—	280	400	µA	4.5	
D011*		—	270	380	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	400	560	µA	3.0	
		—	520	780	µA	4.5	
D012		—	380	540	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	575	810	µA	3.0	
		—	0.875	1.3	mA	4.5	
D013*		—	215	310	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	375	565	µA	3.0	
		—	570	870	µA	4.5	
D014		—	330	475	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	550	800	µA	3.0	
		—	0.85	1.2	mA	4.5	
D016*		—	310	435	µA	2.0	FOSC = 4 MHz INTOSC mode
		—	500	700	µA	3.0	
		—	0.74	1.1	mA	4.5	
D017		—	460	650	µA	2.0	FOSC = 8 MHz INTOSC mode
		—	0.75	1.1	mA	3.0	
		—	1.2	1.6	mA	4.5	
D018		—	320	465	µA	2.0	FOSC = 4 MHz EXTRC mode(3)
		—	510	750	µA	3.0	
		—	0.770	1.0	mA	4.5	
D019		—	2.5	3.4	mA	4.5	FOSC = 20 MHz HS Oscillator mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

15.4 DC Characteristics: PIC16F610/616- I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020	**Power-down Base Current(IPD)(2)**	—	0.05	0.9	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	1.2	µA	3.0	
	PIC16F610/616	—	0.35	1.5	µA	5.0	
		—	150	500	nA	3.0	-40°C ≤ TA ≤ +25°C for industrial
D021		—	0.5	1.5	µA	2.0	WDT Current(1)
		—	2.5	4.0	µA	3.0	
		—	9.5	17	µA	5.0	
D022		—	5.0	9	µA	3.0	BOR Current(1)
		—	6.0	12	µA	5.0	
D023		—	105	115	µA	2.0	Comparator Current(1), both comparators enabled
		—	110	125	µA	3.0	
		—	116	140	µA	5.0	
D024		—	50	60	µA	2.0	Comparator Current(1), single comparator enabled
		—	55	65	µA	3.0	
		—	60	75	µA	5.0	
D025		—	30	40	µA	2.0	CVREF Current(1) (high range)
		—	45	60	µA	3.0	
		—	75	105	µA	5.0	
D026*		—	39	50	µA	2.0	CVREF Current(1) (low range)
		—	59	80	µA	3.0	
		—	98	130	µA	5.0	
D027		—	5.5	10	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	7.0	12	µA	3.0	
		—	8.5	14	µA	5.0	
D028		—	0.2	1.6	µA	3.0	A/D Current(1), no conversion in progress.
		—	0.36	1.9	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

TABLE 15-7: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristics**		**Min**	**Typ†**	**Max**	**Units**	**Comments**
CM01	VOS	Input Offset Voltage(2)		—	± 5.0	± 10	mV	
CM02	VCM	Input Common Mode Voltage		0	—	VDD – 1.5	V	
CM03*	CMRR	Common Mode Rejection Ratio		+55	—	—	dB	
CM04*	TRT	Response Time(1)	Falling	—	150	600	ns	
			Rising	—	200	1000	ns	
CM05*	TMC2COV	Comparator Mode Change to Output Valid		—	—	10	µs	
CM06*	VHYS	Input Hysteresis Voltage		—	45	60	mV	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV. The other input is at (VDD -1.5)/2.

2: Input offset voltage is measured with one comparator input at (VDD - 1.5V)/2.

TABLE 15-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Comments**
CV01	CLSB	Step Size(2)	— —	VDD/24 VDD/32	— —	V V	Low Range (VRR = 1) High Range (VRR = 0)
CV02	CACC	Absolute Accuracy(3)	— —	— —	± 1/2 ± 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03	CR	Unit Resistor Value (R)	—	2k	—	Ω	
CV04	CST	Settling Time(1)	—	—	10	µs	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

2: See **Section 8.11 "Comparator Voltage Reference"** for more information.

3: Absolute Accuracy when CVREF output is ≤ (VDD-1.5).

TABLE 15-9: VOLTAGE REFERENCE SPECIFICATIONS

VR Voltage Reference Specifications			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VR01	VP6OUT	VP6 voltage output	0.50	0.6	0.7	V	
VR02	V1P2OUT	V1P2 voltage output	1.05	1.20	1.35	V	
VR03*	TSTABLE	Settling Time	—	10	—	µs	

* These parameters are characterized but not tested.

TABLE 15-10: SHUNT REGULATOR SPECIFICATIONS (PIC16HV610/616 only)

SHUNT REGULATOR CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
SR01	VSHUNT	Shunt Voltage	4.75	5	5.4	V	
SR02	ISHUNT	Shunt Current	4	—	50	mA	
SR03*	TSETTLE	Settling Time	—	—	150	ns	To 1% of final value
SR04	CLOAD	Load Capacitance	0.01	—	10	µF	Bypass capacitor on VDD pin
SR05	ΔISNT	Regulator operating current	—	180	—	µA	Includes band gap reference current

* These parameters are characterized but not tested.

TABLE 15-11: PIC16F616/16HV616 A/D CONVERTER (ADC) CHARACTERISTICS:

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	±1	LSb	VREF = 5.12V**(5)**
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.12V**(5)**
AD04	EOFF	Offset Error	—	+1.5	+ 2.0	LSb	VREF = 5.12V**(5)**
AD07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.12V**(5)**
AD06 AD06A	VREF	Reference Voltage**(3)**	2.2 2.5	—	— VDD	V	 Absolute minimum to ensure 1 LSb accuracy
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	IREF	VREF Input Current**(3)**	10	—	1000	µA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	µA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

5: VREF = 5V for PIC16HV616.

FIGURE 16-10: PIC16F610/616 IPD BASE vs. VDD

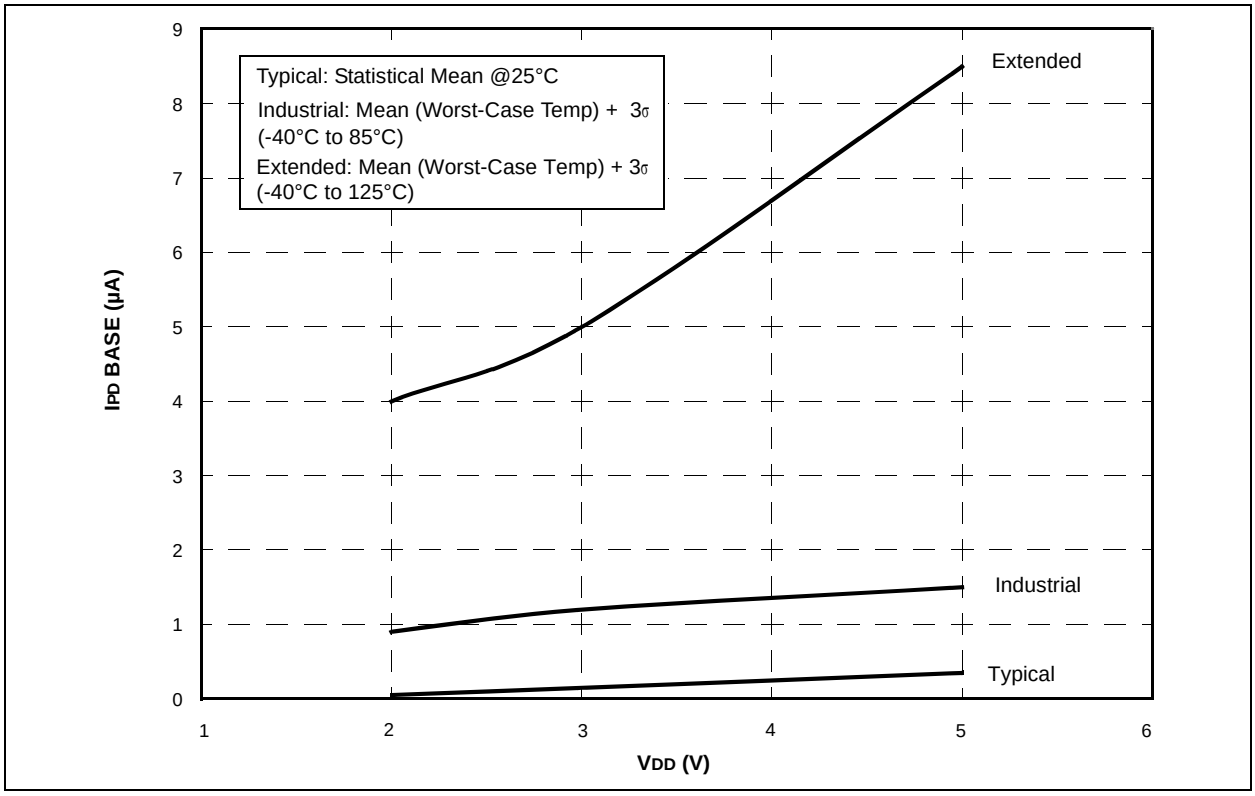


FIGURE 16-11: PIC16F610/616 IPD COMPARATOR (SINGLE ON) vs. VDD

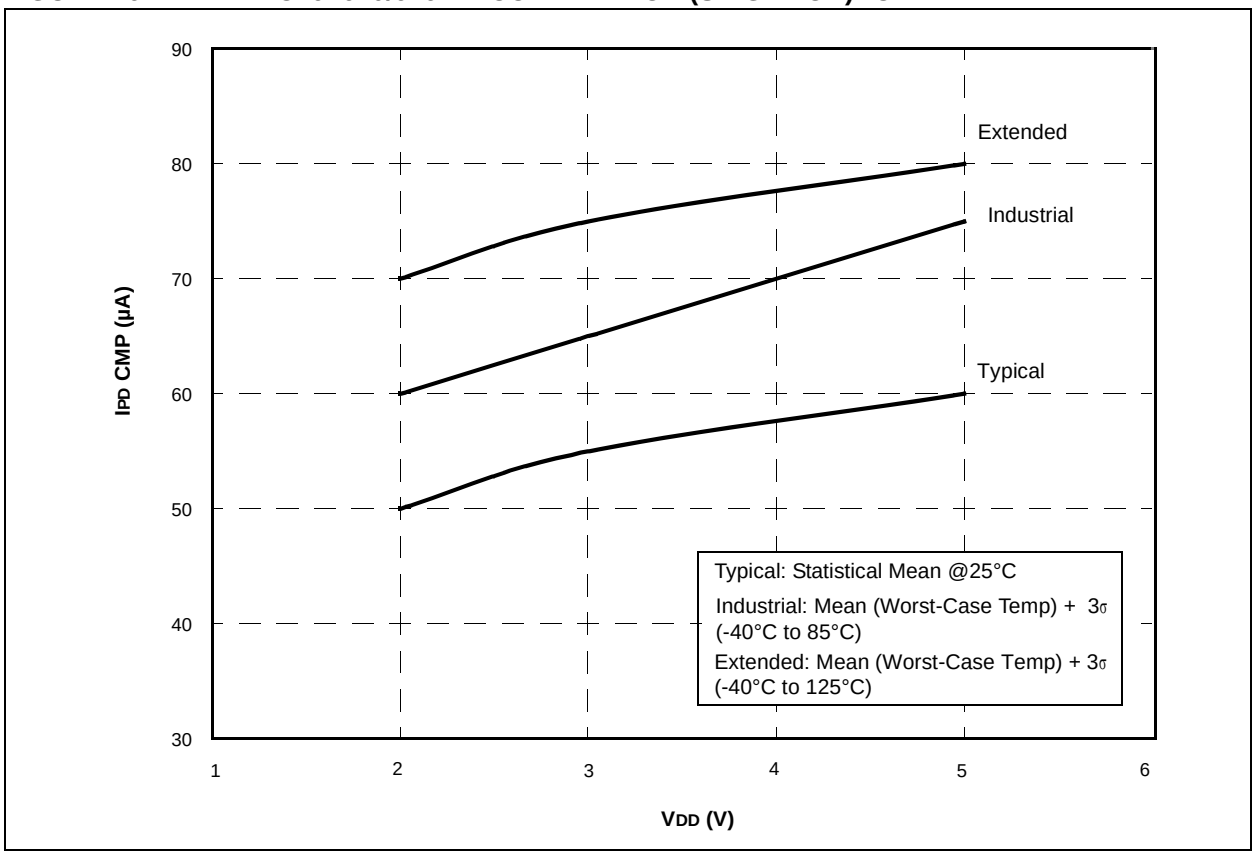


FIGURE 16-26: PIC16HV610/616 IDD EXTRC (4 MHz) vs. VDD

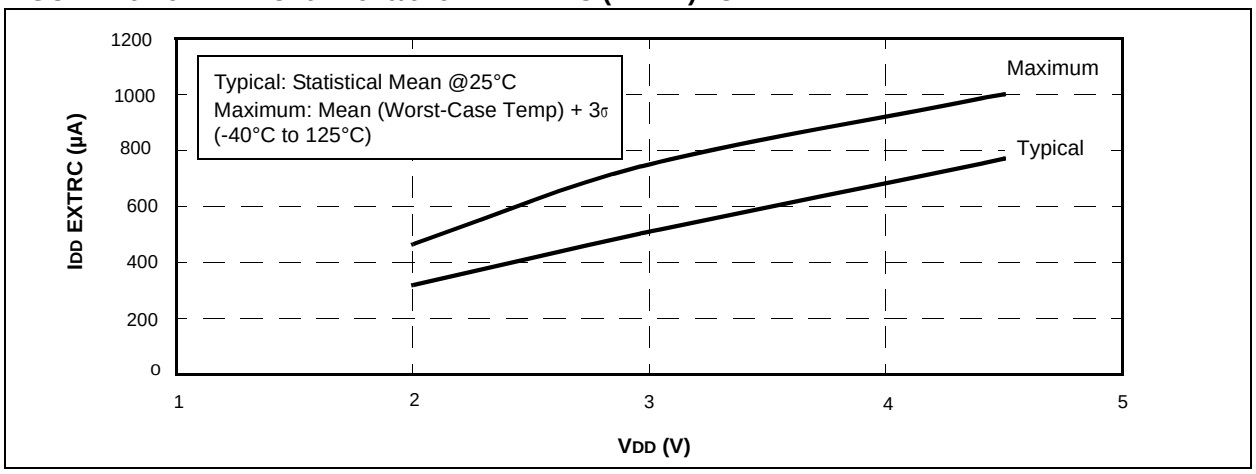


FIGURE 16-27: PIC16HV610/616 IPD BASE vs. VDD

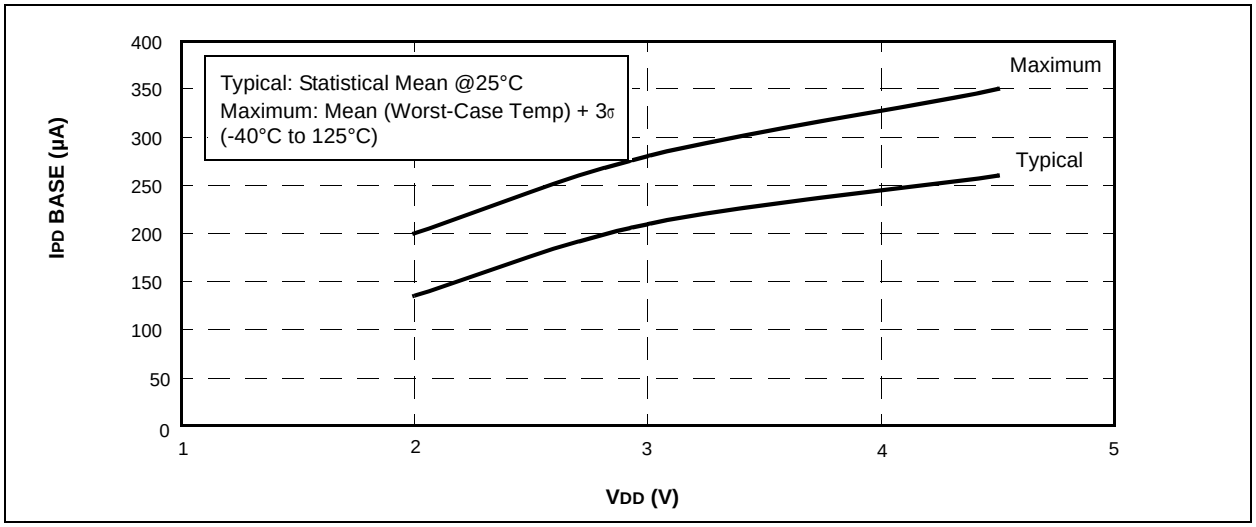


FIGURE 16-28: PIC16HV610/616 IPD COMPARATOR (SINGLE ON) vs. VDD

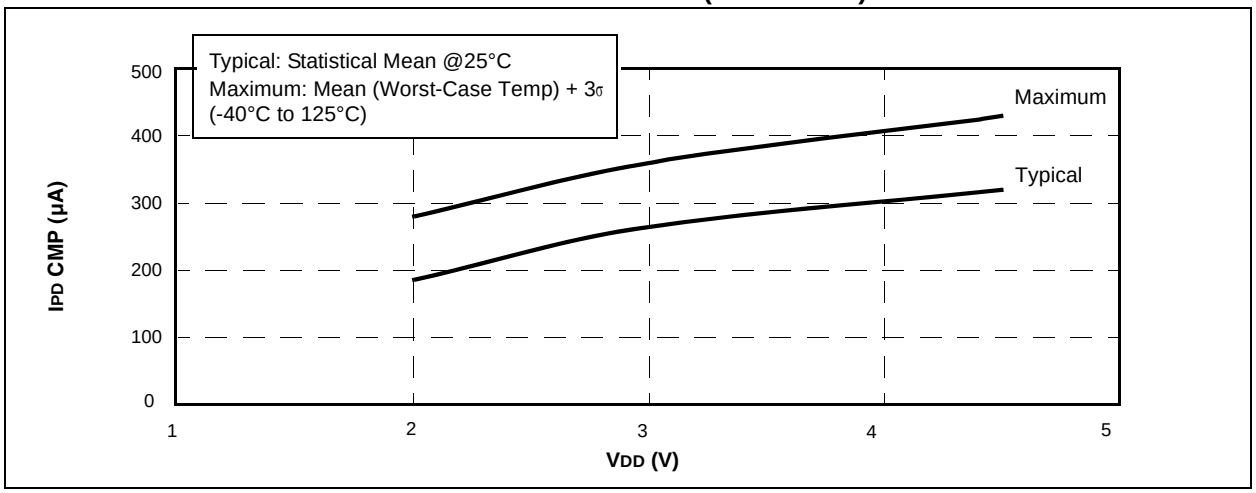


FIGURE 16-49: 0.6V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

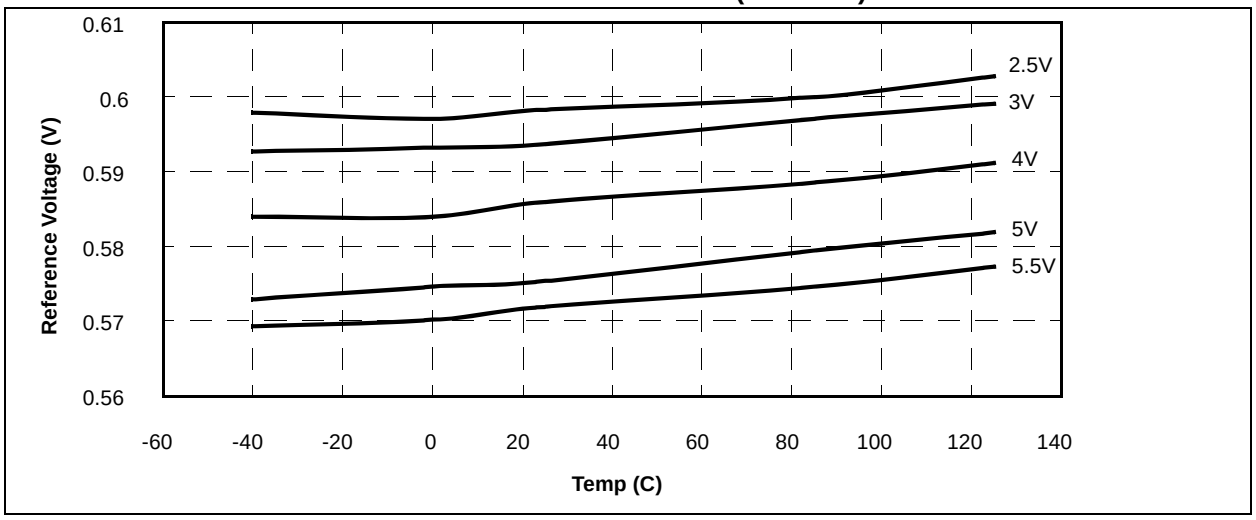


FIGURE 16-50: 1.2V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

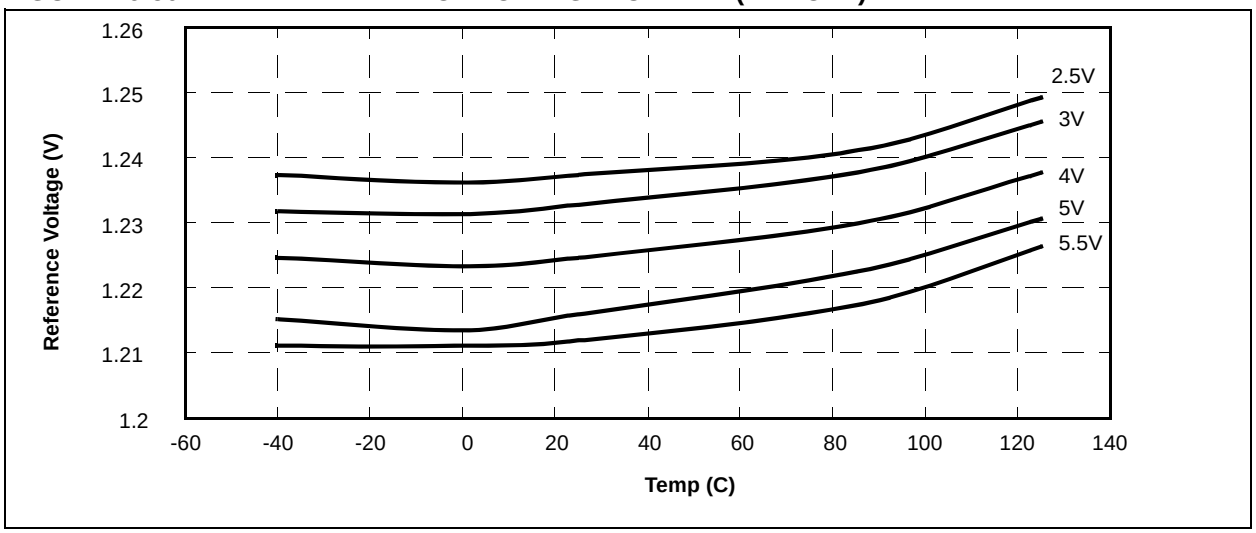


FIGURE 16-51: SHUNT REGULATOR VOLTAGE vs. INPUT CURRENT (TYPICAL)

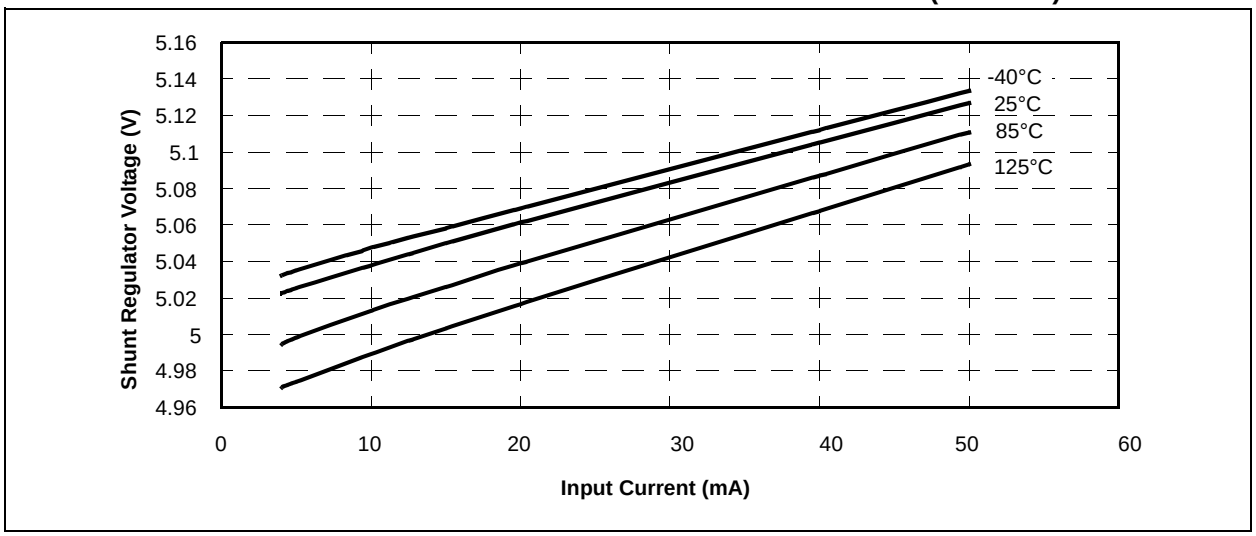


FIGURE 16-52: SHUNT REGULATOR VOLTAGE vs. TEMP (TYPICAL)

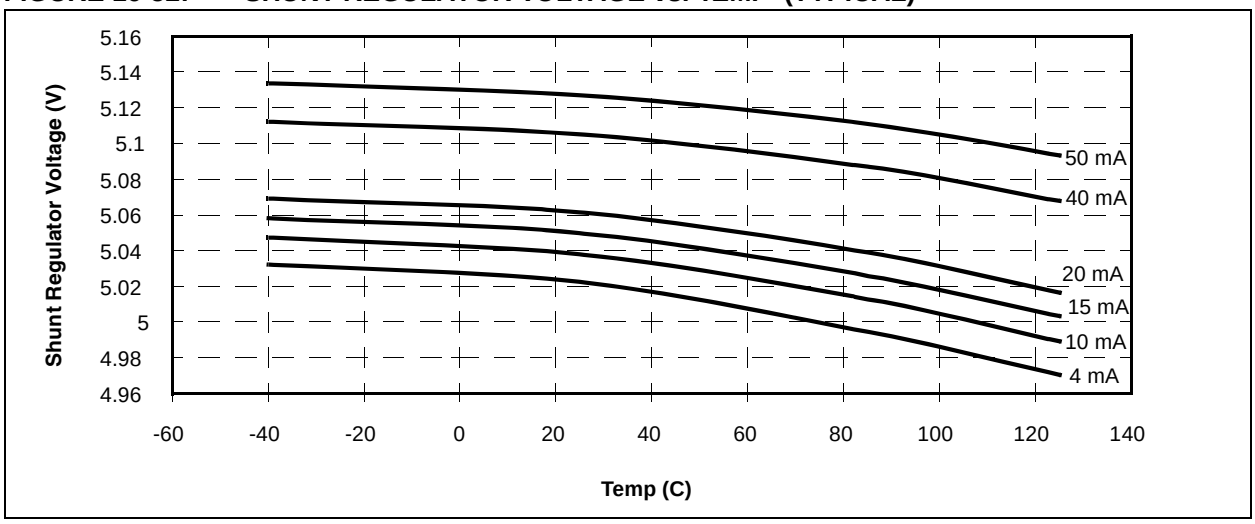
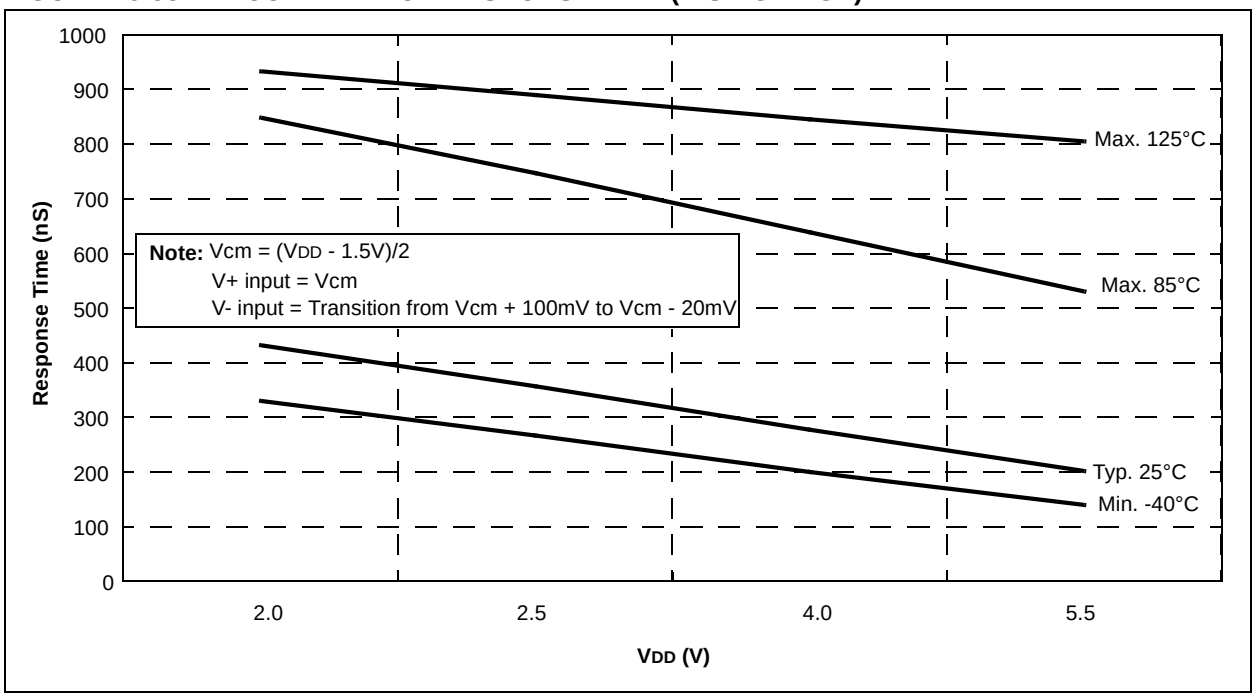


FIGURE 16-53: COMPARATOR RESPONSE TIME (RISING EDGE)



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