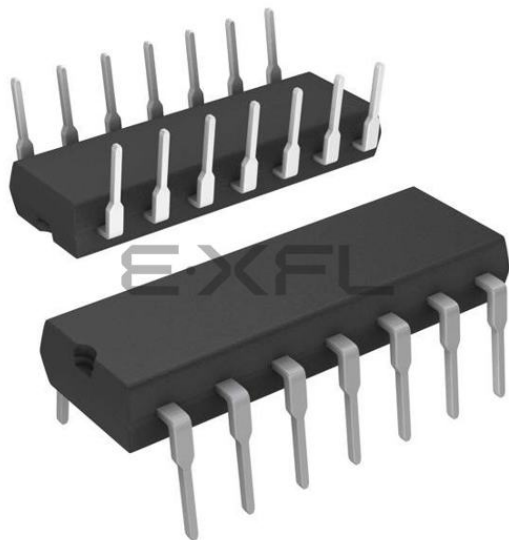




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv616-e-p

PIC16F610/616/16HV610/616

PIC16F610/16HV610 16-Pin Diagram (QFN)

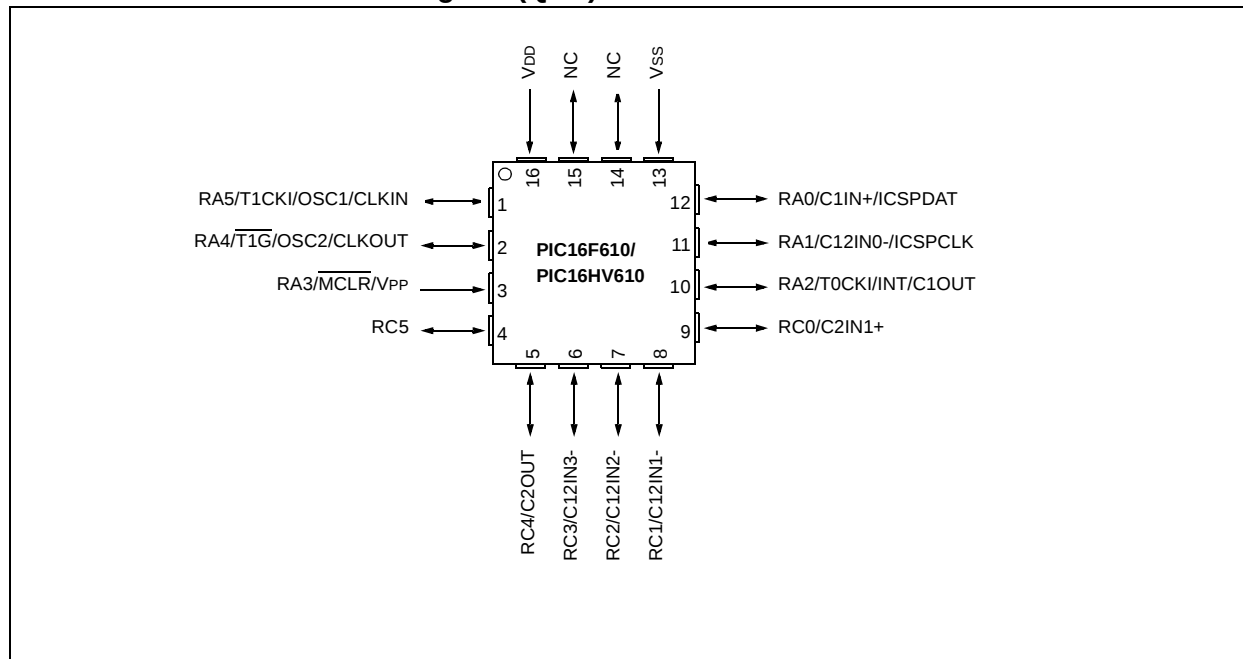


TABLE 3: PIC16F610/16HV610 16-PIN SUMMARY

I/O	Pin	Comparators	Timers	Interrupts	Pull-ups	Basic
RA0	12	C1IN+	—	IOC	Y	ICSPDAT
RA1	11	C12IN0-	—	IOC	Y	ICSPCLK
RA2	10	C1OUT	T0CKI	INT/IOC	Y	—
RA3 ⁽¹⁾	3	—	—	IOC	Y ⁽²⁾	MCLR/VPP
RA4	2	—	T1G	IOC	Y	OSC2/CLKOUT
RA5	1	—	T1CKI	IOC	Y	OSC1/CLKIN
RC0	9	C2IN+	—	—	—	—
RC1	8	C12IN1-	—	—	—	—
RC2	7	C12IN2-	—	—	—	—
RC3	6	C12IN3-	—	—	—	—
RC4	5	C2OUT	—	—	—	—
RC5	4	—	—	—	—	—
—	16	—	—	—	—	VDD
—	13	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

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2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u u1uu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the **Section 13.0 "Instruction Set Summary"**.

Note 1: Bits IRP and RP1 of the STATUS register are not used by the PIC16F610/616/16HV610/616 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **IRP:** This bit is reserved and should be maintained as '0'

bit 6 **RP1:** This bit is reserved and should be maintained as '0'

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)

1 = Bank 1 (80h – FFh)

0 = Bank 0 (00h – 7Fh)

bit 4 **$\overline{\text{TO}}$:** Time-out bit

1 = After power-up, CLRWDt instruction or SLEEP instruction

0 = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$:** Power-down bit

1 = After power-up or by the CLRWDt instruction

0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions), For $\overline{\text{Borrow}}$, the polarity is reversed.

1 = A carry-out from the 4th low-order bit of the result occurred

0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/Borrow bit⁽¹⁾ (ADDWF, ADDLW, SUBLW, SUBWF instructions)

1 = A carry-out from the Most Significant bit of the result occurred

0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

PIC16F610/616/16HV610/616

NOTES:

- a general purpose input
- as Master Clear Reset with weak pull-up
- High Voltage Programming voltage input

--



PIC16F610/616/16HV610/616

9.2 ADC Operation

9.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the analog-to-digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to **Section 9.2.6 "A/D Conversion Procedure"**.

9.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

9.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete analog-to-digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The ECCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not ensure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See **Section 10.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC16F616/16HV616 Only)"** for more information.

9.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an analog-to-digital conversion:

1. Configure Port:
 - Disable pin output driver (See TRIS register)
 - Configure pin as analog
2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Select result format
 - Turn on ADC module
3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
4. Wait the required acquisition time⁽²⁾.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt may be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: See **Section 9.3 "A/D Acquisition Requirements"**.

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REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCS2	ADCS1	ADCS0	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = $F_{osc}/2$

001 = $F_{osc}/8$

010 = $F_{osc}/32$

x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)

100 = $F_{osc}/4$

101 = $F_{osc}/16$

110 = $F_{osc}/64$

bit 3-0 **Unimplemented:** Read as '0'

10.4.2.1 Direction Change in Full-Bridge Mode

In the Full-Bridge mode, the P1M1 bit in the CCP1CON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the P1M1 bit of the CCP1CON register. The following sequence occurs four Timer2 cycles prior to the end of the current PWM period:

- The modulated outputs (P1B and P1D) are placed in their inactive state.
- The associated unmodulated outputs (P1A and P1C) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

See Figure 10-12 for an illustration of this sequence.

The Full-Bridge mode does not provide dead-band delay. As one output is modulated at a time, dead-band delay is generally not required. There is a situation where dead-band delay is required. This situation occurs when both of the following conditions are true:

1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
2. The turn off time of the power switch, including the power device and driver circuit, is greater than the turn on time.

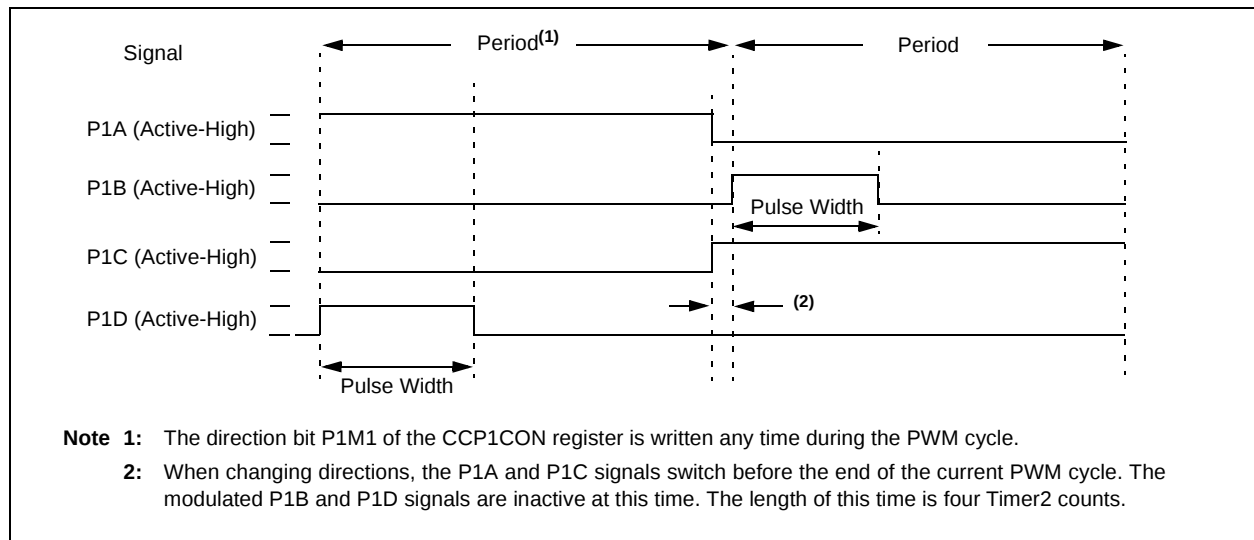
Figure 10-13 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time t1, the output P1A and P1D become inactive, while output P1C becomes active. Since the turn off time of the power devices is longer than the turn on time, a shoot-through current will flow through power devices QC and QD (see Figure 10-10) for the duration of 't'. The same phenomenon will occur to power devices QA and QB for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

1. Reduce PWM duty cycle for one PWM period before changing directions.
2. Use switch drivers that can drive the switches off faster than they can drive them on.

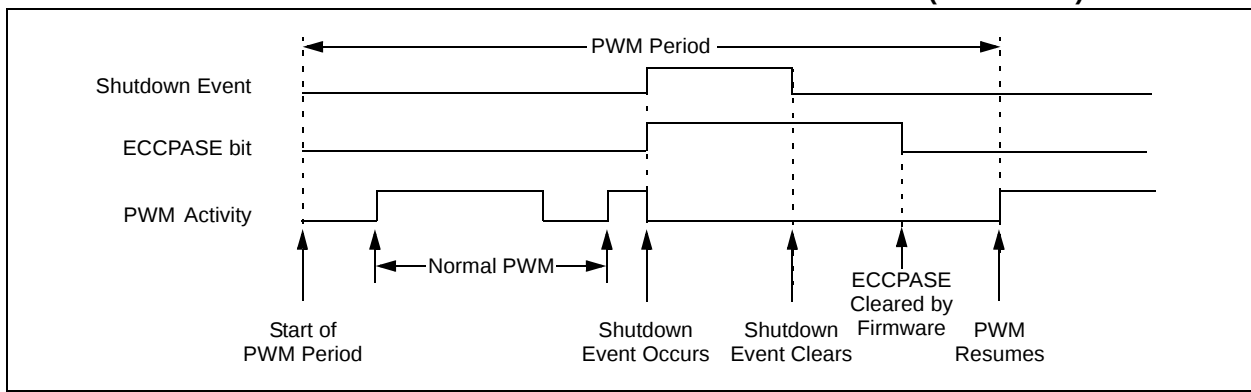
Other options to prevent shoot-through current may exist.

FIGURE 10-12: EXAMPLE OF PWM DIRECTION CHANGE



- Note 1:** The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.
- 2:** Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.
- 3:** Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

FIGURE 10-14: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)

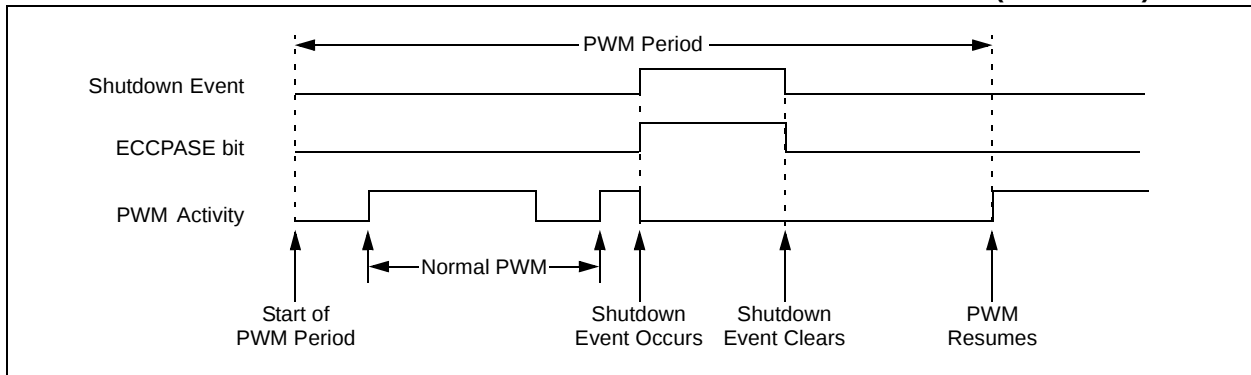


10.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

FIGURE 10-15: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)



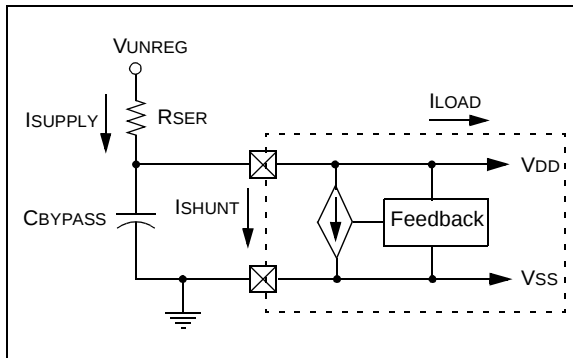
11.0 VOLTAGE REGULATOR

The PIC16HV610/16HV616 include a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (I_{LOAD}).

11.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor R_{SER}. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage V_{UNREG} and the VDD of the microcontroller. See Figure 11-1 for voltage regulator schematic.

FIGURE 11-1: VOLTAGE REGULATOR



An external current limiting resistor, R_{SER}, located between the unregulated supply, V_{UNREG}, and the VDD pin, drops the difference in voltage between V_{UNREG} and VDD. R_{SER} must be between R_{MAX} and R_{MIN} as defined by Equation 11-1.

EQUATION 11-1: R_{SER} LIMITING RESISTOR

$$R_{MAX} = \frac{(V_{UMIN} - 5V)}{1.05 \cdot (4 \text{ mA} + I_{LOAD})}$$

$$R_{MIN} = \frac{(V_{UMAX} - 5V)}{0.95 \cdot (50 \text{ mA})}$$

Where:

R_{MAX} = maximum value of R_{SER} (ohms)

R_{MIN} = minimum value of R_{SER} (ohms)

V_{UMIN} = minimum value of V_{UNREG}

V_{UMAX} = maximum value of V_{UNREG}

VDD = regulated voltage (5V nominal)

I_{LOAD} = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of R_{SER}

0.95 = compensation for -5% tolerance of R_{SER}

11.2 Regulator Considerations

The supply voltage V_{UNREG} and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for R_{SER} must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC16HV610/16HV616 devices.

PIC16F610/616/16HV610/616

RETFIE	Return from Interrupt
Syntax:	[<i>label</i>] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	RETFIE After Interrupt PC = TOS GIE = 1

RETLW	Return with literal in W
Syntax:	[<i>label</i>] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	CALL TABLE;W contains ;table offset ;value GOTO DONE • • ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • RETLW kn ;End of table DONE Before Instruction W = 0x07 After Instruction W = value of k8

RETURN	Return from Subroutine
Syntax:	[<i>label</i>] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

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15.9 DC Characteristics: PIC16F610/616/16HV610/616- I (Industrial) PIC16F610/616/16HV610/616 - E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature				
			-40°C ≤ TA ≤ +85°C for industrial				
			-40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D101*	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	
Program Flash Memory							
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

15.10 Thermal Considerations

Standard Operating Conditions (unless otherwise stated)					
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
Param No.	Sym	Characteristic	Typ	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	70*	C/W	14-pin PDIP package
			85.0*	C/W	14-pin SOIC package
			100*	C/W	14-pin TSSOP package
			37*	C/W	16-pin QFN 4x4mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	32.5*	C/W	14-pin PDIP package
			31.0*	C/W	14-pin SOIC package
			31.7*	C/W	14-pin TSSOP package
			2.6*	C/W	16-pin QFN 4x4mm package
TH03	T_{DIE}	Die Temperature	150*	C	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ (NOTE 1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \sum (I_{OL} \times V_{OL}) + \sum (I_{OH} \times (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = P_{D_{MAX}} (T_{DIE} - T_A) / \theta_{JA}$ (NOTE 2)

* These parameters are characterized but not tested.

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature.

PIC16F610/616/16HV610/616

FIGURE 15-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

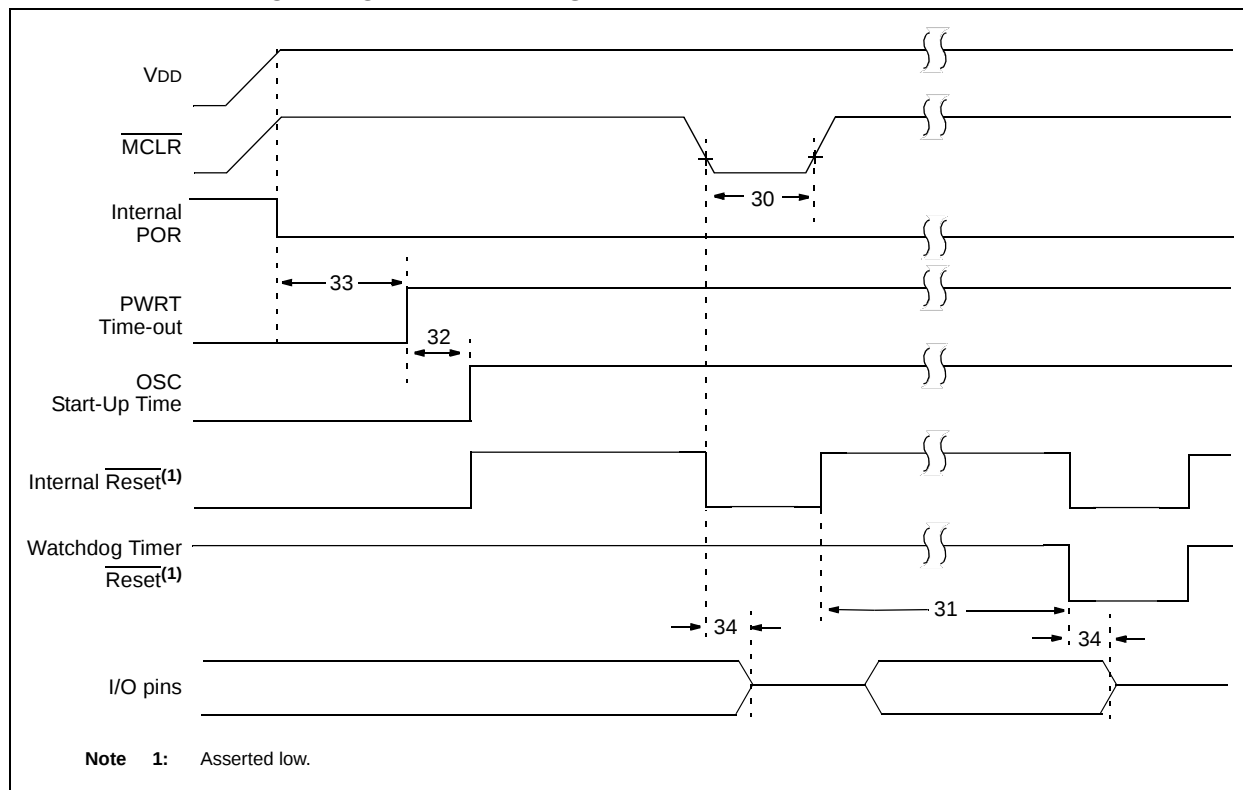
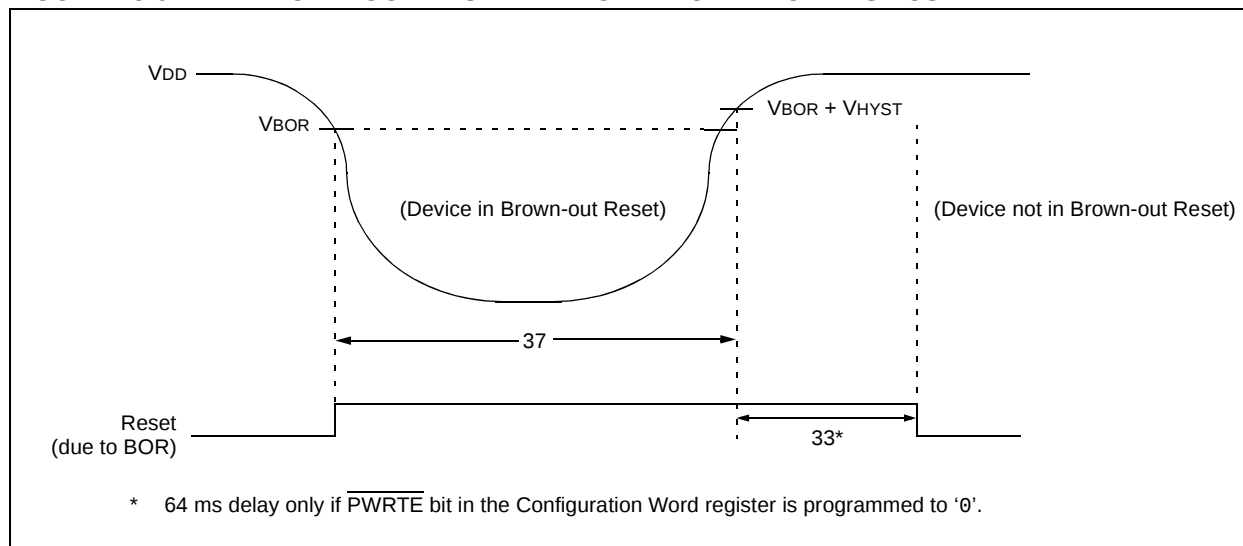


FIGURE 15-9: BROWN-OUT RESET TIMING AND CHARACTERISTICS



PIC16F610/616/16HV610/616

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	$V_{DD} = 5\text{V}$, -40°C to $+85^{\circ}\text{C}$
			5	—	—	μs	$V_{DD} = 5\text{V}$, -40°C to $+125^{\circ}\text{C}$
31*	TWD _T	Watchdog Timer Time-out Period (No Prescaler)	10	20	30	ms	$V_{DD} = 5\text{V}$, -40°C to $+85^{\circ}\text{C}$
			10	20	35	ms	$V_{DD} = 5\text{V}$, -40°C to $+125^{\circ}\text{C}$
32	TOST	Oscillation Start-up Timer Period ^(1, 2)	—	1024	—	T _{OSC}	(NOTE 3)
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
35*	VBOR	Brown-out Reset Voltage	2.0	2.15	2.3	V	(NOTE 4)
36*	VHYS _T	Brown-out Reset Hysteresis	—	100	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	μs	$V_{DD} \leq V_{BOR}$

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (T_{CY}) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

PIC16F610/616/16HV610/616

FIGURE 16-26: PIC16HV610/616 I_{DD} EXTRC (4 MHz) vs. V_{DD}

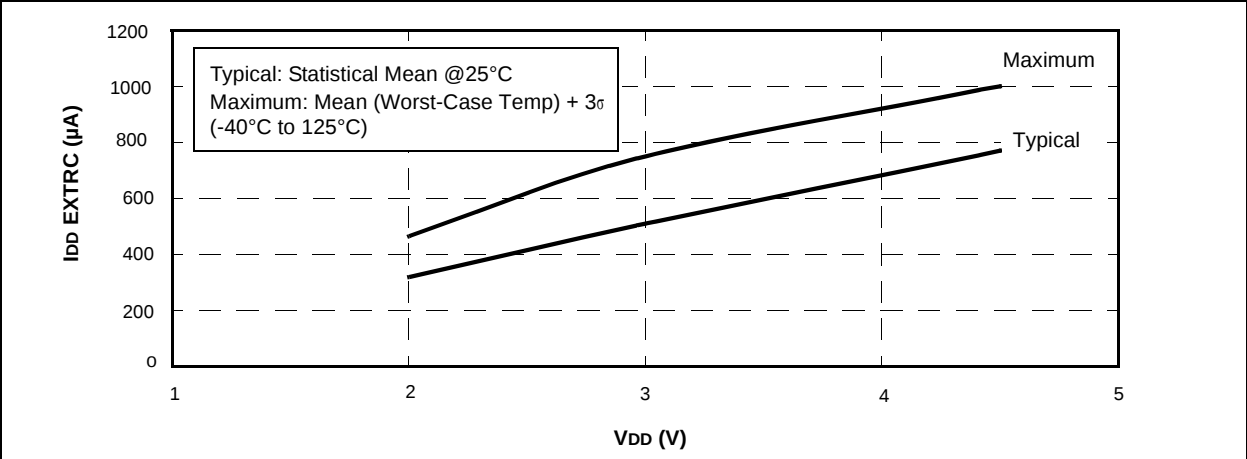


FIGURE 16-27: PIC16HV610/616 I_{PD} BASE vs. V_{DD}

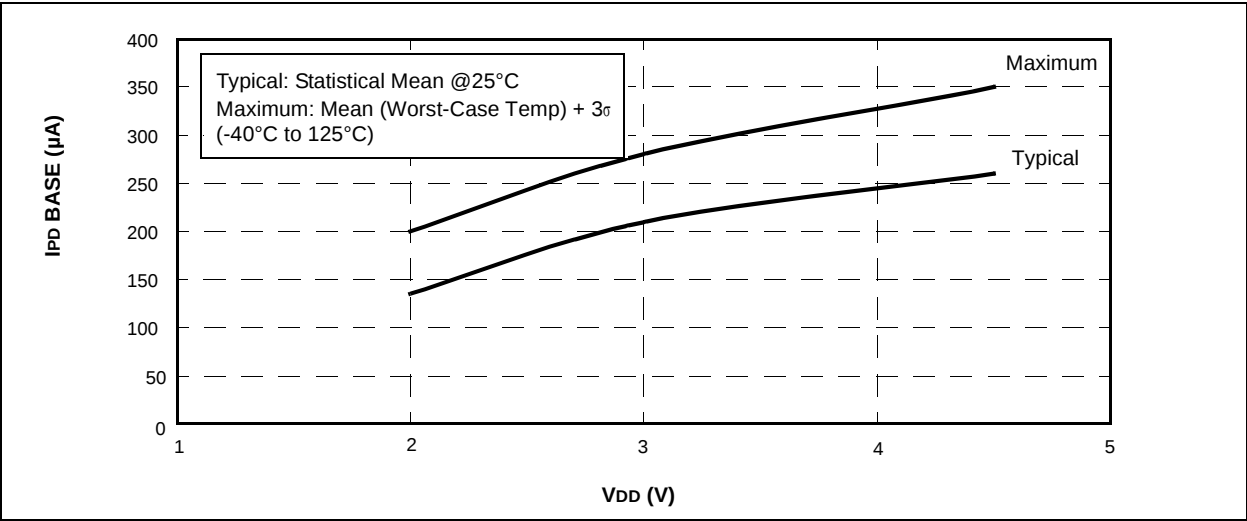
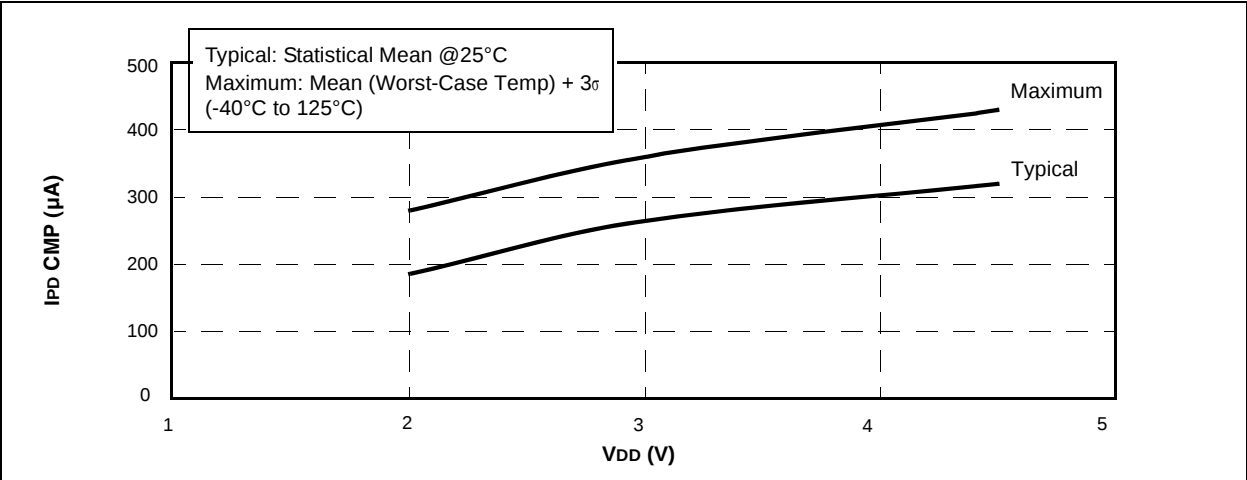


FIGURE 16-28: PIC16HV610/616 I_{PD} COMPARATOR (SINGLE ON) vs. V_{DD}



PIC16F610/616/16HV610/616

FIGURE 16-41: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

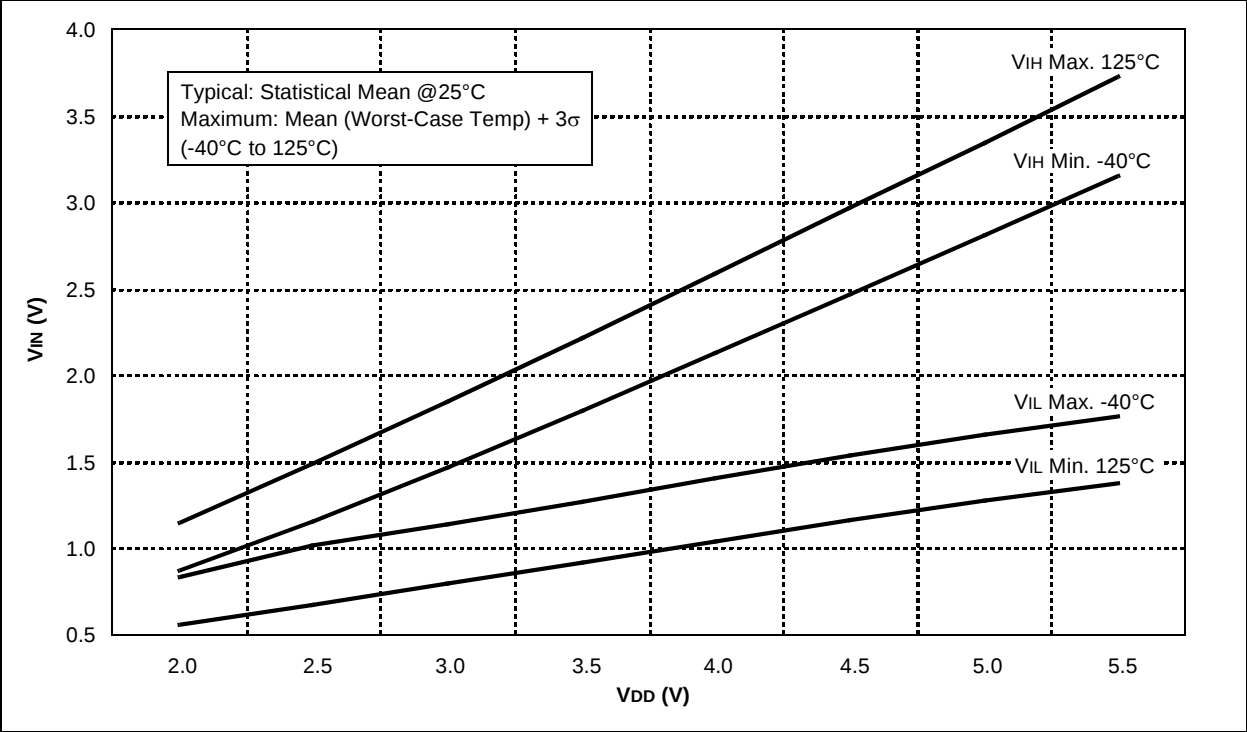


FIGURE 16-42: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

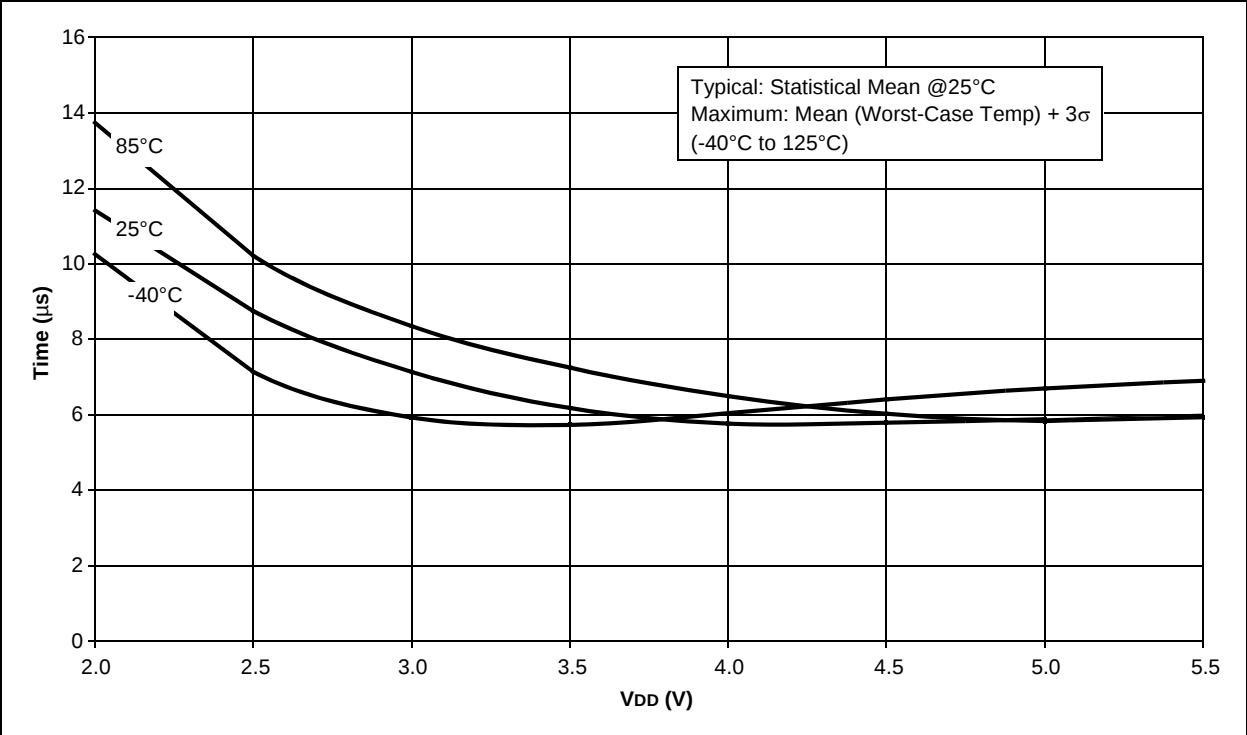


FIGURE 16-52: SHUNT REGULATOR VOLTAGE vs. TEMP (TYPICAL)

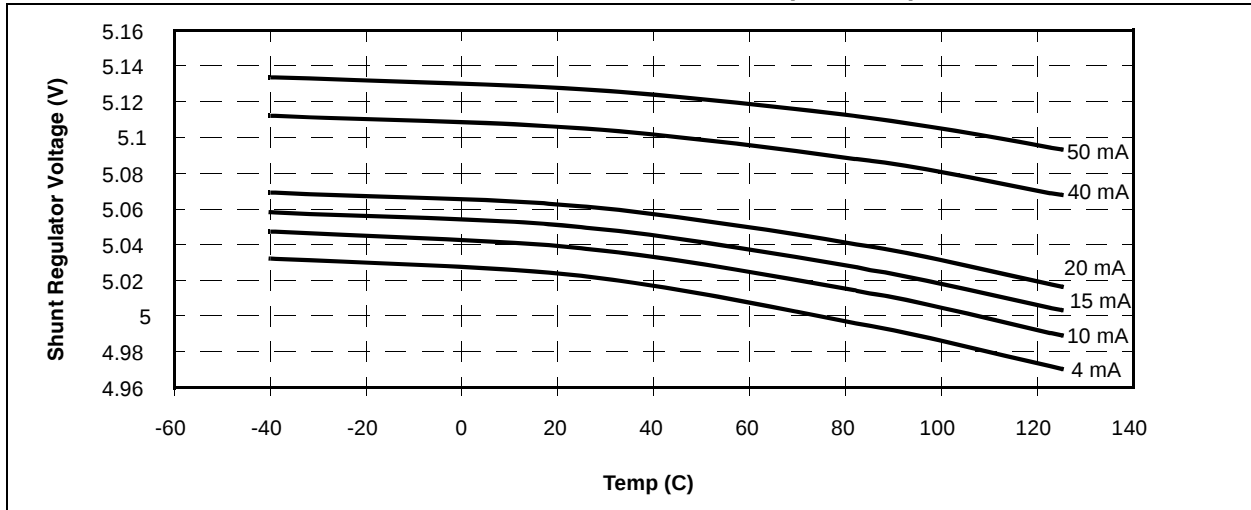
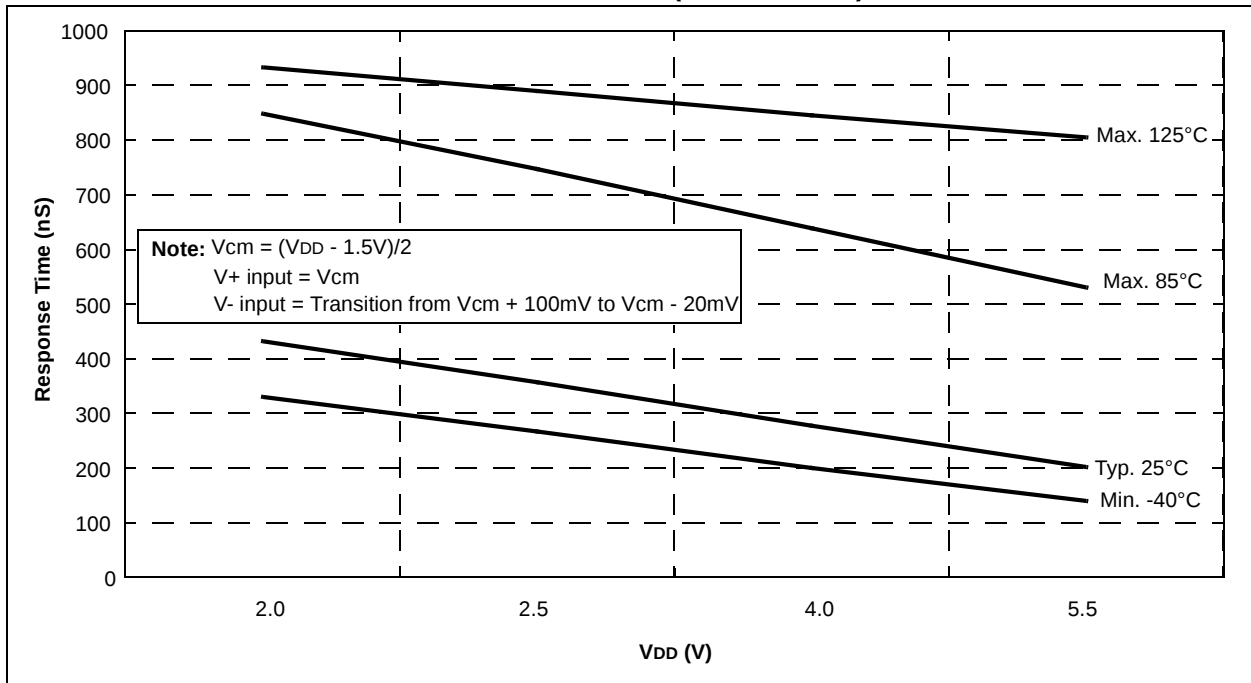


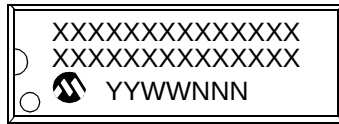
FIGURE 16-53: COMPARATOR RESPONSE TIME (RISING EDGE)



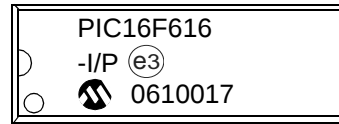
17.0 PACKAGING INFORMATION

17.1 Package Marking Information

14-Lead PDIP



Example



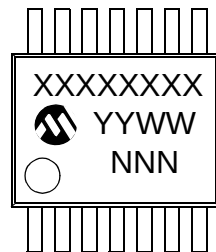
14-Lead SOIC (.150")



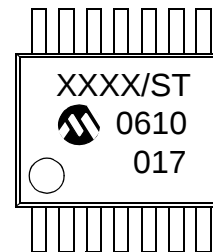
Example



14-Lead TSSOP



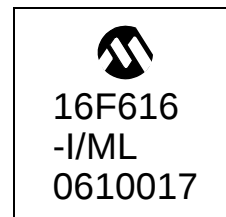
Example



16-Lead QFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

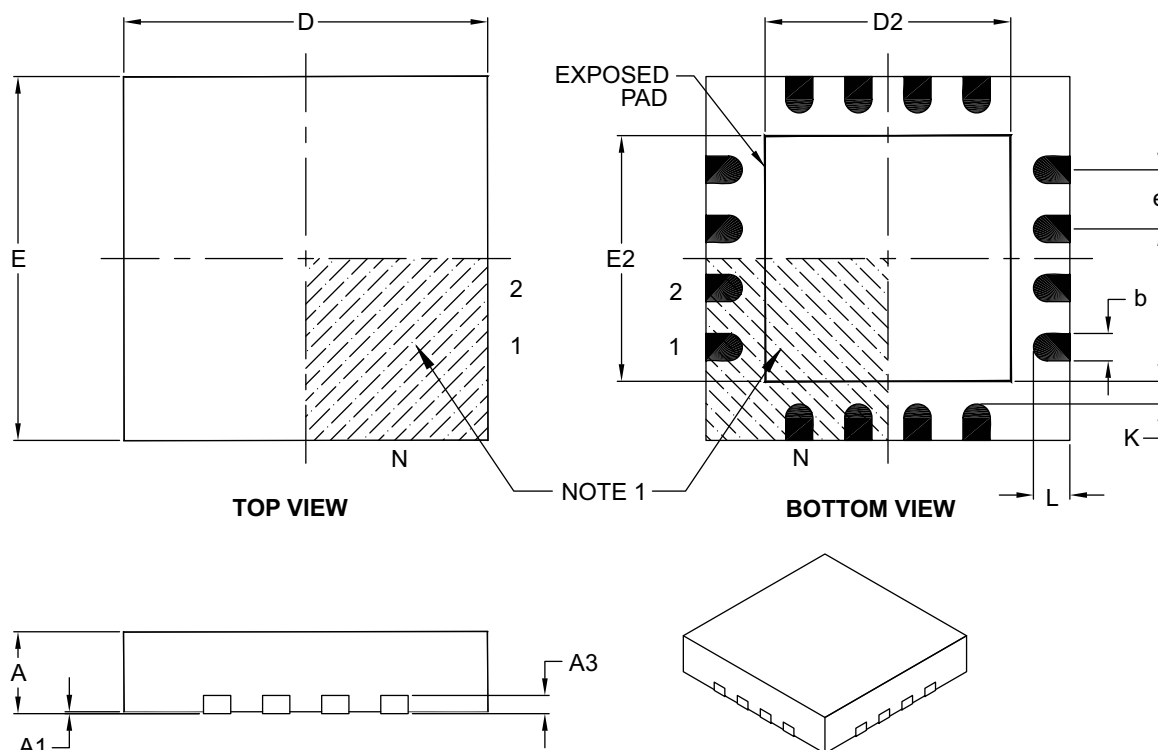
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

- * Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC® device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC16F610/616/16HV610/616

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	16		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

PIC16F610/616/16HV610/616

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4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?
