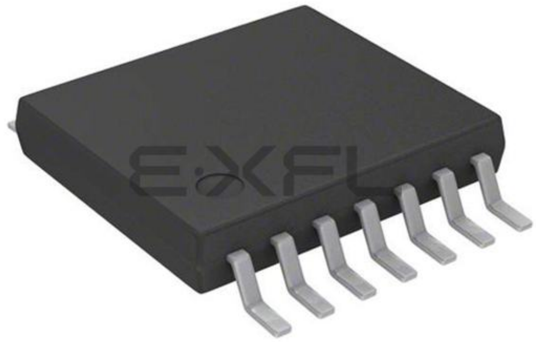

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	11
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16hv616-e-st

TABLE 1-2: PIC16F616/16HV616 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT	RA0	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	C1IN+	AN	—	Comparator C1 non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
RA1/AN1/C12IN0-/V_{REF}/ICSPCLK	RA1	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	C12IN0-	AN	—	Comparators C1 and C2 inverting input
	V_{REF}	AN	—	External Voltage Reference for A/D
	ICSPCLK	ST	—	Serial Programming Clock
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator C1 output
RA3/$\overline{MCLR}$/V_{PP}	RA3	TTL	—	PORTA input with interrupt-on-change
	$\overline{MCLR}$	ST	—	Master Clear w/internal pull-up
	V_{PP}	HV	—	Programming voltage
RA4/AN3/$\overline{T1G}$/OSC2/CLKOUT	RA4	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	$\overline{T1G}$	ST	—	Timer1 gate (count enable)
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	F_{OSC}/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock input
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RC0/AN4/C2IN+	RC0	TTL	CMOS	PORTC I/O
	AN4	AN	—	A/D Channel 4 input
	C2IN+	AN	—	Comparator C2 non-inverting input
RC1/AN5/C12IN1-	RC1	TTL	CMOS	PORTC I/O
	AN5	AN	—	A/D Channel 5 input
	C12IN1-	AN	—	Comparators C1 and C2 inverting input
RC2/AN6/C12IN2-/P1D	RC2	TTL	CMOS	PORTC I/O
	AN6	AN	—	A/D Channel 6 input
	C12IN2-	AN	—	Comparators C1 and C2 inverting input
	P1D	—	CMOS	PWM output
RC3/AN7/C12IN3-/P1C	RC3	TTL	CMOS	PORTC I/O
	AN7	AN	—	A/D Channel 7 input
	C12IN3-	AN	—	Comparators C1 and C2 inverting input
	P1C	—	CMOS	PWM output
RC4/C2OUT/P1B	RC4	TTL	CMOS	PORTC I/O
	C2OUT	—	CMOS	Comparator C2 output
	P1B	—	CMOS	PWM output
RC5/CCP1/P1A	RC5	TTL	CMOS	PORTC I/O
	CCP1	ST	CMOS	Capture input/Compare output
	P1A	—	CMOS	PWM output
V_{DD}	V_{DD}	Power	—	Positive supply
V_{SS}	V_{SS}	Power	—	Ground reference

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; HV = High Voltage; ST = Schmitt Trigger input with CMOS levels; TTL = TTL compatible input; XTAL = Crystal

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F610/616/16HV610/616 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-3FF) for the PIC16F610/16HV610 and the first 2K x 14 (0000h-07FFh) for the PIC16F616/16HV616 is physically implemented. Accessing a location above these boundaries will cause a wraparound within the first 1K x 14 space (PIC16F610/16HV610) and 2K x 14 space (PIC16F616/16HV616). The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F610/16HV610

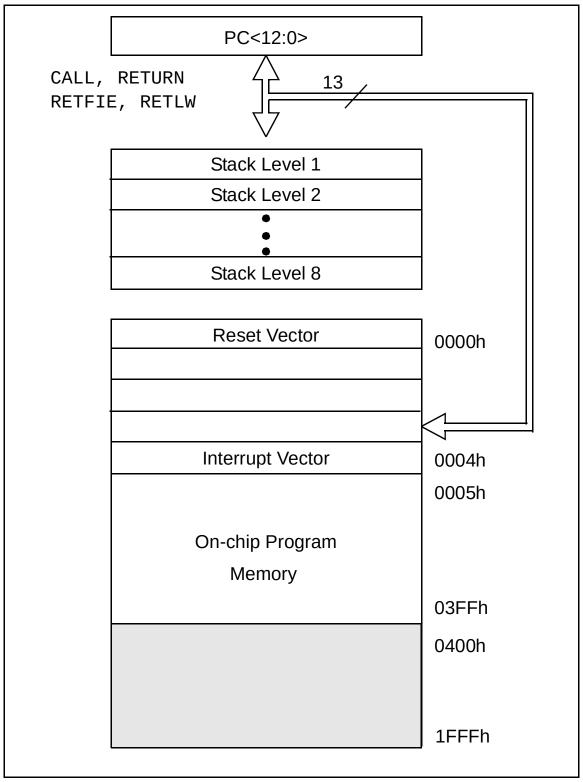


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F616/16HV616

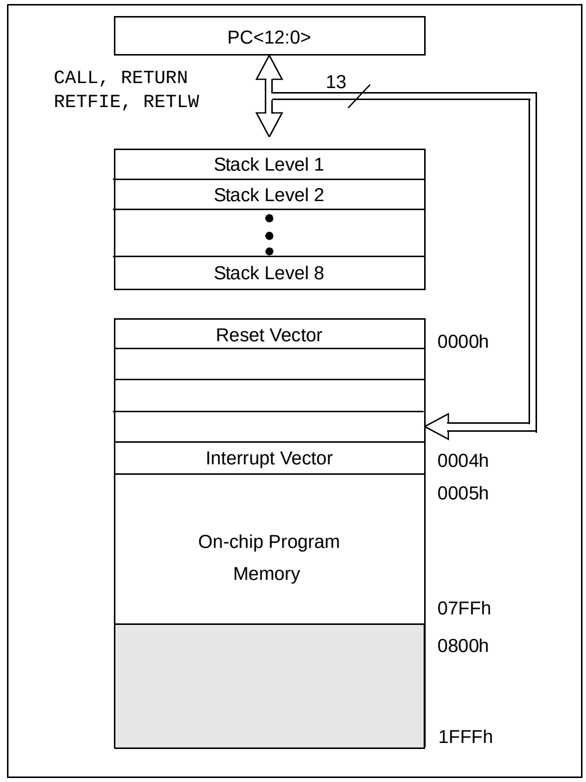


FIGURE 2-3: DATA MEMORY MAP OF THE PIC16F610/16HV610

Bank 0	File Address	Bank 1	File Address
Indirect Addr.(1)	00h	Indirect Addr.(1)	80h
TMR0	01h	OPTION_REG	81h
PCL	02h	PCL	82h
STATUS	03h	STATUS	83h
FSR	04h	FSR	84h
PORTA	05h	TRISA	85h
	06h		86h
PORTC	07h	TRISC	87h
	08h		88h
	09h		89h
PCLATH	0Ah	PCLATH	8Ah
INTCON	0Bh	INTCON	8Bh
PIR1	0Ch	PIE1	8Ch
	0Dh		8Dh
TMR1L	0Eh	PCON	8Eh
TMR1H	0Fh		8Fh
T1CON	10h	OSCTUNE	90h
	11h	ANSEL	91h
	12h		92h
	13h		93h
	14h		94h
	15h	WPUA	95h
	16h	IOCA	96h
	17h		97h
	18h		98h
VRCON	19h	SRCON0	99h
CM1CON0	1Ah	SRCON1	9Ah
CM2CON0	1Bh		9Bh
CM2CON1	1Ch		9Ch
	1Dh		9Dh
	1Eh		9Eh
	1Fh		9Fh
	20h–3Fh		A0h–EFh
General Purpose Registers 64 Bytes	40h–6Fh		
Accesses 70h-7Fh	70h–7Fh	Accesses 70h-7Fh	F0h–FFh

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

FIGURE 2-4: DATA MEMORY MAP OF THE PIC16F616/16HV616

Bank 0	File Address	Bank 1	File Address
Indirect Addr.(1)	00h	Indirect Addr.(1)	80h
TMR0	01h	OPTION_REG	81h
PCL	02h	PCL	82h
STATUS	03h	STATUS	83h
FSR	04h	FSR	84h
PORTA	05h	TRISA	85h
	06h		86h
PORTC	07h	TRISC	87h
	08h		88h
	09h		89h
PCLATH	0Ah	PCLATH	8Ah
INTCON	0Bh	INTCON	8Bh
PIR1	0Ch	PIE1	8Ch
	0Dh		8Dh
TMR1L	0Eh	PCON	8Eh
TMR1H	0Fh		8Fh
T1CON	10h	OSCTUNE	90h
TMR2	11h	ANSEL	91h
T2CON	12h	PR2	92h
CCPR1L	13h		93h
CCPR1H	14h		94h
CCP1CON	15h	WPUA	95h
PWM1CON	16h	IOCA	96h
ECCPAS	17h		97h
	18h		98h
VRCON	19h	SRCON0	99h
CM1CON0	1Ah	SRCON1	9Ah
CM2CON0	1Bh		9Bh
CM2CON1	1Ch		9Ch
	1Dh		9Dh
ADRESH	1Eh	ADRESL	9Eh
ADCON0	1Fh	ADCON1	9Fh
General Purpose Registers 96 Bytes	20h–7Fh	General Purpose Registers 32 Bytes	A0h–BFh
			C0h–EFh
		Accesses 70h-7Fh	F0h–FFh

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

REGISTER 4-4: WPUA: WEAK PULL-UP PORTA REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-4 **WPUA<5:4>:** Weak Pull-up Control bits
1 = Pull-up enabled
0 = Pull-up disabled

bit 3 **Unimplemented**: Read as ‘0’

bit 2-0 **WPUA<2:0>:** Weak Pull-up Control bits
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).
3: The RA3 pull-up is enabled when configured as $\overline{\text{MCLR}}$ and disabled as an input in the Configuration Word.
4: WPUA<5:4> always reads ‘1’ in XT, HS and LP Oscillator modes.

REGISTER 4-5: IOCA: INTERRUPT-ON-CHANGE PORTA REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOCA<5:0>:** Interrupt-on-change PORTA Control bit
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note 1: Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.
2: IOCA<5:4> always reads ‘1’ in XT, HS and LP Oscillator modes.

4.3 PORTC and the TRISC Registers

PORTC is a general purpose I/O port consisting of 6 bidirectional pins. The pins can be configured for either digital I/O or analog input to A/D Converter (ADC) or Comparator. For specific information about individual functions such as the Enhanced CCP or the ADC, refer to the appropriate section in this data sheet.

> **Note:** The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

EXAMPLE 4-2: INITIALIZING PORTC

```
BCF     STATUS,RP0     ;Bank 0
CLRF    PORTC          ;Init PORTC
BSF     STATUS,RP0     ;Bank 1
CLRF    ANSEL          ;digital I/O
MOVLW   0Ch            ;Set RC<3:2> as inputs
MOVWF   TRISC          ;and set RC<5:4,1:0>
                       ;as outputs
BCF     STATUS,RP0     ;Bank 0
```

REGISTER 4-6: PORTC: PORTC REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-0	R/W-0	R/W-x	R/W-x
—	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **RC<5:0>**: PORTC I/O Pin bit
1 = PORTC pin is > V_{IH}
0 = PORTC pin is < V_{IL}

REGISTER 4-7: TRISC: PORTC TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **TRISC<5:0>:** PORTC Tri-State Control bit
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or $\overline{\text{T1G}}$ pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with ECCP)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

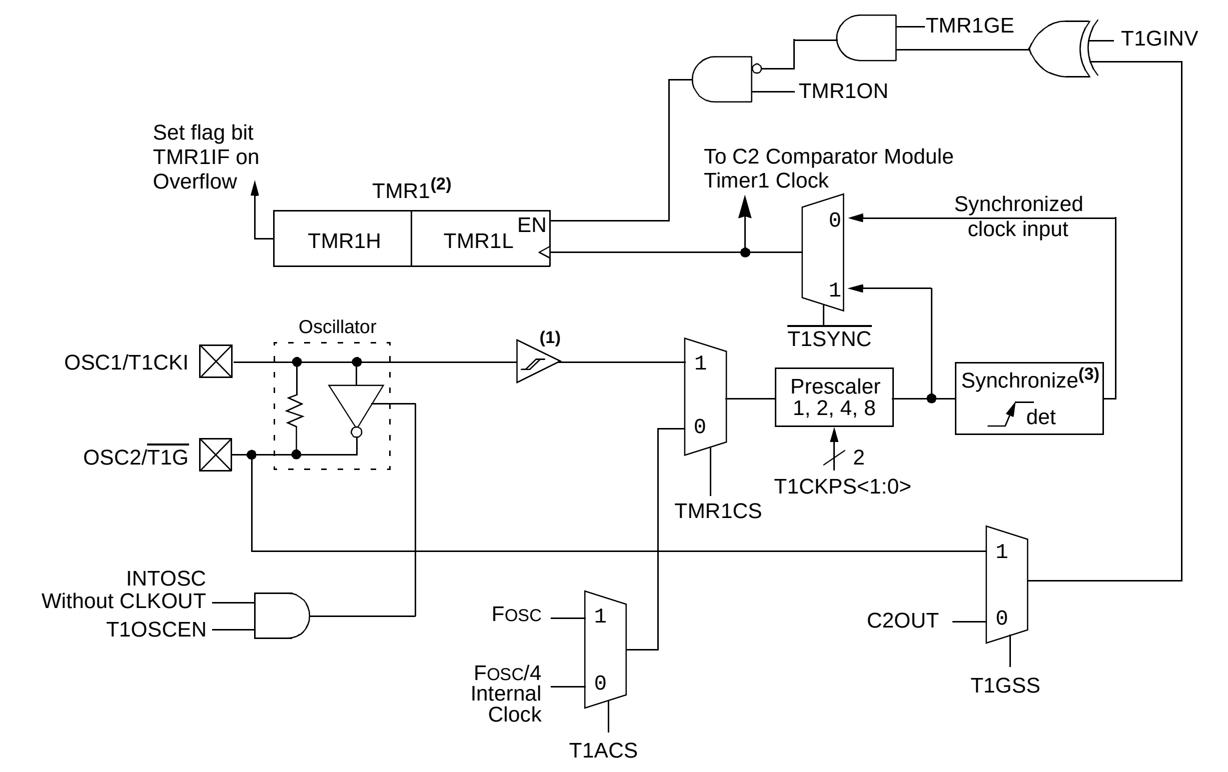
When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is FOSC/4. When TMR1CS = 1, the clock source is supplied externally.

Clock Source	TMR1CS	T1ACS
FOSC/4	0	0
FOSC	0	1
T1CKI pin	1	x

FIGURE 6-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is low power type when using LP osc, or high speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.

REGISTER 8-1: CM1CON0: COMPARATOR 1 CONTROL REGISTER 0

R/W-0	R-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **C1ON:** Comparator C1 Enable bit
1 = Comparator C1 is enabled
0 = Comparator C1 is disabled

bit 6 **C1OUT:** Comparator C1 Output bit
If C1POL = 1 (inverted polarity):
C1OUT = 0 when C1VIN+ > C1VIN-
C1OUT = 1 when C1VIN+ < C1VIN-
If C1POL = 0 (non-inverted polarity):
C1OUT = 1 when C1VIN+ > C1VIN-
C1OUT = 0 when C1VIN+ < C1VIN-

bit 5 **C1OE:** Comparator C1 Output Enable bit
1 = C1OUT is present on the C1OUT pin(1)
0 = C1OUT is internal only

bit 4 **C1POL:** Comparator C1 Output Polarity Select bit
1 = C1OUT logic is inverted
0 = C1OUT logic is not inverted

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **C1R:** Comparator C1 Reference Select bit (non-inverting input)
1 = C1VIN+ connects to C1VREF output
0 = C1VIN+ connects to C1IN+ pin

bit 1-0 **C1CH<1:0>:** Comparator C1 Channel Select bit
00 = C12IN0- pin of C1 connects to C1VIN-
01 = C12IN1- pin of C1 connects to C1VIN-
10 = C12IN2- pin of C1 connects to C1VIN-
11 = C12IN3- pin of C1 connects to C1VIN-

Note 1: Comparator output requires the following three conditions: C1OE = 1, C1ON = 1 and corresponding port TRIS bit = 0.

10.4.4 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the ECCPASx bits of the ECCPAS register. A shutdown event may be generated by:

- A logic '0' on the INT pin
- Comparator C1
- Comparator C2
- Setting the ECCPASE bit in firmware

A shutdown condition is indicated by the ECCPASE (Auto-Shutdown Event Status) bit of the ECCPAS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The ECCPASE bit is set to '1'. The ECCPASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 10.4.5 "Auto-Restart Mode"**).

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [P1A/P1C] and [P1B/P1D]. The state of each pin pair is determined by the PSSAC and PSSBD bits of the ECCPAS register. Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

REGISTER 10-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ECCPASE:** ECCP Auto-Shutdown Event Status bit
1 = A shutdown event has occurred; ECCP outputs are in shutdown state
0 = ECCP outputs are operating

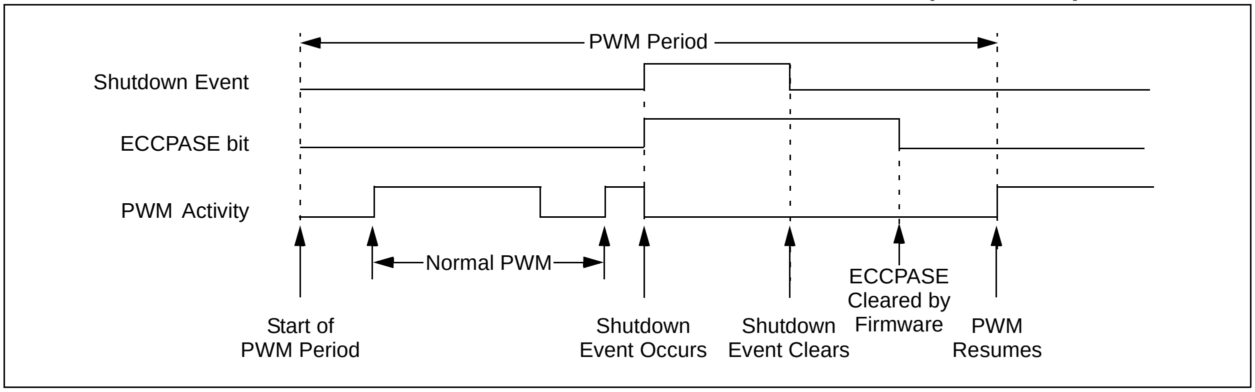
bit 6-4 **ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits
000 = Auto-Shutdown is disabled
001 = Comparator C1 output high
010 = Comparator C2 output high(1)
011 = Either Comparators output is high
100 = V_{IL} on INT pin
101 = V_{IL} on INT pin or Comparator C1 output high
110 = V_{IL} on INT pin or Comparator C2 output high
111 = V_{IL} on INT pin or either Comparators output is high

bit 3-2 **PSSACn:** Pins P1A and P1C Shutdown State Control bits
00 = Drive pins P1A and P1C to '0'
01 = Drive pins P1A and P1C to '1'
1x = Pins P1A and P1C tri-state

bit 1-0 **PSSBDn:** Pins P1B and P1D Shutdown State Control bits
00 = Drive pins P1B and P1D to '0'
01 = Drive pins P1B and P1D to '1'
1x = Pins P1B and P1D tri-state

> **Note 1:** The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.
>
> **2:** Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.
>
> **3:** Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

FIGURE 10-14: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)

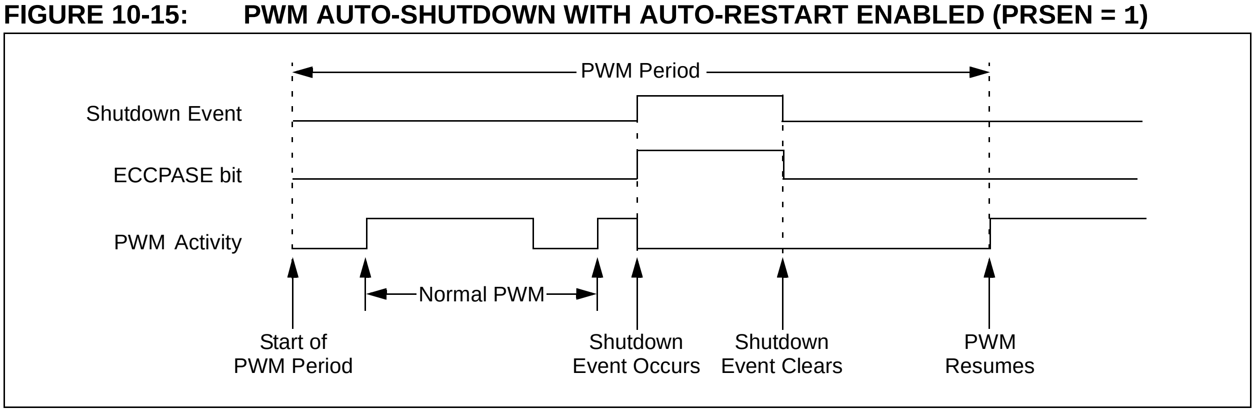


10.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

FIGURE 10-15: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)



REGISTER 10-3: PWM1CON: ENHANCED PWM CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **PRSEN:** PWM Restart Enable bit
1 = Upon auto-shutdown, the ECCPASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically
0 = Upon auto-shutdown, ECCPASE must be cleared in software to restart the PWM

bit 6-0 **PDC<6:0>:** PWM Delay Count bits
PDCn = Number of FOSC/4 (4 * TOSC) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it transitions active

TABLE 10-7: SUMMARY OF REGISTERS ASSOCIATED WITH PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON(1)	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
CCPR1L(1)	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
CCPR1H(1)	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0	0000 -000	0000 -000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	0000 -000	0000 -000
CM2CON1	MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC	00-0 0010	00-0 0010
ECCPAS(1)	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000	0000 0000
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	C2IE	C1IE	—	TMR2IE(1)	TMR1IE	-000 0-00	0000 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	C2IF	C1IF	—	TMR2IF(1)	TMR1IF	-000 0-00	0000 0-00
PWM1CON(1)	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000	0000 0000
T2CON(1)	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR2(1)	Timer2 Module Register								0000 0000	0000 0000
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.
Note 1: PIC16F616/16HV616 only.

14.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

14.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

14.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

14.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

15.4 DC Characteristics: PIC16F610/616- I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Device Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
						VDD	**Note**
D020	**Power-down Base Current(IPD)(2)**	—	0.05	0.9	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	1.2	μA	3.0	
	PIC16F610/616	—	0.35	1.5	μA	5.0	
		—	150	500	nA	3.0	-40°C ≤ TA ≤ +25°C for industrial
D021		—	0.5	1.5	μA	2.0	WDT Current(1)
		—	2.5	4.0	μA	3.0	
		—	9.5	17	μA	5.0	
D022		—	5.0	9	μA	3.0	BOR Current(1)
		—	6.0	12	μA	5.0	
D023		—	105	115	μA	2.0	Comparator Current(1), both comparators enabled
		—	110	125	μA	3.0	
		—	116	140	μA	5.0	
D024		—	50	60	μA	2.0	Comparator Current(1), single comparator enabled
		—	55	65	μA	3.0	
		—	60	75	μA	5.0	
D025		—	30	40	μA	2.0	CVREF Current(1) (high range)
		—	45	60	μA	3.0	
		—	75	105	μA	5.0	
D026*		—	39	50	μA	2.0	CVREF Current(1) (low range)
		—	59	80	μA	3.0	
		—	98	130	μA	5.0	
D027		—	5.5	10	μA	2.0	T1OSC Current(1), 32.768 kHz
		—	7.0	12	μA	3.0	
		—	8.5	14	μA	5.0	
D028		—	0.2	1.6	μA	3.0	A/D Current(1), no conversion in progress.
		—	0.36	1.9	μA	5.0	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

15.6 DC Characteristics: PIC16HV610/616- I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions: VDD	Conditions: Note
D020	**Power-down Base Current(IPD)[2,3]**	—	135	200	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	210	280	μA	3.0	
	PIC16HV610/616	—	260	350	μA	4.5	
D021		—	135	200	μA	2.0	WDT Current[1]
		—	210	285	μA	3.0	
		—	265	360	μA	4.5	
D022		—	215	285	μA	3.0	BOR Current[1]
		—	265	360	μA	4.5	
D023		—	240	340	μA	2.0	Comparator Current[1], both comparators enabled
		—	320	420	μA	3.0	
		—	370	500	μA	4.5	
D024		—	185	270	μA	2.0	Comparator Current[1], single comparator enabled
		—	265	350	μA	3.0	
		—	320	430	μA	4.5	
D025		—	165	235	μA	2.0	CVREF Current[1] (high range)
		—	255	330	μA	3.0	
		—	330	430	μA	4.5	
D026*		—	175	245	μA	2.0	CVREF Current[1] (low range)
		—	275	350	μA	3.0	
		—	355	450	μA	4.5	
D027		—	140	205	μA	2.0	T1OSC Current[1], 32.768 kHz
		—	220	290	μA	3.0	
		—	270	360	μA	4.5	
D028		—	210	280	μA	3.0	A/D Current[1], no conversion in progress
		—	260	350	μA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: Shunt regulator is always enabled and always draws operating current.

TABLE 15-10: SHUNT REGULATOR SPECIFICATIONS (PIC16HV610/616 only)

SHUNT REGULATOR CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
SR01	V_{SHUNT}	Shunt Voltage	4.75	5	5.4	V	
SR02	I_{SHUNT}	Shunt Current	4	—	50	mA	
SR03*	T_{SETTLE}	Settling Time	—	—	150	ns	To 1% of final value
SR04	C_{LOAD}	Load Capacitance	0.01	—	10	μF	Bypass capacitor on VDD pin
SR05	ΔI_{SNT}	Regulator operating current	—	180	—	μA	Includes band gap reference current

* These parameters are characterized but not tested.

TABLE 15-11: PIC16F616/16HV616 A/D CONVERTER (ADC) CHARACTERISTICS:

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AD01	N_R	Resolution	—	—	10 bits	bit	
AD02	E_{IL}	Integral Error	—	—	±1	LSb	VREF = 5.12V(5)
AD03	E_{DL}	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.12V(5)
AD04	E_{OFF}	Offset Error	—	+1.5	+ 2.0	LSb	VREF = 5.12V(5)
AD07	E_{GN}	Gain Error	—	—	±1	LSb	VREF = 5.12V(5)
AD06 AD06A	V_{REF}	Reference Voltage(3)	2.2 2.5	—	— VDD	V	 Absolute minimum to ensure 1 LSb accuracy
AD07	V_{AIN}	Full-Scale Range	VSS	—	VREF	V	
AD08	Z_{AIN}	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	I_{REF}	VREF Input Current(3)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	μA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

5: VREF = 5V for PIC16HV616.

15.13 High Temperature Operation

This section outlines the specifications for the PIC16F616 device operating in a temperature range between -40°C and 150°C.(4) The specifications between -40°C and 150°C(4) are identical to those shown in DS41302 and DS80329.

Note 1: Writes are **not allowed** for Flash Program Memory above 125°C.

2: All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.

3: The temperature range indicator in the part number is “H” for -40°C to 150°C.(4)

Example: PIC16F616T-H/ST indicates the device is shipped in a tAPE and reel configuration, in the TSSOP package, and is rated for operation from -40°C to 150°C.(4)

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

TABLE 15-13: ABSOLUTE MAXIMUM RATINGS

Parameter	Source/Sink	Value	Units
Max. Current: VDD	Source	20	mA
Max. Current: VSS	Sink	50	mA
Max. Current: PIN	Source	5	mA
Max. Current: PIN	Sink	10	mA
Pin Current: at VOH	Source	3	mA
Pin Current: at VOL	Sink	8.5	mA
Port Current: A and C	Source	20	mA
Port Current: A and C	Sink	50	mA
Maximum Junction Temperature		155	°C

Note: Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 15-18: OSCILLATOR PARAMETERS FOR PIC16F616 – H (High Temp.)

Param No.	Sym	Characteristic	Frequency Tolerance	Units	Min	Typ	Max	Conditions
OS08	INTOSC	Int. Calibrated INTOSC Freq.(1)	±10%	MHz	7.2	8.0	8.8	2.0V ≤ V_{DD} ≤ 5.5V -40°C ≤ T_A ≤ 150°C

Note 1: To ensure these oscillator frequency tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

TABLE 15-19: COMPARATOR SPECIFICATIONS FOR PIC16F616 – H (High Temp.)

Param No.	Sym	Characteristic	Units	Min	Typ	Max	Conditions
CM01	V_{OS}	Input Offset Voltage	mV	—	±5	±20	(V_{DD} - 1.5)/2

FIGURE 16-20: PIC16HV610/616 IDD EC (1 MHz) vs. VDD

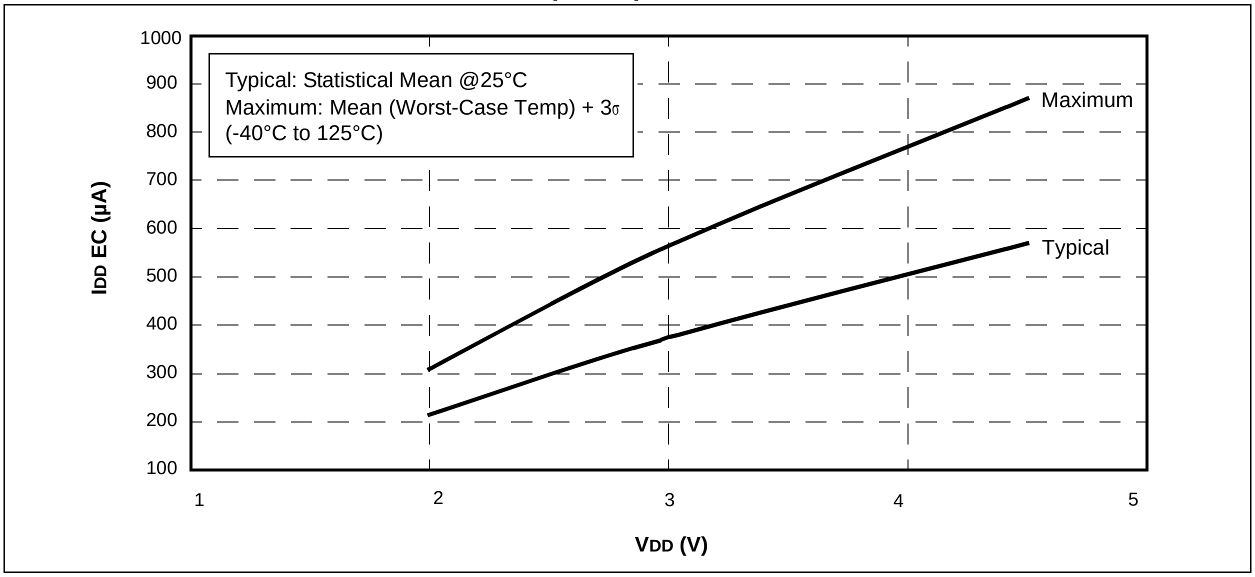


FIGURE 16-21: PIC16HV610/616 IDD EC (4 MHz) vs. VDD

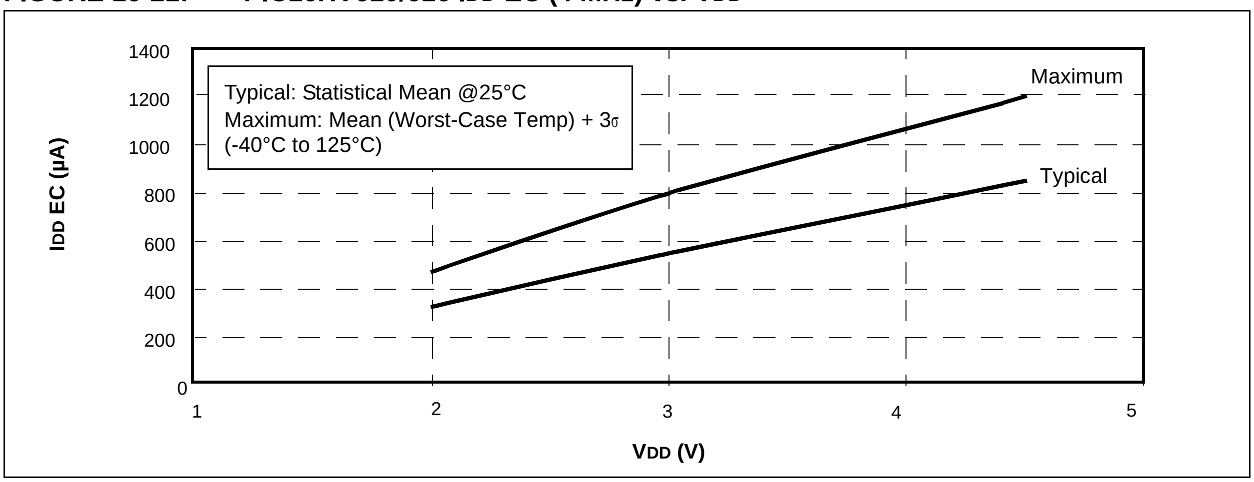


FIGURE 16-22: PIC16HV610/616 IDD XT (1 MHz) vs. VDD

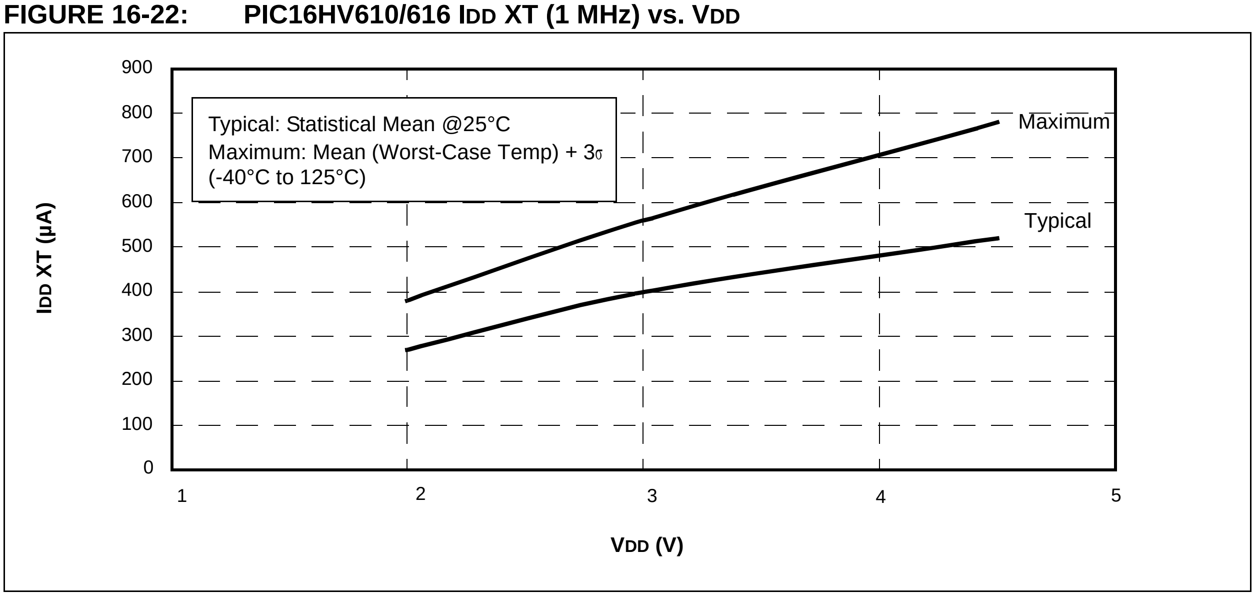


FIGURE 16-37: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

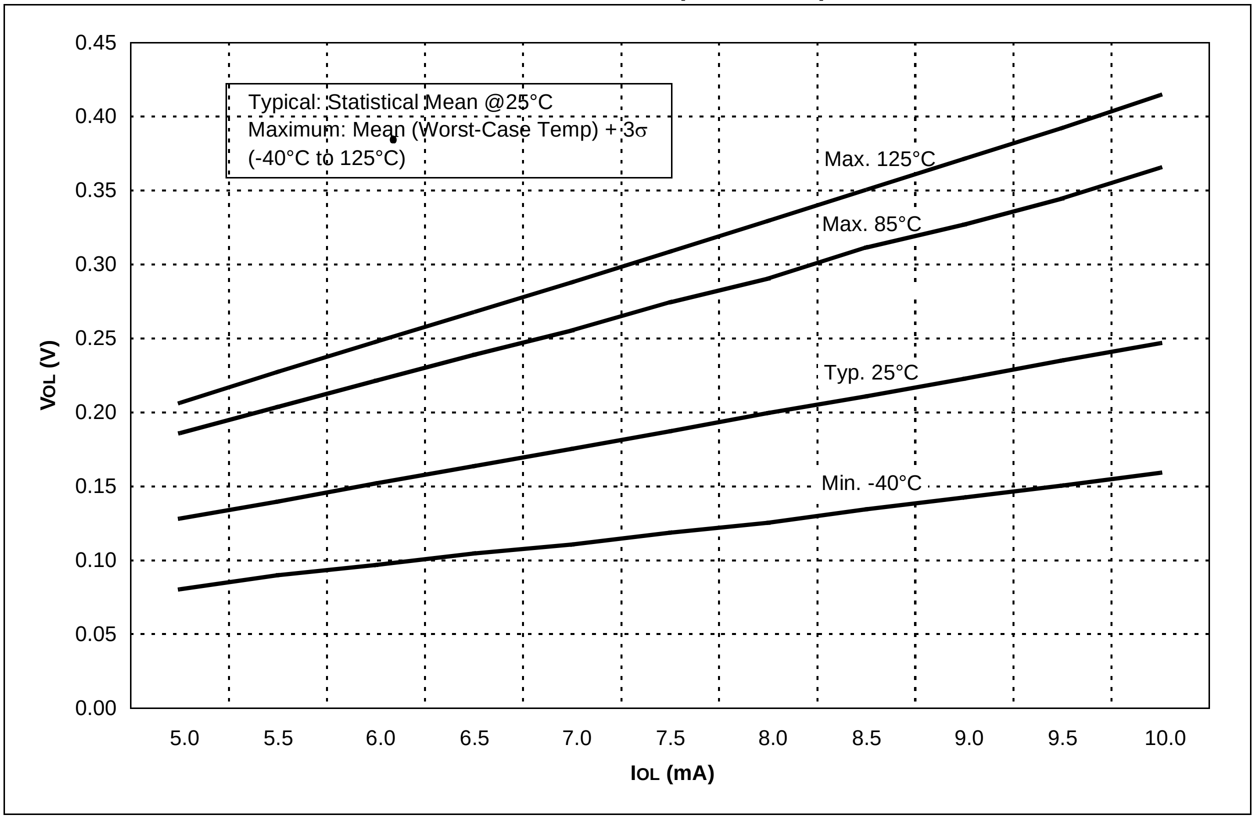


FIGURE 16-38: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)

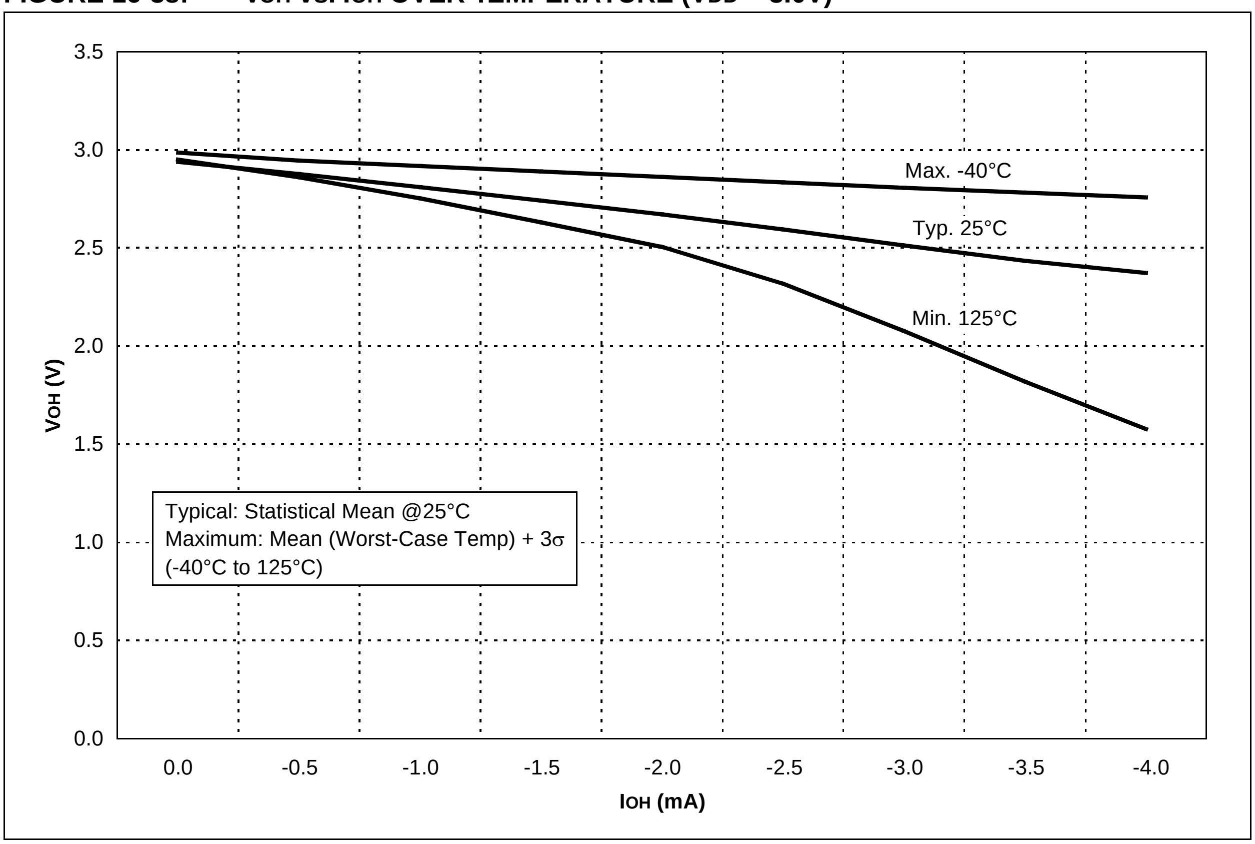


FIGURE 16-43: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

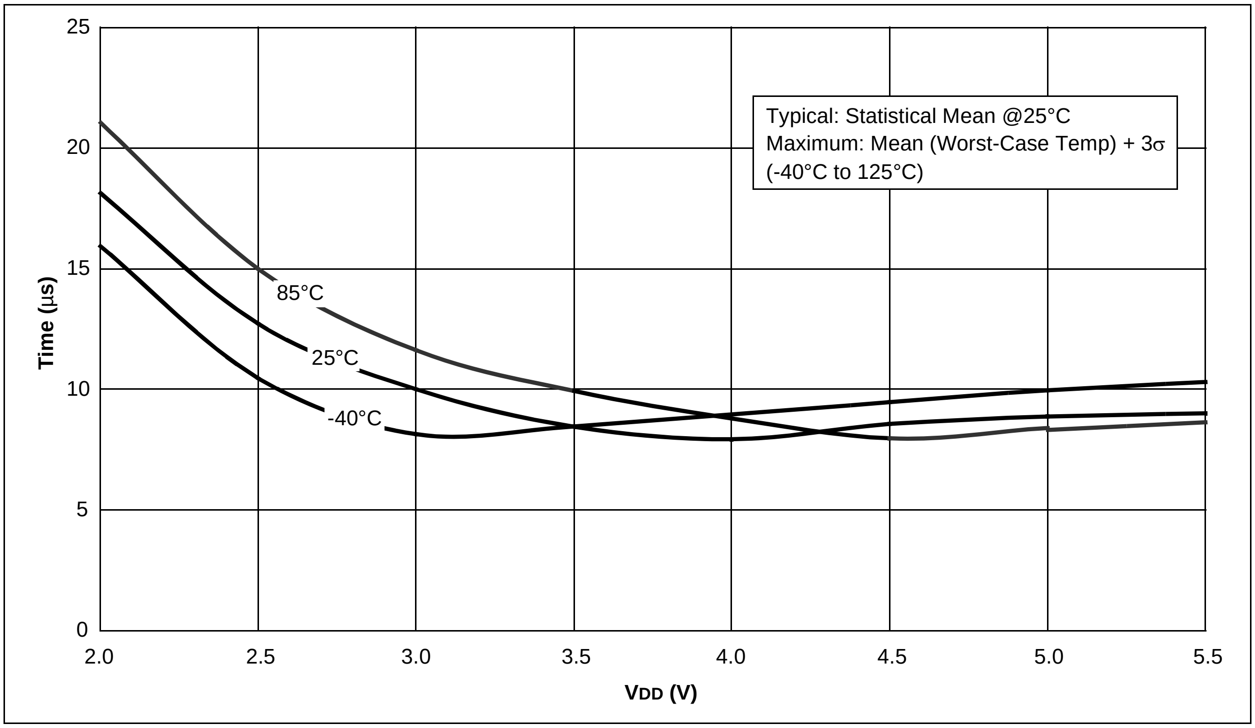


FIGURE 16-44: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE