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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	4.2MHz
Connectivity	I²C, SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	14
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q432a-nnntc0agl

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)

- PWM
  - Resolution 16 bits × 1 channel

- Real time clock
  - Year, month, day, day of the week, hour, minute, and second registers
  - Automatic leap year correction
  - Regular interrupts (0.5 sec, 1 sec, 1 minute, 1 hour)
  - Alarm interrupt × 2 channels (day of the week, hour, minute; month, day hour, minute)

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@4MHz, 50kbps@500kHz)

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- Successive approximation type A/D converter
  - 12-bit A/D converter
  - Input × 2 channels

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 6 channels (including secondary functions)
  - Output-only port × 3 channels (including secondary functions)
  - Input/output port
    ML610Q431: 22 channels (including secondary functions)
    ML610Q432: 14 channels (including secondary functions)

• Product name – Supported Function
The line-up of the ML610Q431 and the ML610Q432 is below.

- Chip (Die) -	ROM type	Low-speed oscillation stop detect reset	Operating temperature	Product availability
ML610Q431-xxxWA	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q431A-xxxWA	Flash ROM	-	-20°C to +70°C	Yes
ML610Q432-xxxWA	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q432A-xxxWA	Flash ROM	-	-20°C to +70°C	Yes

-144-pin plastic LQFP -	ROM type	Low-speed oscillation stop detect reset	Operating temperature	Product availability
ML610Q431-xxxTC	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q432-xxxTC	Flash ROM	Yes	-20°C to +70°C	Yes
ML610Q432A-xxxTC	Flash ROM	-	-20°C to +70°C	Yes

xxx: ROM code number (xxx of the blank product is NNN)
Q: Flash ROM version
A: Low-speed clock oscillation stop detection reset is disabled always (A version)
WA: Chip (Die),
TC: LQFP

BLOCK DIAGRAM

ML610Q431 Block Diagram

Figure 1 show the block diagram of the ML610Q431.
"*" indicates the secondary function of each port.

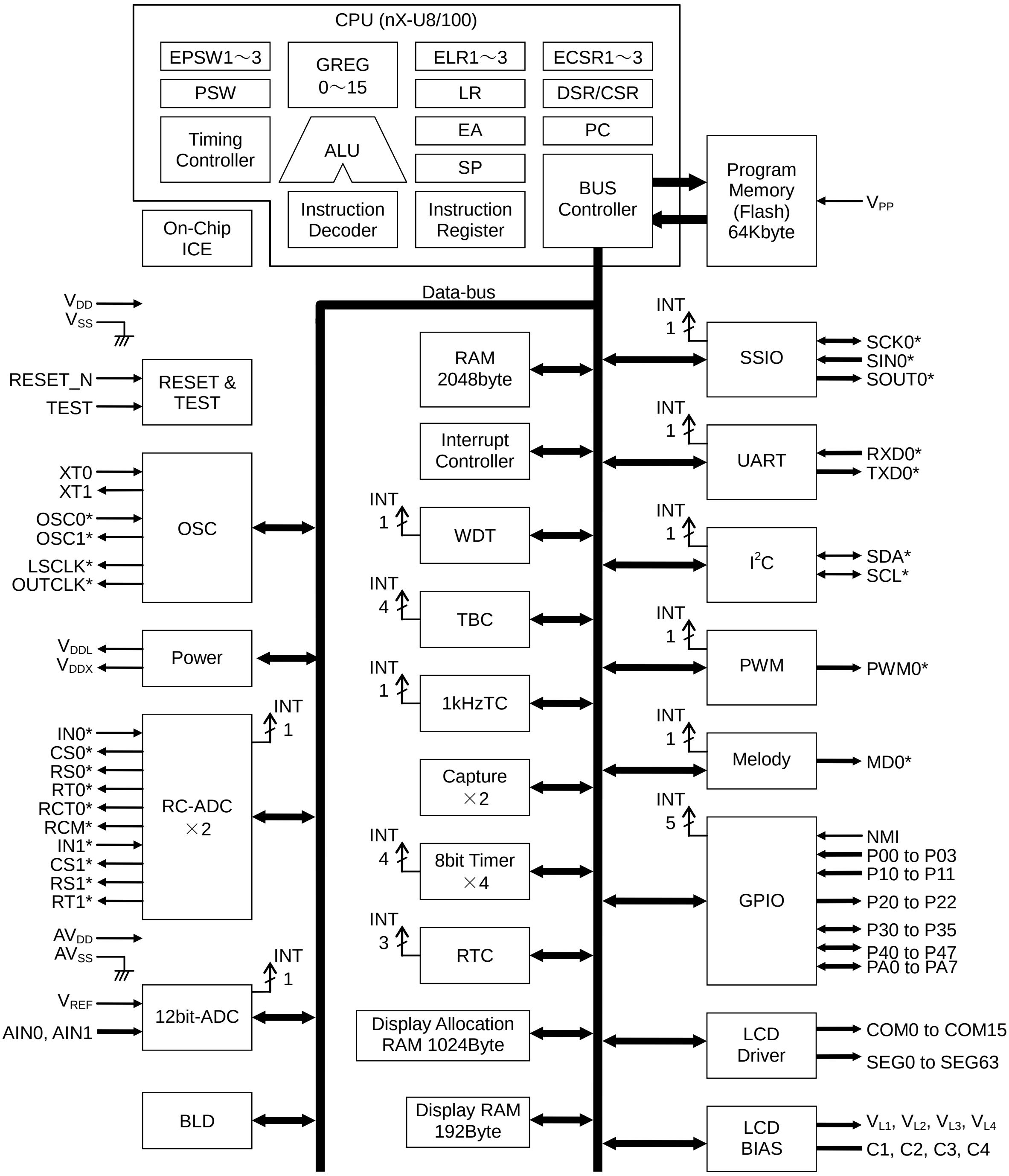


Figure 1 ML610Q431 Block Diagram

ML610Q432 Block Diagram

Figure 2 show the block diagram of the ML610Q432.
"*" indicates the secondary function of each port.

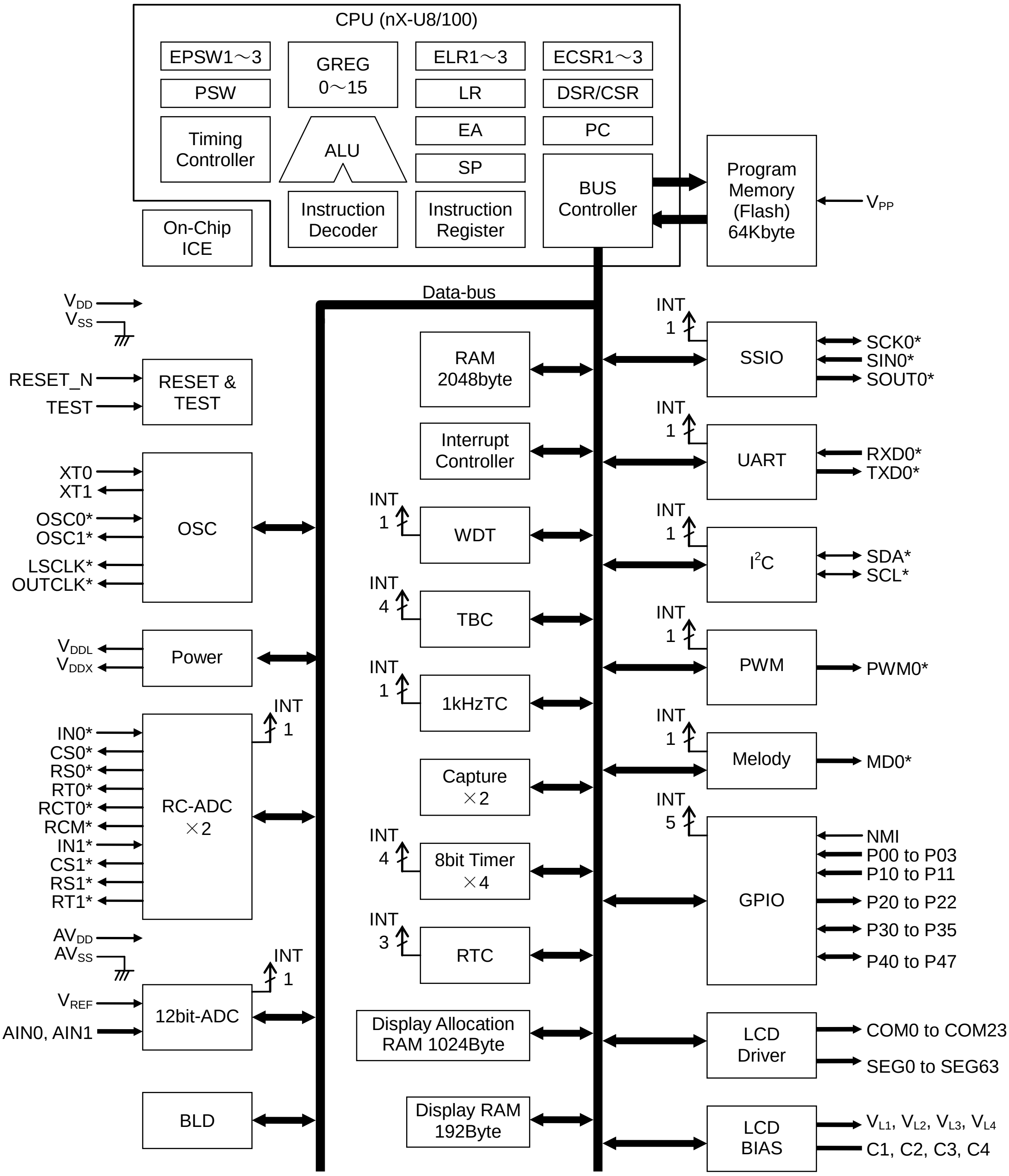


Figure 2 ML610Q432 Block Diagram

ML610Q431 Pad Coordinates

Table 1 ML610Q431 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)
1	P01	-1400	-1978
2	P00	-1300	-1978
3	NMI	-1200	-1978
4	V_{SS}	-1100	-1978
5	P20	-1000	-1978
6	P21	-900	-1978
7	P22	-800	-1978
8	P40	-700	-1978
9	P41	-600	-1978
10	RESET_N	-500	-1978
11	P42	-400	-1978
12	P43	-300	-1978
13	P44	-200	-1978
14	P45	-100	-1978
15	P46	0	-1978
16	P47	100	-1978
17	P30	200	-1978
18	P31	300	-1978
19	P32	400	-1978
20	P33	500	-1978
21	P34	600	-1978
22	P35	700	-1978
23	V_{DDX}	800	-1978
24	XT0	900	-1978
25	XT1	1000	-1978
26	V_{SS}	1100	-1978
27	V_{DDL}	1200	-1978
28	V_{DD}	1300	-1978
29	P10	1400	-1978
30	P11	1528	-1900
31	TEST	1528	-1800
32	PA0	1528	-1700
33	PA1	1528	-1600
34	PA2	1528	-1500
35	PA3	1528	-1400
36	PA4	1528	-1300
37	PA5	1528	-1200
38	PA6	1528	-1100
39	PA7	1528	-1000
40	COM15	1528	-900
41	COM14	1528	-800
42	COM13	1528	-700
43	COM12	1528	-600
44	SEG0	1528	-500
45	SEG1	1528	-400
46	SEG2	1528	-300
47	SEG3	1528	-200
48	SEG4	1528	-100
49	SEG5	1528	0
50	SEG6	1528	100
51	SEG7	1528	200
52	SEG8	1528	300
53	SEG9	1528	400
54	SEG10	1528	500
55	SEG11	1528	600
56	SEG12	1528	700
57	SEG13	1528	800
58	SEG14	1528	900
59	V_{L1}	1528	1000
60	V_{L2}	1528	1100
61	V_{L3}	1528	1200
62	V_{L4}	1528	1300
63	C1	1528	1400
64	C2	1528	1500
65	C3	1528	1600
66	C4	1528	1700
67	SEG15	1528	1800
68	SEG16	1528	1900
69	SEG17	1400	1978
70	SEG18	1300	1978
71	SEG19	1200	1978
72	SEG20	1100	1978
73	SEG21	1000	1978
74	SEG22	900	1978
75	SEG23	800	1978
76	SEG24	700	1978
77	SEG25	600	1978
78	SEG26	500	1978
79	SEG27	400	1978
80	SEG28	300	1978
81	SEG29	200	1978
82	SEG30	100	1978
83	SEG31	0	1978
84	SEG32	-100	1978
85	SEG33	-200	1978
86	SEG34	-300	1978
87	SEG35	-400	1978
88	SEG36	-500	1978
89	SEG37	-600	1978
90	SEG38	-700	1978
91	SEG39	-800	1978
92	SEG40	-900	1978
93	SEG41	-1000	1978
94	SEG42	-1100	1978
95	SEG43	-1200	1978
96	SEG44	-1300	1978
97	SEG45	-1400	1978
98	SEG46	-1528	1900
99	SEG47	-1528	1800
100	V_{DD}	-1528	1700
101	V_{PP}	-1528	1600
102	SEG48	-1528	1500
103	SEG49	-1528	1400
104	SEG50	-1528	1300
105	SEG51	-1528	1200
106	SEG52	-1528	1100
107	SEG53	-1528	1000
108	SEG54	-1528	900
109	SEG55	-1528	800
110	SEG56	-1528	700
111	SEG57	-1528	600
112	SEG58	-1528	500
113	SEG59	-1528	400
114	SEG60	-1528	300
115	SEG61	-1528	200
116	SEG62	-1528	100
117	SEG63	-1528	0
118	COM0	-1528	-100
119	COM1	-1528	-200
120	COM2	-1528	-300
121	COM3	-1528	-400
122	COM4	-1528	-500
123	COM5	-1528	-600
124	COM6	-1528	-700
125	COM7	-1528	-800
126	COM8	-1528	-900
127	COM9	-1528	-1000
128	COM10	-1528	-1100
129	COM11	-1528	-1200
130	A_{VDD}	-1528	-1300
131	V_{REF}	-1528	-1400
132	A_{VSS}	-1528	-1500
133	AIN0	-1528	-1600
134	AIN1	-1528	-1700
135	P03	-1528	-1800
136	P02	-1528	-1900

PAD No.		Primary function			Secondary function			Tertiary function		
Q432	Q431	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
—	38	PA6	I/O	Input/output port	—	—	—	—	—	—
—	39	PA7	I/O	Input/output port	—	—	—	—	—	—
118	118	COM0	O	LCD common pin	—	—	—	—	—	—
119	119	COM1	O	LCD common pin	—	—	—	—	—	—
120	120	COM2	O	LCD common pin	—	—	—	—	—	—
121	121	COM3	O	LCD common pin	—	—	—	—	—	—
122	122	COM4	O	LCD common pin	—	—	—	—	—	—
123	123	COM5	O	LCD common pin	—	—	—	—	—	—
124	124	COM6	O	LCD common pin	—	—	—	—	—	—
125	125	COM7	O	LCD common pin	—	—	—	—	—	—
126	126	COM8	O	LCD common pin	—	—	—	—	—	—
127	127	COM9	O	LCD common pin	—	—	—	—	—	—
128	128	COM10	O	LCD common pin	—	—	—	—	—	—
129	129	COM11	O	LCD common pin	—	—	—	—	—	—
43	43	COM12	O	LCD common pin	—	—	—	—	—	—
42	42	COM13	O	LCD common pin	—	—	—	—	—	—
41	41	COM14	O	LCD common pin	—	—	—	—	—	—
40	40	COM15	O	LCD common pin	—	—	—	—	—	—
39	—	COM16	O	LCD common pin	—	—	—	—	—	—
38	—	COM17	O	LCD common pin	—	—	—	—	—	—
37	—	COM18	O	LCD common pin	—	—	—	—	—	—
36	—	COM19	O	LCD common pin	—	—	—	—	—	—
35	—	COM20	O	LCD common pin	—	—	—	—	—	—
34	—	COM21	O	LCD common pin	—	—	—	—	—	—
33	—	COM22	O	LCD common pin	—	—	—	—	—	—
32	—	COM23	O	LCD common pin	—	—	—	—	—	—
44	44	SEG0	O	LCD segment pin	—	—	—	—	—	—
45	45	SEG1	O	LCD segment pin	—	—	—	—	—	—
46	46	SEG2	O	LCD segment pin	—	—	—	—	—	—
47	47	SEG3	O	LCD segment pin	—	—	—	—	—	—
48	48	SEG4	O	LCD segment pin	—	—	—	—	—	—
49	49	SEG5	O	LCD segment pin	—	—	—	—	—	—
50	50	SEG6	O	LCD segment pin	—	—	—	—	—	—
51	51	SEG7	O	LCD segment pin	—	—	—	—	—	—
52	52	SEG8	O	LCD segment pin	—	—	—	—	—	—
53	53	SEG9	O	LCD segment pin	—	—	—	—	—	—
54	54	SEG10	O	LCD segment pin	—	—	—	—	—	—
55	55	SEG11	O	LCD segment pin	—	—	—	—	—	—
56	56	SEG12	O	LCD segment pin	—	—	—	—	—	—
57	57	SEG13	O	LCD segment pin	—	—	—	—	—	—
58	58	SEG14	O	LCD segment pin	—	—	—	—	—	—
67	67	SEG15	O	LCD segment pin	—	—	—	—	—	—
68	68	SEG16	O	LCD segment pin	—	—	—	—	—	—
69	69	SEG17	O	LCD segment pin	—	—	—	—	—	—
70	70	SEG18	O	LCD segment pin	—	—	—	—	—	—
71	71	SEG19	O	LCD segment pin	—	—	—	—	—	—
72	72	SEG20	O	LCD segment pin	—	—	—	—	—	—
73	73	SEG21	O	LCD segment pin	—	—	—	—	—	—
74	74	SEG22	O	LCD segment pin	—	—	—	—	—	—
75	75	SEG23	O	LCD segment pin	—	—	—	—	—	—
76	76	SEG24	O	LCD segment pin	—	—	—	—	—	—
77	77	SEG25	O	LCD segment pin	—	—	—	—	—	—
78	78	SEG26	O	LCD segment pin	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q432	Q431	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
79	79	SEG27	O	LCD segment pin	—	—	—	—	—	—
80	80	SEG28	O	LCD segment pin	—	—	—	—	—	—
81	81	SEG29	O	LCD segment pin	—	—	—	—	—	—
82	82	SEG30	O	LCD segment pin	—	—	—	—	—	—
83	83	SEG31	O	LCD segment pin	—	—	—	—	—	—
84	84	SEG32	O	LCD segment pin	—	—	—	—	—	—
85	85	SEG33	O	LCD segment pin	—	—	—	—	—	—
86	86	SEG34	O	LCD segment pin	—	—	—	—	—	—
87	87	SEG35	O	LCD segment pin	—	—	—	—	—	—
88	88	SEG36	O	LCD segment pin	—	—	—	—	—	—
89	89	SEG37	O	LCD segment pin	—	—	—	—	—	—
90	90	SEG38	O	LCD segment pin	—	—	—	—	—	—
91	91	SEG39	O	LCD segment pin	—	—	—	—	—	—
92	92	SEG40	O	LCD segment pin	—	—	—	—	—	—
93	93	SEG41	O	LCD segment pin	—	—	—	—	—	—
94	94	SEG42	O	LCD segment pin	—	—	—	—	—	—
95	95	SEG43	O	LCD segment pin	—	—	—	—	—	—
96	96	SEG44	O	LCD segment pin	—	—	—	—	—	—
97	97	SEG45	O	LCD segment pin	—	—	—	—	—	—
98	98	SEG46	O	LCD segment pin	—	—	—	—	—	—
99	99	SEG47	O	LCD segment pin	—	—	—	—	—	—
102	102	SEG48	O	LCD segment pin	—	—	—	—	—	—
103	103	SEG49	O	LCD segment pin	—	—	—	—	—	—
104	104	SEG50	O	LCD segment pin	—	—	—	—	—	—
105	105	SEG51	O	LCD segment pin	—	—	—	—	—	—
106	106	SEG52	O	LCD segment pin	—	—	—	—	—	—
107	107	SEG53	O	LCD segment pin	—	—	—	—	—	—
108	108	SEG54	O	LCD segment pin	—	—	—	—	—	—
109	109	SEG55	O	LCD segment pin	—	—	—	—	—	—
110	110	SEG56	O	LCD segment pin	—	—	—	—	—	—
111	111	SEG57	O	LCD segment pin	—	—	—	—	—	—
112	112	SEG58	O	LCD segment pin	—	—	—	—	—	—
113	113	SEG59	O	LCD segment pin	—	—	—	—	—	—
114	114	SEG60	O	LCD segment pin	—	—	—	—	—	—
115	115	SEG61	O	LCD segment pin	—	—	—	—	—	—
116	116	SEG62	O	LCD segment pin	—	—	—	—	—	—
117	117	SEG63	O	LCD segment pin	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
XT1	O		—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock. A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V_{SS}. This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
OSC1	O		Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q431, but are not provided in the ML610Q432.	Primary	Positive

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
AV_{DD}	V_{SS}
AV_{SS}	V_{SS}
V_{REF}	V_{SS}
AIN0, AIN1	Open
V_{L1}, V_{L2}, V_{L3}, V_{L4}	Open
C1, C2, C3, C4	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V_{DD} or V_{SS}
P10 to P11	V_{DD}
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7	Open
COM0 to 23	Open
SEG0 to 63	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Unit
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor *1	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation *2	—	0	—	pF
		C_L=9pF of crystal oscillation	—	6	—	
		C_L=12pF of crystal oscillation	—	12	—	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	—	4.0M / 4.096M	—	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	—	24	—	pF
	C_{GH}	—	—	24	—	

*1: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.
*2: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase*1	2.75 to 3.6	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase*1	7.7 to 8.3	
Write cycles	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

*1:When writing to and erasing on the flash Memory, the voltage in the specified range needs to be supplied to the V_{DDL} pin.
The V_{PP} pin has an internal pull-down resistor.

DC CHARACTERISTICS (2/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified) (2/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L1} voltage	V_{L1}	V_{DD} = 3.0V, Tj = 25°C	CN4–0 = 00H	0.89	0.94	0.99	V	1
			CN4–0 = 01H	0.91	0.96	1.01		
			CN4–0 = 02H	0.93	0.98	1.03		
			CN4–0 = 03H	0.95	1.00	1.05		
			CN4–0 = 04H	0.97	1.02	1.07		
			CN4–0 = 05H	0.99	1.04	1.09		
			CN4–0 = 06H	1.01	1.06	1.11		
			CN4–0 = 07H	1.03	1.08	1.13		
			CN4–0 = 08H	1.05	1.10	1.15		
			CN4–0 = 09H	1.07	1.12	1.17		
			CN4–0 = 0AH	1.09	1.14	1.19		
			CN4–0 = 0BH	1.11	1.16	1.21		
			CN4–0 = 0CH	1.13	1.18	1.23		
			CN4–0 = 0DH	1.15	1.20	1.25		
			CN4–0 = 0EH	1.17	1.22	1.27		
			CN4–0 = 0FH	1.19	1.24	1.29		
			CN4–0 = 10H	1.21	1.26	1.31		
			CN4–0 = 11H	1.23	1.28	1.33		
			CN4–0 = 12H	1.25	1.30	1.35		
			CN4–0 = 13H	1.27	1.32	1.37		
			CN4–0 = 14H *1	1.29	1.34	1.39		
			CN4–0 = 15H *1	1.31	1.36	1.41		
			CN4–0 = 16H *1	1.33	1.38	1.43		
			CN4–0 = 17H *1	1.35	1.40	1.45		
			CN4–0 = 18H *1	1.37	1.42	1.47		
			CN4–0 = 19H *1	1.39	1.44	1.49		
			CN4–0 = 1AH *1	1.41	1.46	1.51		
			CN4–0 = 1BH *1	1.43	1.48	1.53		
			CN4–0 = 1CH *1	1.45	1.50	1.55		
			CN4–0 = 1DH *1	1.47	1.52	1.57		
			CN4–0 = 1EH *1	1.49	1.54	1.59		
			CN4–0 = 1FH *1	1.51	1.56	1.61		
V_{L1} temperature deviation	ΔV_{L1}	V_{DD} = 3.0V		—	−1.5	—	mV/°C	
V_{L1} voltage dependency	ΔV_{L1}	V_{DD} = 1.3 to 3.6V		—	5	20	mV/V	
V_{L2} voltage	V_{L2}	V_{DD} = 3.0V, Tj = 25°C 300kΩ load (V_{L4}–V_{SS})		Typ. −10%	V_{L1}×2	Typ. +4%	V	
V_{L3} voltage	V_{L3}	V_{DD} = 3.0V, Tj = 25°C 300kΩ load (V_{L4}–V_{SS})	1/3 bias	Typ. −10%	V_{L1}×2	Typ. +4%		
			1/4 bias		V_{L1}×3			
V_{L4} voltage	V_{L4}		1/3 bias	Typ. −10%	V_{L1}×3	Typ. +5%		
			1/4 bias		V_{L1}×4			
LCD bias voltage generation time	T_{BIAS}	—		—	—	600	ms	

*1: When using 1/4 bias, the V_{L1} voltage is set to typ. 1.32 V (same voltage as in CN4–0 = 13H).

DC CHARACTERISTICS (3/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	V_{DD} = 1.35 to 3.6V	LD2–0 = 0H	Typ. –2%	1.35	Typ. +2%	V	1
			LD2–0 = 1H		1.4			
			LD2–0 = 2H		1.45			
			LD2–0 = 3H		1.5			
			LD2–0 = 4H		1.6			
			LD2–0 = 5H		1.7			
			LD2–0 = 6H		1.8			
			LD2–0 = 7H		1.9			
			LD2–0 = 8H		2.0			
			LD2–0 = 9H		2.1			
			LD2–0 = 0AH		2.2			
			LD2–0 = 0BH		2.3			
			LD2–0 = 0CH		2.4			
			LD2–0 = 0DH		2.5			
			LD2–0 = 0EH		2.7			
			LD2–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	V_{DD} = 1.35 to 3.6V		—	0.1	—	%/°C	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.15	0.50	µA	
			Ta = -20 to +70°C	—	—	2.50		
Supply current 2	IDD2	CPU: In HALT state (LTBC, RTC: Operating*[3]*[5]). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	Ta = 25°C	—	0.5	1.3	µA	
			Ta = -20 to +70°C	—	—	3.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*[1]*[3] High-speed oscillation: Stopped. LCD/BIAS circuits: Operating.*[2]	Ta = 25°C	—	5	7	µA	
			Ta = -20 to +70°C	—	—	12		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating.*[2]	Ta = 25°C	—	70	85	µA	
			Ta = -20 to +70°C	—	—	100		
Supply current 5	IDD5	CPU: In 4.096MHz operating state.*[2]*[3] PLL: In oscillating state. LCD/BIAS circuits: Operating. *[2] V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.8	1.0	mA	
			Ta = -20 to +70°C	—	—	1.2		
Supply current 6	IDD6	CPU: In 4.096MHz operating state.*[2] PLL: In oscillating state. *[3]*[4] A/D: In operating state. LCD/BIAS circuits: Operating. *[2] V_{DD} = AV_{DD} = 3.0V	Ta = 25°C	—	1.5	1.6	mA	
			Ta = -20 to +70°C	—	—	2.5		

*[1]: CPU operating rate is 100% (No HALT state).
*[2]: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*[3] : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*[4] : Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).
*[5] : Significant bits of BLKCON0~BLKCON4 registers are all “1”.

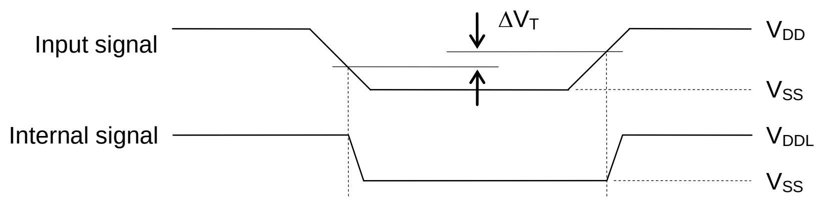
DC CHARACTERISTICS (5/5))

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (5/5)

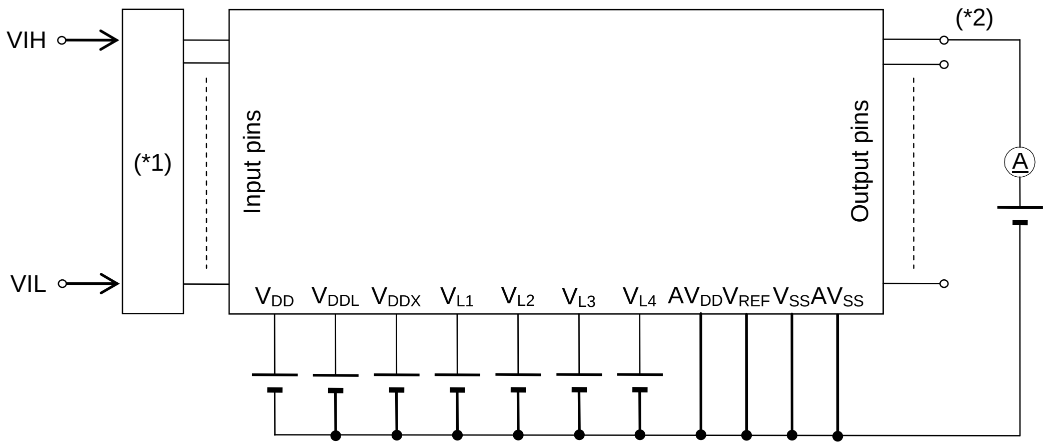
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)*1	VIH1	V_{DD} = 1.3 to 3.6V	0.7 ×V_{DD}	—	V_{DD}	V	5
		V_{DD} = 1.1 to 3.6V	0.7 ×V_{DD}	—	V_{DD}		
	VIL1	V_{DD} = 1.3 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0	—	0.2 ×V_{DD}		
Hysteresis width (RESET_N) (TEST_N) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)*1	ΔVT	V_{DD} = 2.0 to 3.6V	0.05 ×V_{DD}	0.18 ×V_{DD}	0.4 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0.02 ×V_{DD}	0.18 ×V_{DD}	0.4 ×V_{DD}		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7)*1	CIN	f = 10kHz, V_{rms} = 50mV, Ta = 25°C	—	—	5	pF	—

*1: ML610Q431 only

HYSTERESIS WIDTH

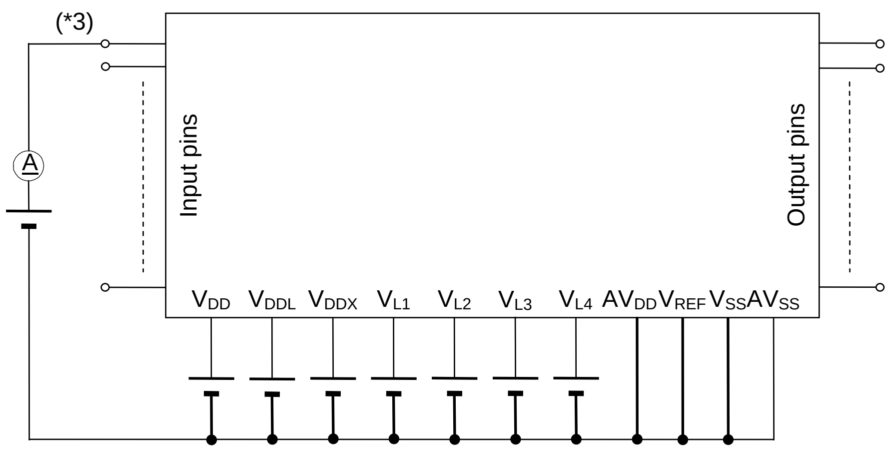


MEASURING CIRCUIT 3



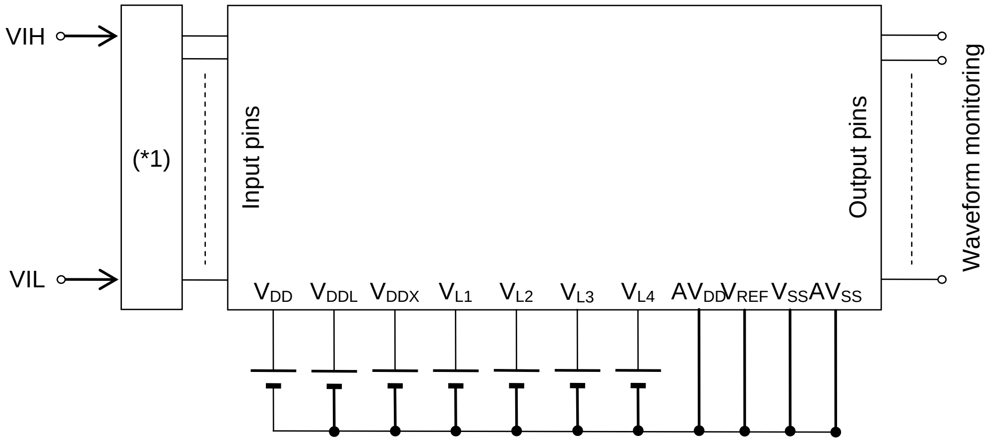
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5



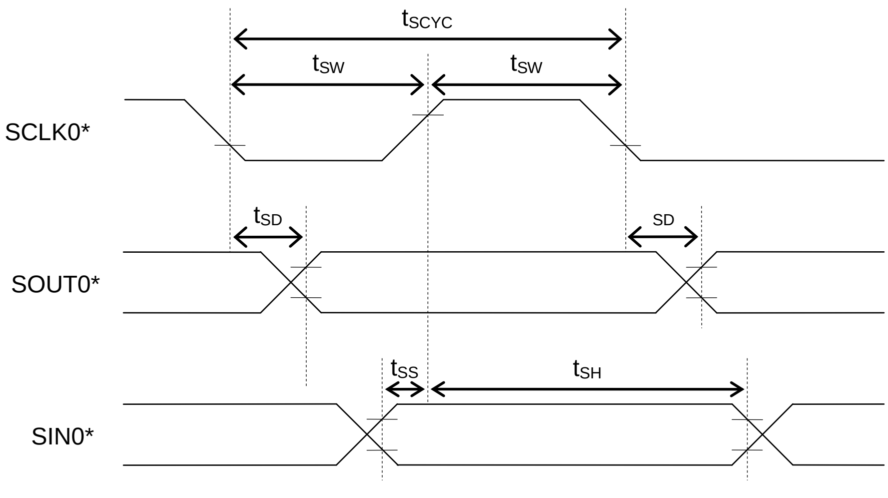
*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When RC oscillation is active*[2] (V_{DD} = 1.3 to 3.6V)	10	—	—	μs
		When high-speed oscillation is active*[3] (V_{DD} = 1.8 to 3.6V)	1	—	—	μs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*[1]	—	s
SCLK input pulse width (slave mode)	t_{SW}	When RC oscillation is active*[2] (V_{DD} = 1.3 to 3.6V)	4	—	—	μs
		When high-speed oscillation is active*[3] (V_{DD} = 1.8 to 3.6V)	0.4	—	—	μs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*[1] ×0.4	SCLK*[1] ×0.5	SCLK*[1] ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	When RC oscillation is active*[2] (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*[3] (V_{DD} = 1.8 to 3.6V)	—	—	240	
SOUT output delay time (master mode)	t_{SD}	When RC oscillation is active*[2] (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*[3] (V_{DD} = 1.8 to 3.6V)	—	—	240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	When RC oscillation is active*[2] (V_{DD} = 1.3 to 3.6V)	500	—	—	ns
		When high-speed oscillation is active*[3] (V_{DD} = 1.8 to 3.6V)	240	—	—	
SIN input hold time	t_{SH}	When RC oscillation is active*[2] (V_{DD} = 1.3 to 3.6V)	300	—	—	ns
		When high-speed oscillation is active*[3] (V_{DD} = 1.8 to 3.6V)	80	—	—	

*[1]: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)
*[2]: When RC oscillation is selected with OSCM1–0 of the frequency control register (FCON0)
*[3]: When Crystal/ceramic oscillation, built-in PLL oscillation, or external clock input is selected with OSCM1–0 of the frequency control register (FCON0)



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I^{2}C Bus Interface: Standard Mode 100kHz)

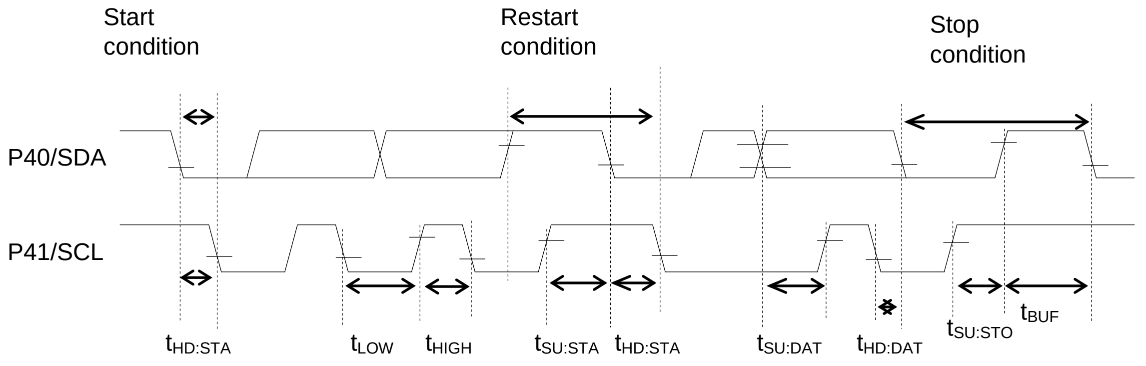
(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL ”L” level time	t_{LOW}	—	4.7	—	—	µs
SCL ”H” level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	3.45	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC CHARACTERISTICS (I^{2}C Bus Interface: Fast Mode 400kHz)

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL ”L” level time	t_{LOW}	—	1.3	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	0.9	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



AC CHARACTERISTICS (RC Oscillation A/D Converter)

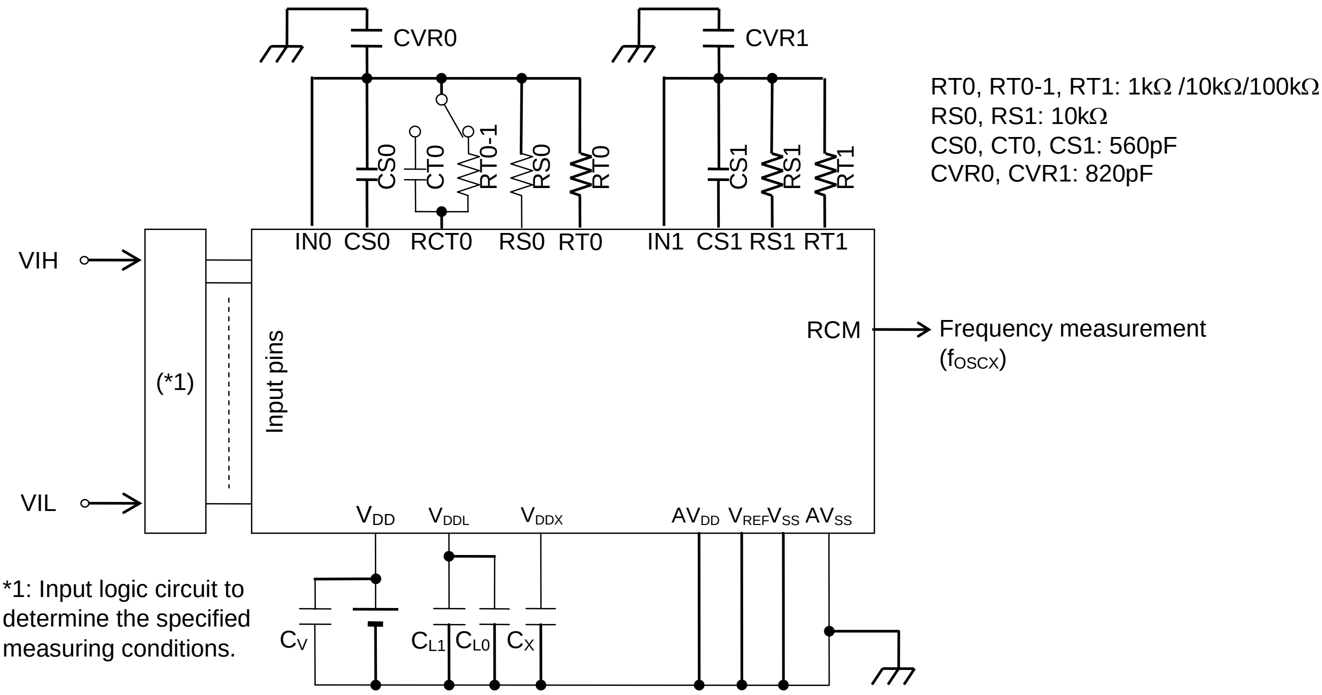
(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Unit
Resistors for oscillation	RS0, RS1, RT0, RT0-1,RT1	CS0, CT0, CS1 ≥ 740pF	1	—	—	kΩ
Oscillation frequency VDD = 1.5V	f_{OSC1}	Resistor for oscillation = 1kΩ	209.4	330.6	435.1	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	41.29	55.27	64.16	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	4.71	5.97	7.06	kHz
RS to RT oscillation frequency ratio *1 VDD = 1.5V	Kf1	RT0, RT0-1, RT1 = 1kHz	5.567	5.982	6.225	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.104	0.108	0.118	—
Oscillation frequency VDD = 3.0V	f_{OSC1}	Resistor for oscillation = 1kΩ	407.3	486.7	594.6	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	49.76	59.28	72.76	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	5.04	5.993	7.04	kHz
RS to RT oscillation frequency ratio *1 VDD = 3.0V	Kf1	RT0, RT0-1, RT1 = 1kHz	8.006	8.210	8.416	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.100	0.108	0.115	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCX}(\text{RT0–CS0 oscillation})}{f_{OSCX}(\text{RS0–CS0 oscillation})}, \quad \frac{f_{OSCX}(\text{RT0-1–CS0 oscillation})}{f_{OSCX}(\text{RS0–CS0 oscillation})}, \quad \frac{f_{OSCX}(\text{RT1–CS1 oscillation})}{f_{OSCX}(\text{RS1–CS1 oscillation})}$$

(x = 1, 2, 3)



Note:

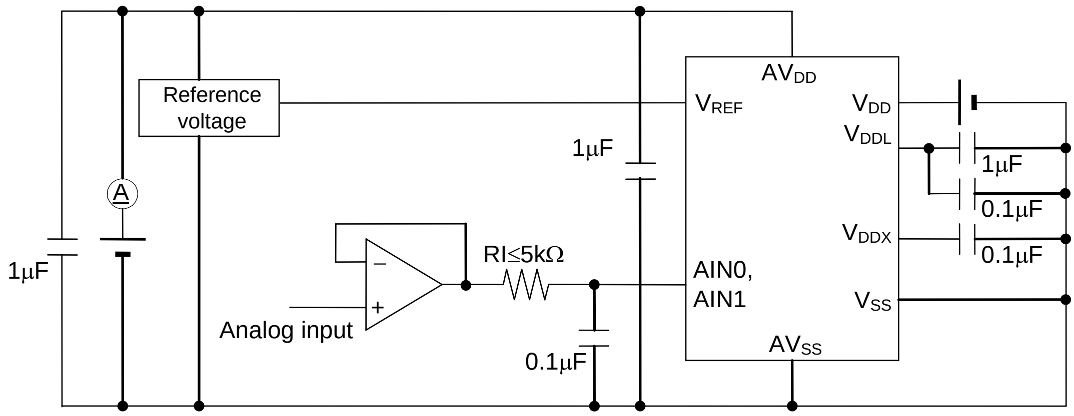
- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resisteor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 3.6V	−4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	−6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	−3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	−5	—	+5	
Zero-scale error	V_{OFF}	—	−6	—	+6	
Full-scale error	FSE	—	−6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	SACK = 0 (HSCLK = 375kHz to 625kHz)	—	25	—	φ/CH
		SACK = 1 (HSCLK = 1.5MHz to 4.2MHz)	—	112	—	

φ: Period of high-speed clock (HSCLK)



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q431-01	Jun.29,2010	—	—	Formally edition 1.0
FEDL610Q431-02	Feb.8,2011	3	3	The product name of A version is abbed.
		4	4	Terminal name CRT0 is corrected to RCT0.
		5	5	Terminal name CRT0 is corrected to RCT0.
		23	23	Typ value"0" of a BLD threshold voltage temperature deviation is corrected to "0.1."
		33	33	Substitution of a packege dimensions.
FEDL610Q431-03	Mar.23,2015	All	All	Change header and footer.
		3	4	Change from "Shipment" to "Product name － Supported Function"
		—	22	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		21	23	Change "RESET" to "Reset pulse width (P_{RST}) " and "Power-on reset activation power rise time (T_{POR}) ".
		35	37	Change description in Notes.
		2	2	Corrected a typo. “100kbps@1MHz HSCLK” is corrected to 100kbps@4MHz HSCLK.

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