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Understanding **Embedded - Microprocessors**

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d5eym10ac

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

- — Three I2C, supporting 400 kbps
- — Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps
- — Four Pulse Width Modulators (PWM)
- — System JTAG Controller (SJC)
- — GPIO with interrupt capabilities
- — 8x8 Key Pad Port (KPP)
- — Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- — Two Controller Area Network (FlexCAN), 1 Mbps each
- — Two Watchdog timers (WDOG)
- — Audio MUX (AUDMUX)

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPUs)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES 2.0) version 4
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

i.MX 6Dual/6Quad Applications Processors for Consumer Products, Rev. 1

- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU3Dv4	Graphics Processing Unit, ver. 4	Multimedia Peripherals	The GPU3Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.

4.1.9   PCIe 2.0 Maximum Power Consumption

Table 25 provides PCIe PHY currents for certain operating modes.

Table 14. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
PO: Normal Operation	5G Operations	PCIe_VP (1.1 V)	40	mA
		PCIe_VPTX (1.1 V)	20	
		PCIe_VPH (2.5 V)	21	
	2.5G Operations	PCIe_VP (1.1 V)	27	
		PCIe_VPTX (1.1 V)	20	
		PCIe_VPH (2.5 V)	20	
POs: Low Recovery Time Latency, Power Saving State	5G Operations	PCIe_VP (1.1 V)	30	mA
		PCIe_VPTX (1.1 V)	2.4	
		PCIe_VPH (2.5 V)	18	
	2.5G Operations	PCIe_VP (1.1 V)	20	
		PCIe_VPTX (1.1 V)	2.4	
		PCIe_VPH (2.5 V)	18	
P1: Longer Reocvery Time Latency, Lower Power State		PCIe_VP (1.1 V)	12	mA
		PCIe_VPTX (1.1 V)	2.4	
		PCIe_VPH (2.5 V)	12	
Power Down		PCIe_VP (1.1 V)	1.3	mA
		PCIe_VPTX (1.1 V)	0.18	
		PCIe_VPH (2.5 V)	0.36	

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see Table 7 for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDDHIGH_IN (see Table 7 for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 2.25V or 2.75V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the

4.9.3.5   General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20 and Table 39 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual for the EIM programming model.
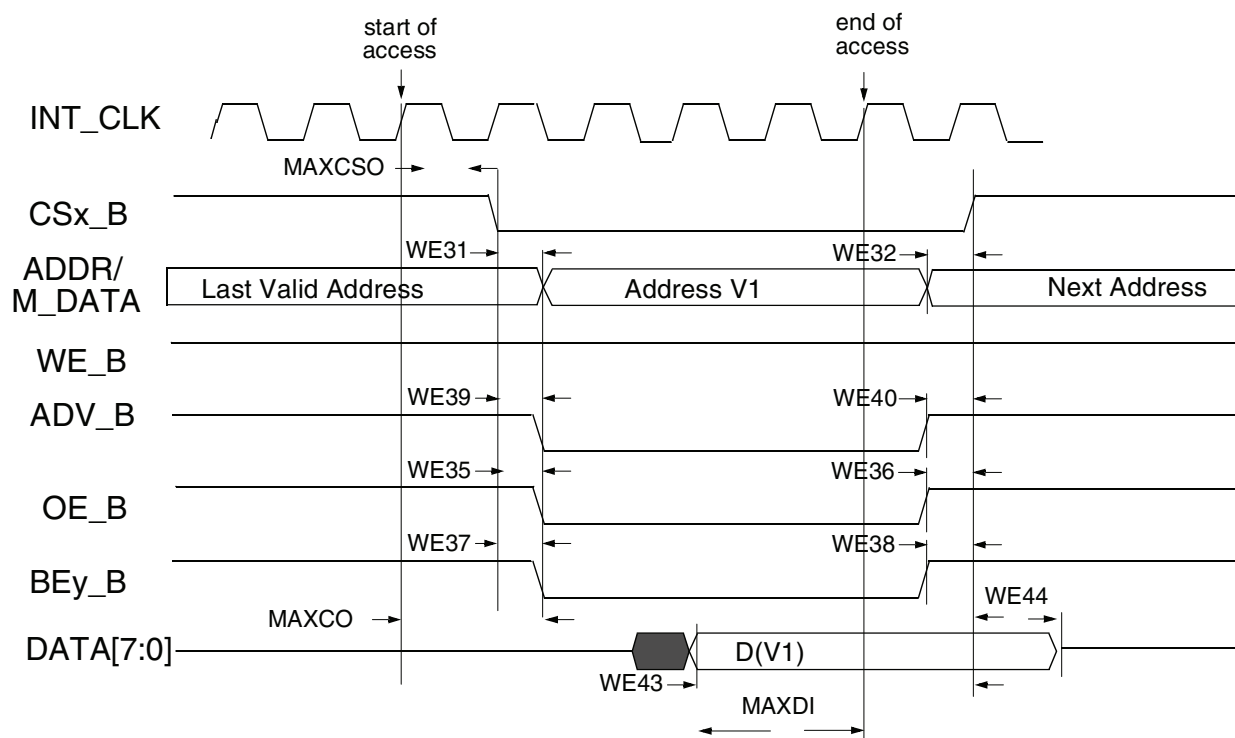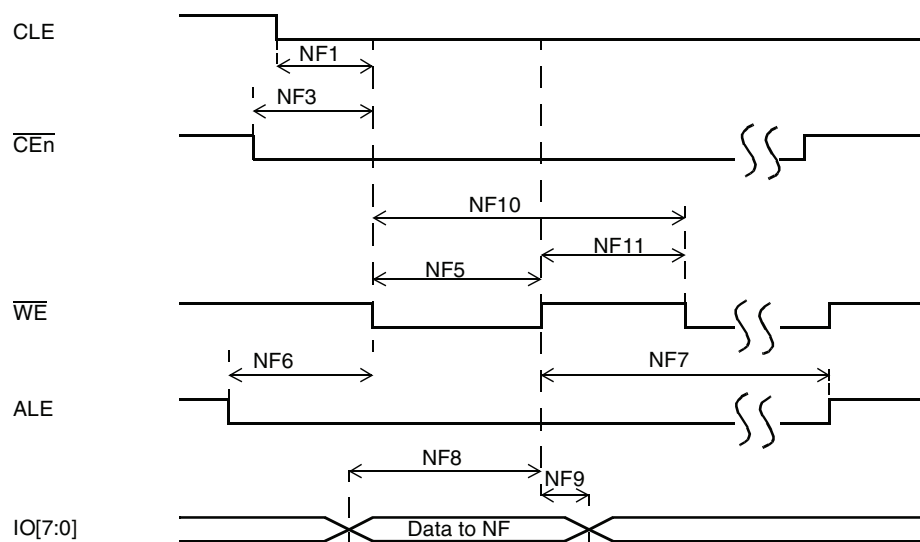

Figure 16. Asynchronous Memory Read Access (RWSC = 5)

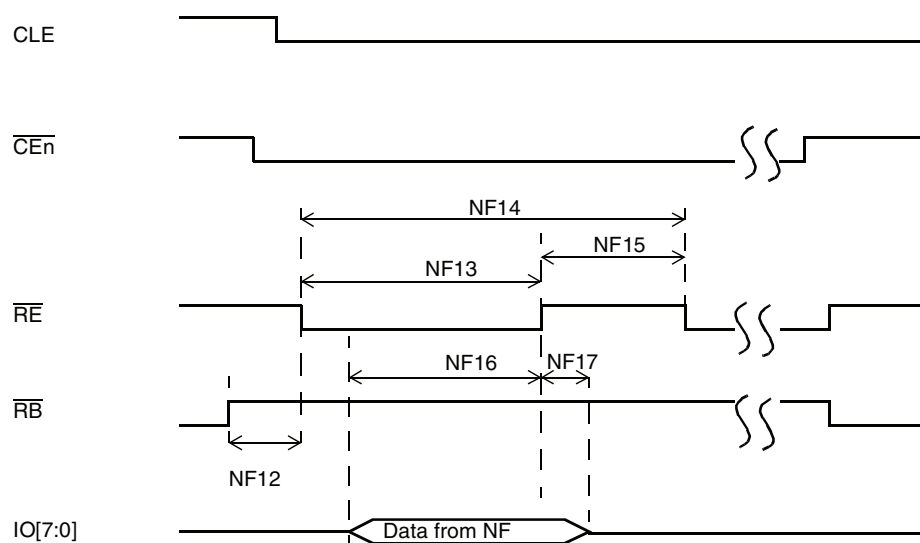**Figure 30. Write Data Latch Cycle Timing Diagram**

Figure 31. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

4.11.2.2 ECSPI Slave Mode Timing

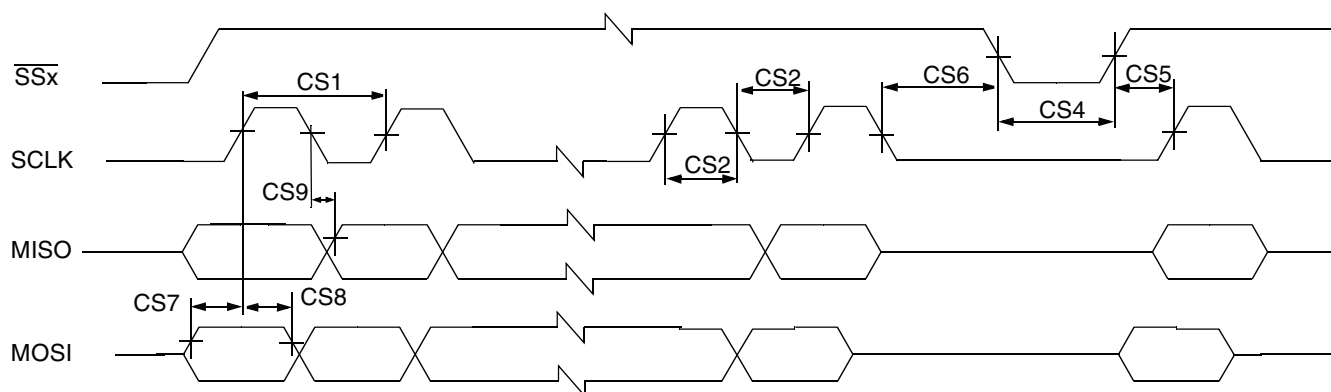Figure 40 depicts the timing of ECSPI in slave mode and Table 50 lists the ECSPI slave mode timing characteristics.

Figure 40. ECSPI Slave Mode Timing Diagram

Table 50. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read • Slow group[1] • Fast group[2] SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	SCLK High or Low Time–Read • Slow group[1] • Fast group[2] SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF) • Slow group[1] • Fast group[2]	t_{PDmiso}	4	 25 17	ns

[1] ECSPI slow include:
 ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/DISP0_DAT17, ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

[2] ECSPI fast include:
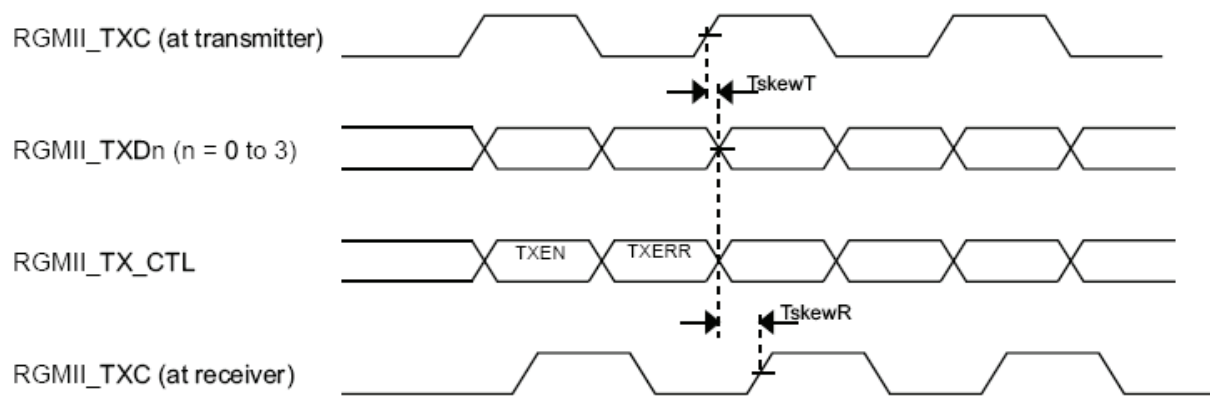 ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

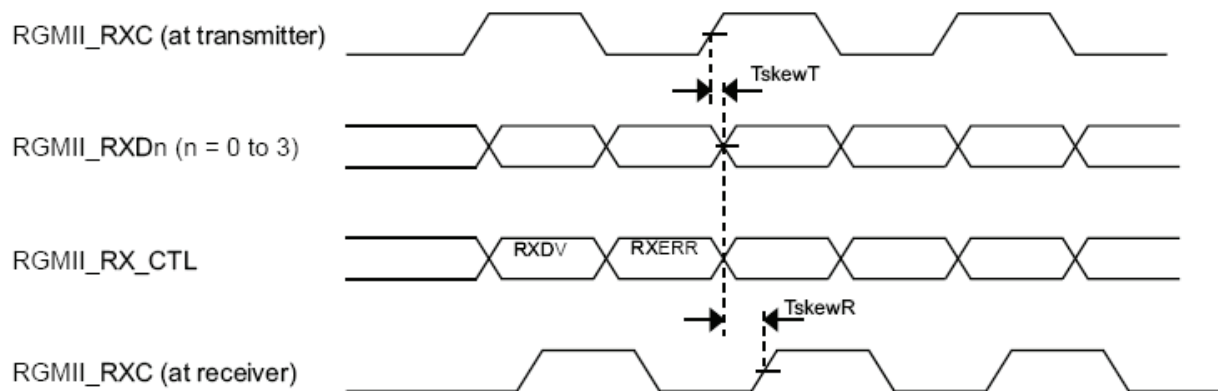**Figure 51. RGMII Transmit Signal Timing Diagram Original**

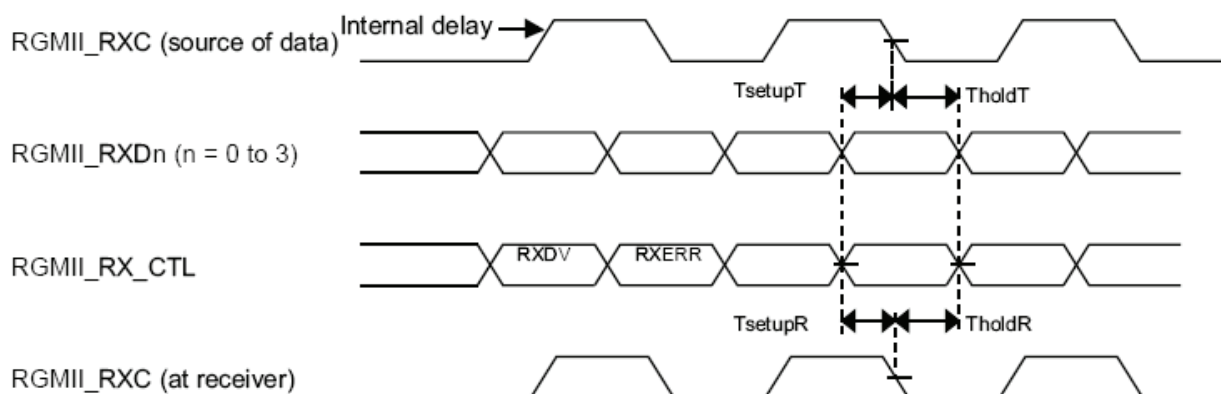**Figure 52. RGMII Receive Signal Timing Diagram Original**

Figure 53. RGMII Receive Signal Timing Diagram with Internal Delay

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal.
If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

Table 70. Electrical and Timing Information (continued)

V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		920			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold		200		450	mV

4.11.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 71 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.
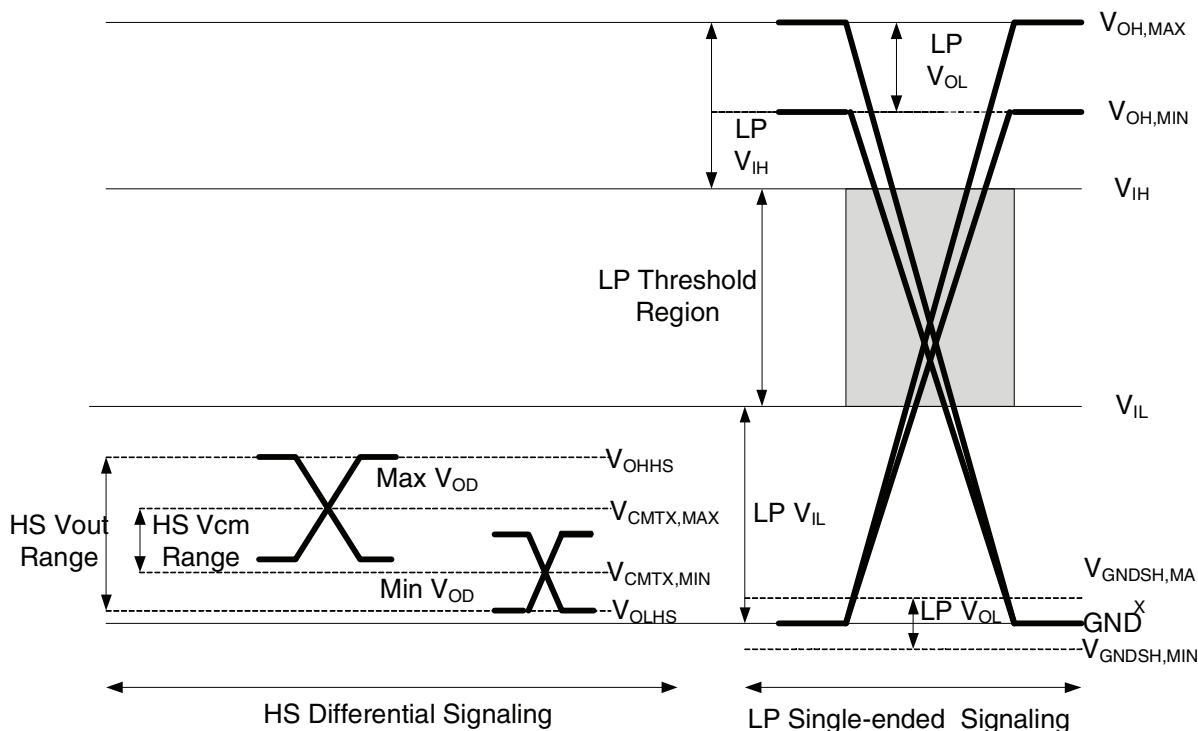

Figure 71. D-PHY Signaling Levels

Table 71. Electrical and Timing Information

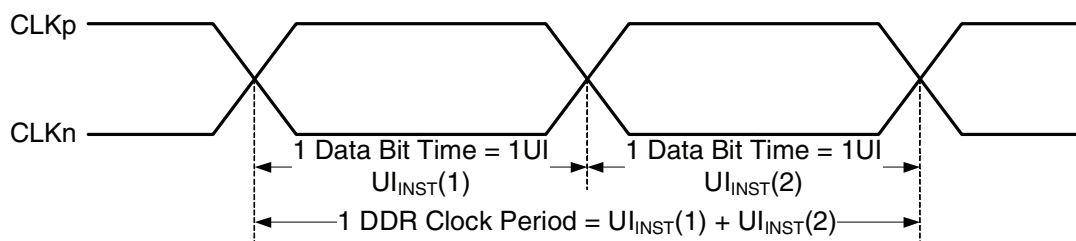|						
L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

Figure 74. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 75:
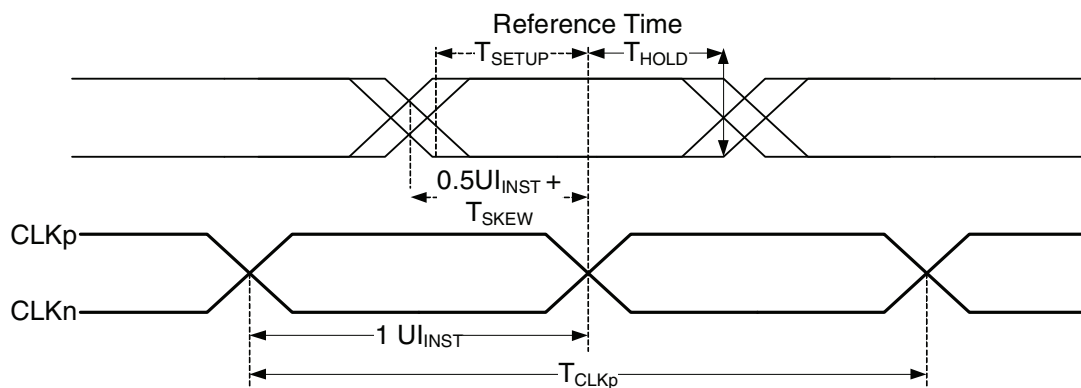

Figure 75. Data to Clock Timing Definitions

Table 80. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

- All timings are on Audiomux Pads when SSI is being used for data transfer.

- "Tx" and "Rx" refer to the Transmit and Receive sections of the SSI.

- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).

- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.3 SSI Transmitter Timing with External Clock

Figure 95 depicts the SSI transmitter external clock timing and Table 81 lists the timing parameters for the transmitter timing with the external clock.
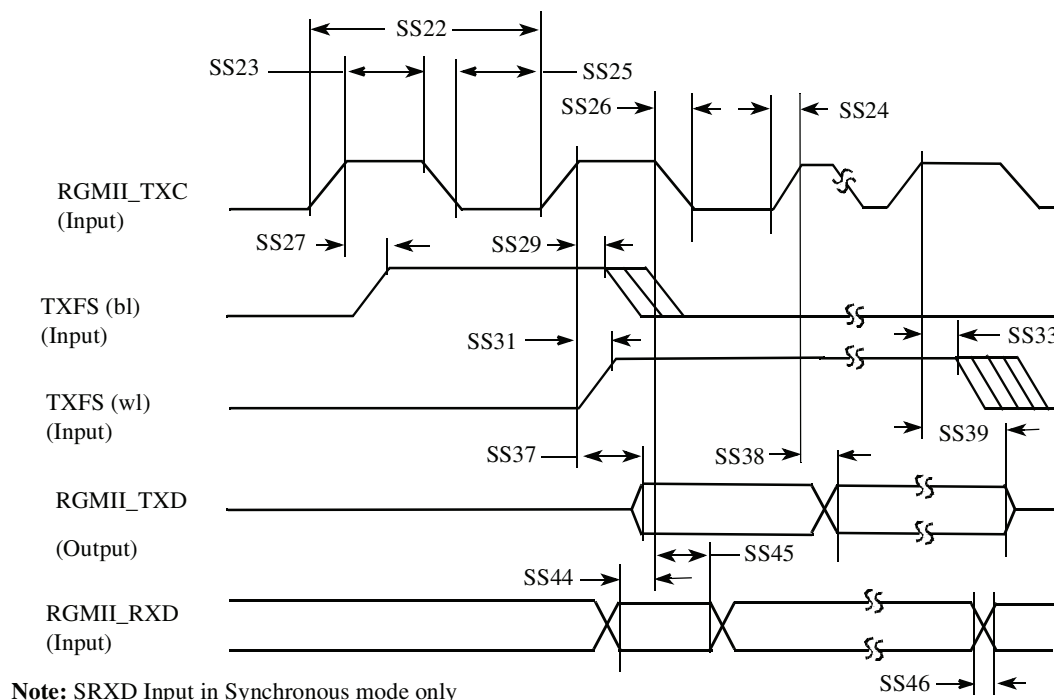

Figure 95. SSI Transmitter External Clock Timing Diagram

Table 81. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	−10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	−10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

4.11.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 99 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 86 lists the transmit timing characteristics.
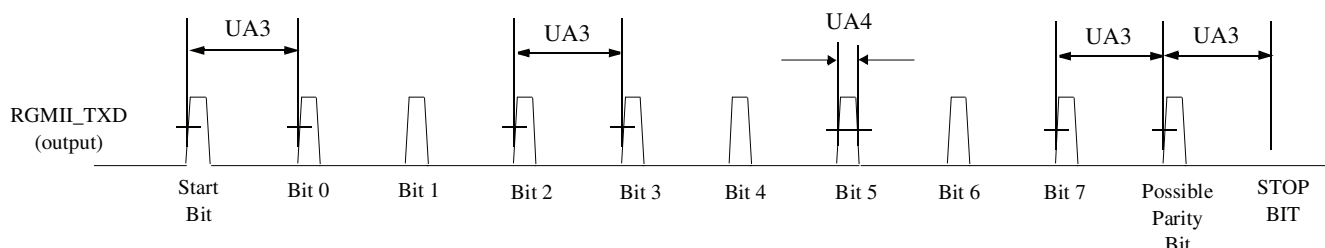

Figure 99. UART IrDA Mode Transmit Timing Diagram

Table 86. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] $- T_{ref\_clk}$[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16)*(1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 100 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 87 lists the receive timing characteristics.
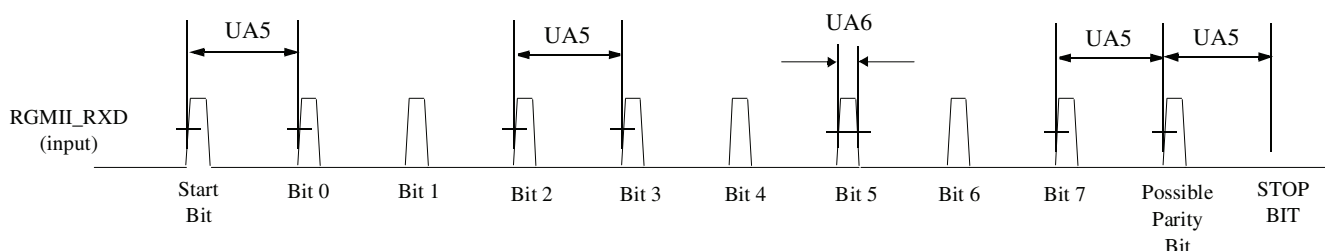
Figure 100. UART IrDA Mode Receive Timing Diagram

Table 87. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] $- 1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16)*(1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 21 x 21 mm Package Information

6.1.1 Case FCPBGA, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

6.1.1.1 21 x 21 mm Bare Die Package

6.1.2   21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 92 shows the device connection list for ground, power, sense, and reference contact signals.

Table 92. 21 x 21 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
FA_ANA	A5	
GND	A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5	
GPANAIO	C8	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9	Supply of the DDR interface
NVCC_EIM0	K19	Supply of the EIM interface
NVCC_EIM1	L19	Supply of the EIM interface
NVCC_EIM2	M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered.
NVCC_MIPI	K7	Supply of the MIPI interface

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Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[13]	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[12]	Input	PU (100K)
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[3]	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[2]	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[4]	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[5]	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[6]	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[7]	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[1]	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[0]	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[18]	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[17]	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[8]	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[10]	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[9]	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[8]	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[9]	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[10]	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[11]	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	gpio2_PIO[12]	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[13]	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[14]	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[15]	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_ SNVS_TD1	Input	PD (100K)
TEST_MODE	E12	VDD_SNVS_IN			Reserved—Factory Use Only	Input	PD (100K)
USB_H1_DN	F10	VDDUSB_CAP			USB_H1_DN	—	—
USB_H1_DP	E10	VDDUSB_CAP			USB_H1_DP	—	—
USB_H1_VBUS	D10	VDDUSB_CAP			USB_H1_VBUS	—	—

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