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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d5eym10acr

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU3Dv4	Graphics Processing Unit, ver. 4	Multimedia Peripherals	The GPU3Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

4.8.1 GPIO Output Buffer Impedance

Table 31 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 31. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 32 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 32. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

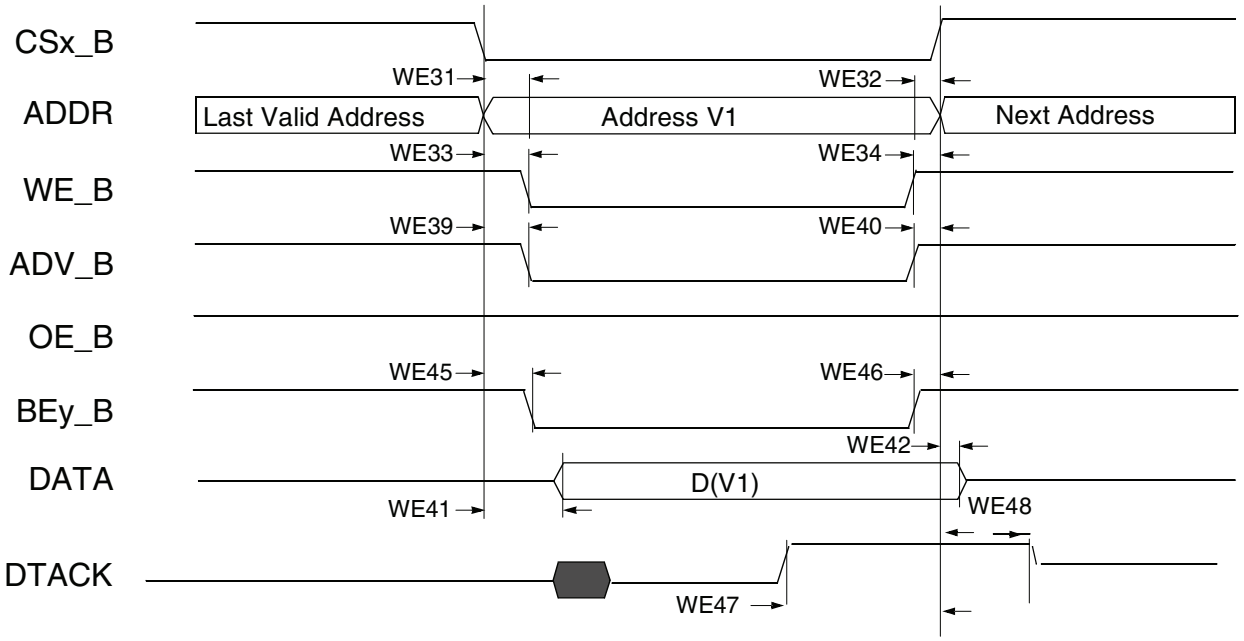

Figure 21. DTACK Write Access (DAP=0)

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A (muxed A/D)	CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+AD H+1-RCSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns

6 In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 22 shows the DDR3/DDR3L basic timing diagram. The timing parameters for this diagram appear in Table 40.

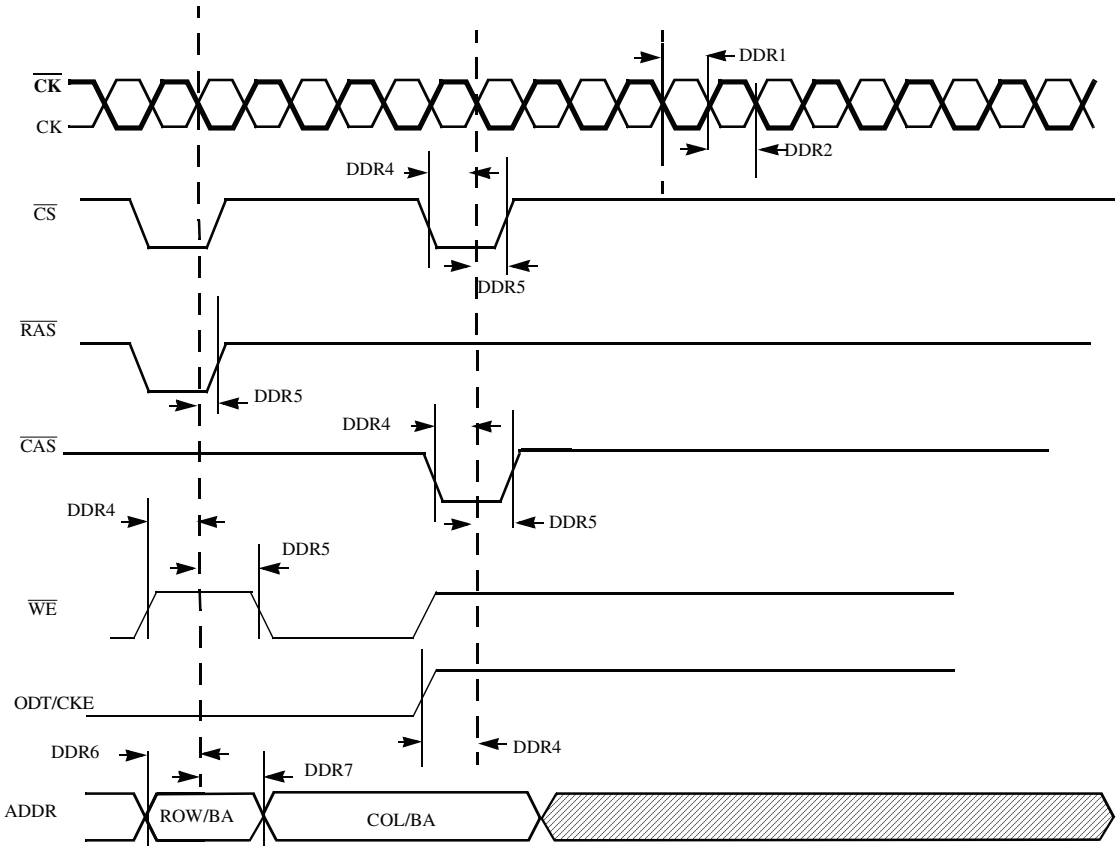

Figure 22. DDR3/DDR3L Command and Address Timing Diagram

Table 40. DDR3/DDR3L Timing Parameter Table

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	t_{CH}	0.47	0.53	t_{CK}
DDR2	CK clock low-level width	t_{CL}	0.47	0.53	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	500	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	400	—	ps

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 28 through Figure 31 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 46 describes the timing parameters (NF1–NF17) that are shown in the figures.

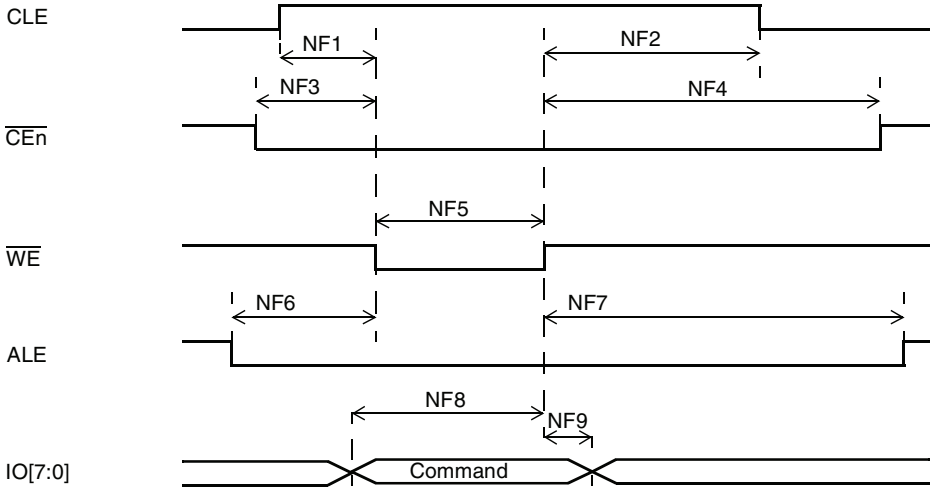

Figure 28. Command Latch Cycle Timing Diagram

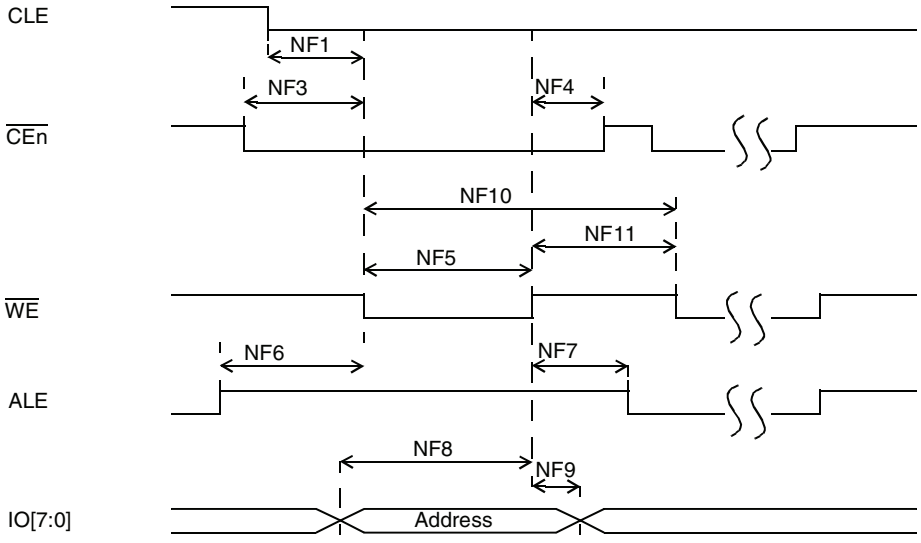

Figure 29. Address Latch Cycle Timing Diagram

4.11.2.2 ECSPI Slave Mode Timing

Figure 40 depicts the timing of ECSPI in slave mode and Table 50 lists the ECSPI slave mode timing characteristics.

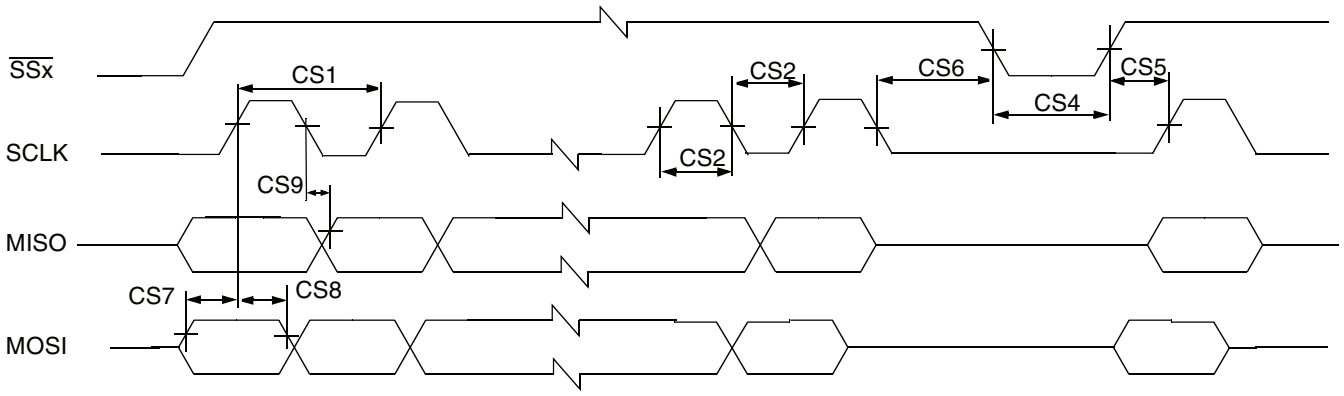

Figure 40. ECSPI Slave Mode Timing Diagram

Table 50. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read • Slow group[1] • Fast group[2] SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	SCLK High or Low Time–Read • Slow group[1] • Fast group[2] SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF) • Slow group[1] • Fast group[2]	t_{PDmiso}	4	 25 17	ns

1 ECSPI slow include:
ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/DISP0_DAT17, ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

2 ECSPI fast include:
ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

Table 54. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5*t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 22, "GPIO I/O DC Parameters," on page 39.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 46 shows MII receive signal timings. Table 55 describes the timing parameters (M1–M4) shown in the figure.

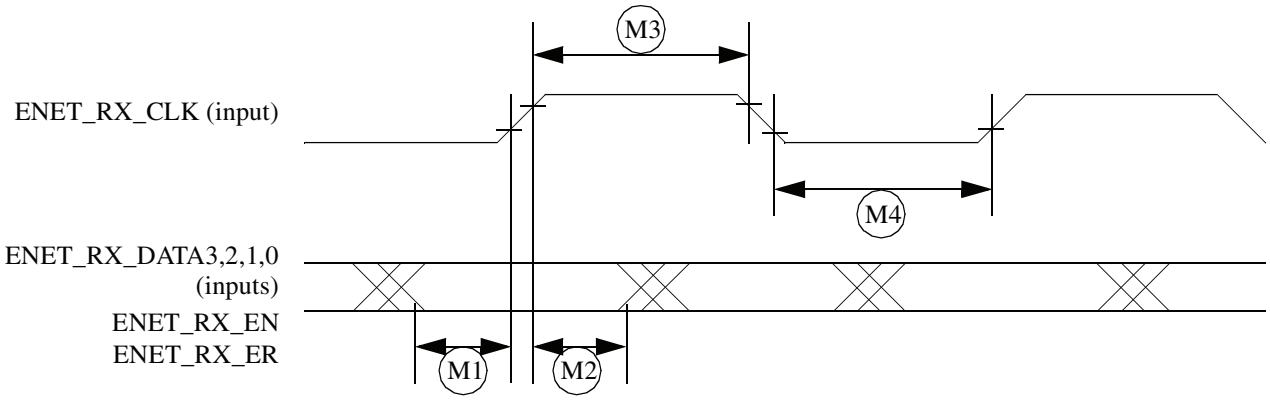

Figure 46. MII Receive Signal Timing Diagram

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 48 shows MII asynchronous input timings. Table 57 describes the timing parameter (M9) shown in the figure.

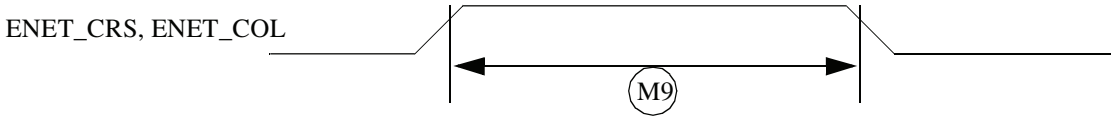

Figure 48. MII Async Inputs Timing Diagram

Table 57. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 49 shows MII asynchronous input timings. Table 58 describes the timing parameters (M10–M15) shown in the figure.

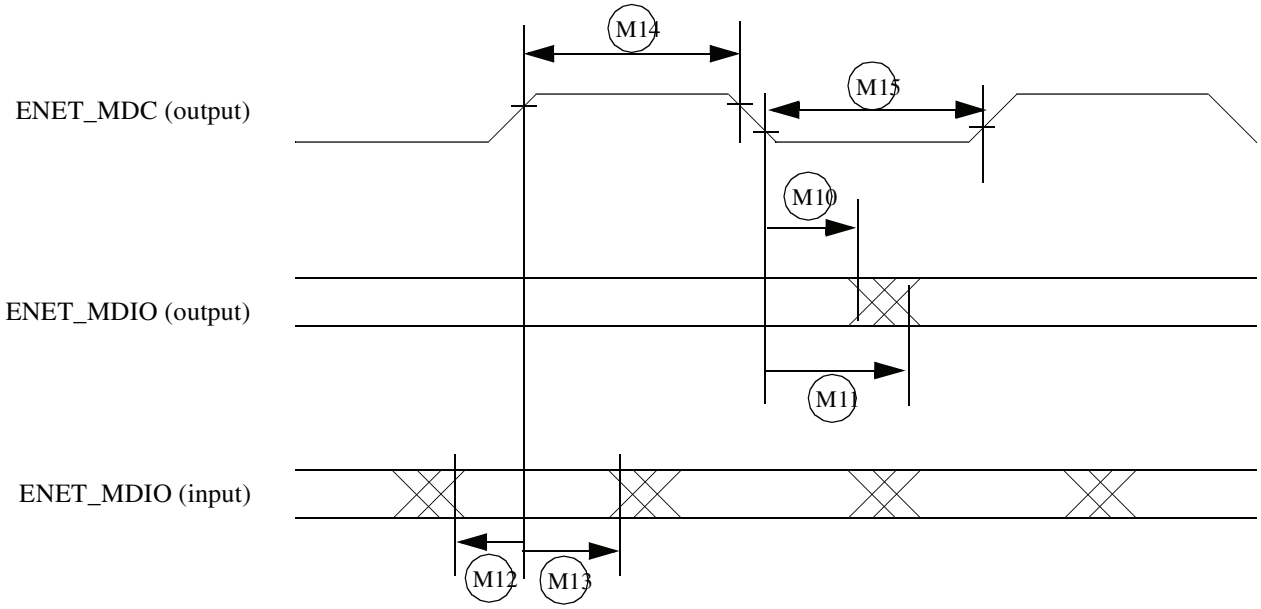

Figure 49. MII Serial Management Channel Timing Diagram

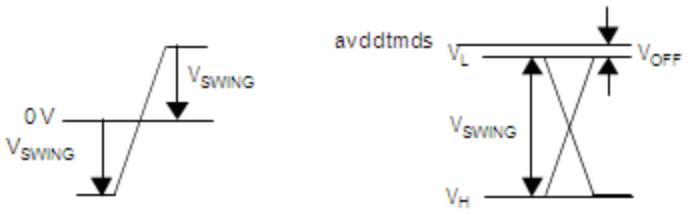

Figure 55. Driver Definitions

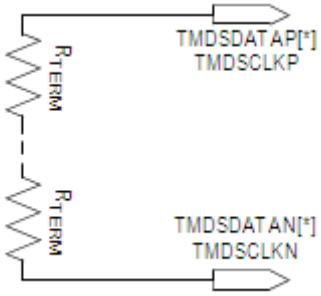

Figure 56. Source Termination

Table 61. Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	-	3.15	3.3	3.45	V
R_T	Termination resistance	-	45	50	55	Ω
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	-	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above.	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds – 200 mV	-	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above.	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds – 600 mV	-	avddtmds – 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds – 700 mV	-	avddtmds – 400 mV	mV

Table 67 shows timing characteristics of signals presented in Figure 68 and Figure 69.

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	Width of second vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$\text{Accuracy} = T_{diclk} \pm 0.62\text{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

Figure 70 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are register-controlled. Table 68 lists the synchronous display interface timing characteristics.

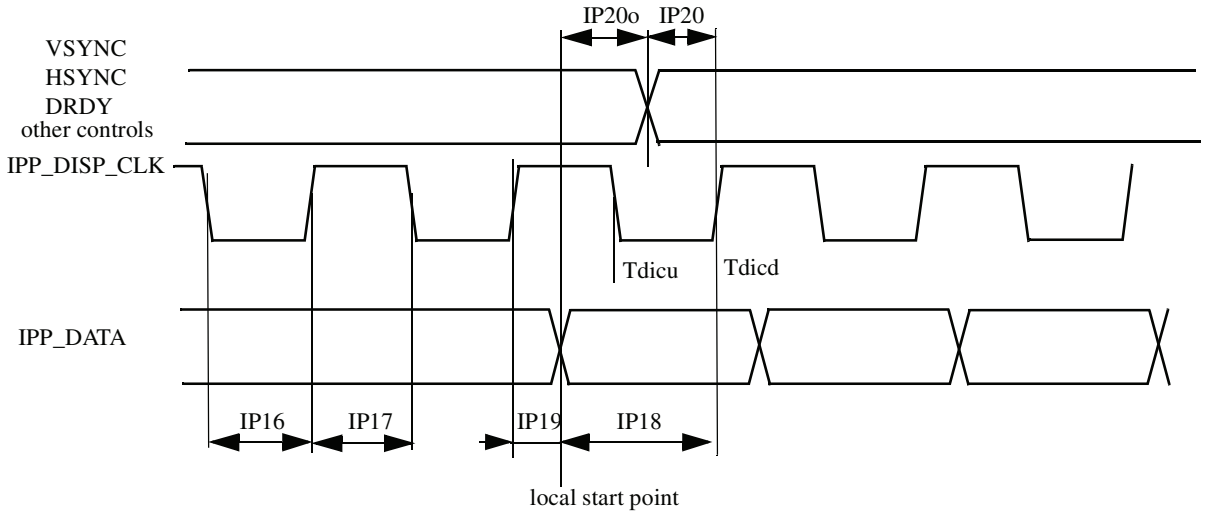

Figure 70. Synchronous Display Interface Timing Diagram—Access Level

Table 68. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defined for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defined for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

Table 71. Electrical and Timing Information

L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

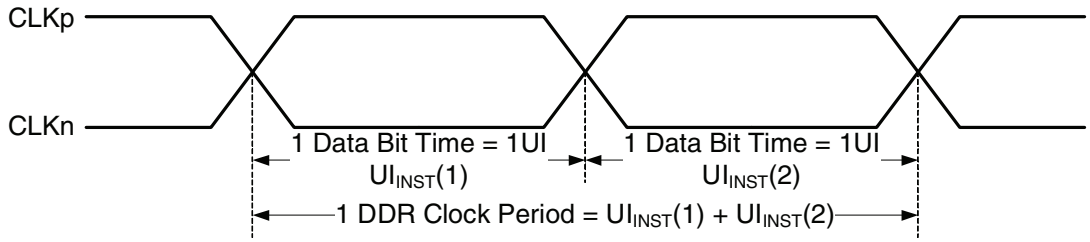

Figure 74. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 75:

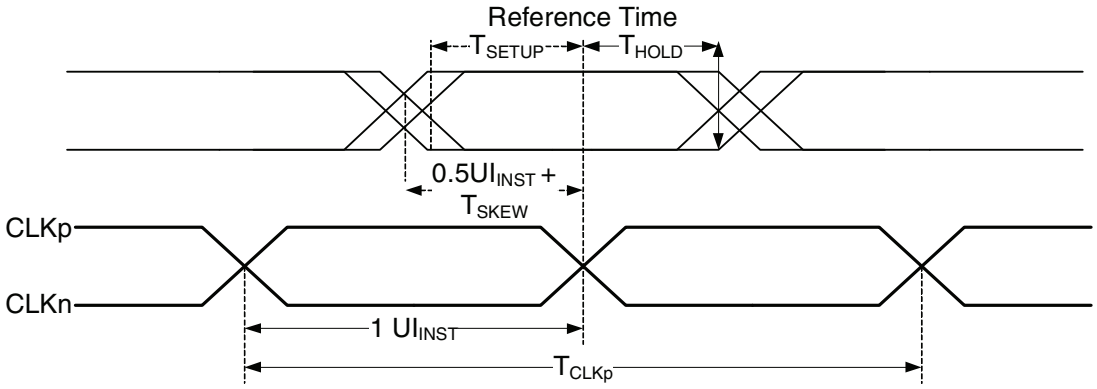

Figure 75. Data to Clock Timing Definitions

4.11.16.1.1 SATA PHY Transmitter Characteristics

Table 74 provides specifications for SATA PHY transmitter characteristics.

Table 74. SATA2 PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.11.16.1.2 SATA PHY Receiver Characteristics

Table 75 provides specifications for SATA PHY receiver characteristics.

Table 75. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	175	—	—	mV
Tolerance	PPM	–400	—	400	ppm

4.11.16.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 87 depicts the SJC test clock input timing. Figure 88 depicts the SJC boundary scan timing. Figure 89 depicts the SJC test access port. Signal parameters are listed in Table 76.

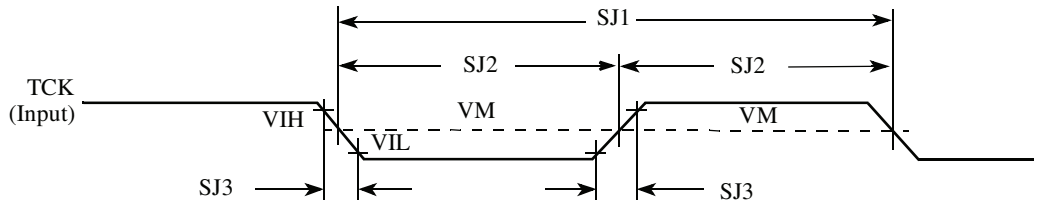

Figure 87. Test Clock Input Timing Diagram

4.11.19 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 78.

Table 78. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX 6Dual/6Quad reference manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as RGMII_TXC.

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 94 depicts the SSI receiver internal clock timing and Table 80 lists the timing parameters for the receiver timing with the internal clock.

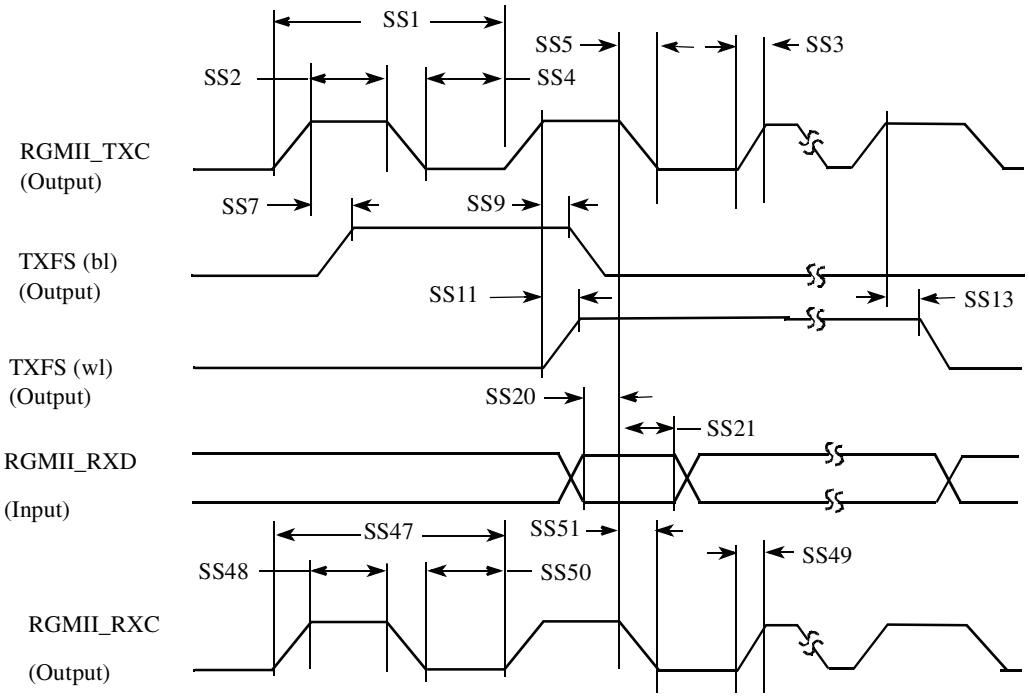

Figure 94. SSI Receiver Internal Clock Timing Diagram

Table 80. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 624 I/O FC PBGA, 21 X 21 PKG, 0.8 MM PITCH, NO LID	CASE NUMBER:	2197–01
	STANDARD:	JEDEC MS–034
	SHEET:	2

Figure 103. 21 x 21 mm Bare Die Package Top, Bottom, and Side Views

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm_PMIC_VSTBY_REQ	Output	0
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src_POR_B	Input	PU (100K)
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[25]	Input	PU (100K)
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[27]	Input	PU (100K)
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[28]	Input	PU (100K)
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[29]	Input	PU (100K)
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[24]	Input	PD (100K)
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[30]	Input	PD (100K)
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[20]	Input	PU (100K)
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[21]	Input	PU (100K)
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[22]	Input	PU (100K)
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[23]	Input	PU (100K)
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[26]	Input	PD (100K)
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[19]	Input	PD (100K)
RTC_XTALI	D9	VDD_SNVS_CAP			RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP			RTC_XTALO	—	—
SATA_RXM	A14	SATA_VPH			SATA_RXM	—	—
SATA_RXP	B14	SATA_VPH			SATA_RXP	—	—
SATA_TXM	B12	SATA_VPH			SATA_TXM	—	—
SATA_TXP	A12	SATA_VPH			SATA_TXP	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[20]	Input	PU (100K)
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[18]	Input	PU (100K)
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[16]	Input	PU (100K)
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[17]	Input	PU (100K)
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[19]	Input	PU (100K)
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[21]	Input	PU (100K)
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[10]	Input	PU (100K)
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[11]	Input	PU (100K)
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[15]	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[14]	Input	PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[13]	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[12]	Input	PU (100K)
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[3]	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[2]	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[4]	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[5]	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[6]	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[7]	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[1]	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[0]	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[18]	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[17]	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[8]	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[10]	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[9]	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[8]	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[9]	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[10]	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[11]	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	gpio2_PIO[12]	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[13]	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[14]	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[15]	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_ SNVS_TD1	Input	PD (100K)
TEST_MODE	E12	VDD_SNVS_IN			Reserved—Factory Use Only	Input	PD (100K)
USB_H1_DN	F10	VDDUSB_CAP			USB_H1_DN	—	—
USB_H1_DP	E10	VDDUSB_CAP			USB_H1_DP	—	—
USB_H1_VBUS	D10	VDDUSB_CAP			USB_H1_VBUS	—	—