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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d5eym10ad

3 Modules List

The i.MX 6Dual/6Quad processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Dual/6Quad Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Dual/6Quad processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	System Control Peripherals	DMA controller used for GPMI2 operation
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of 4x (four) Cortex-A9 cores version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Dual/6Quad processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 33 shows DDR I/O output buffer impedance of i.MX 6Dual/6Quad processors.

Table 33. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			Ω
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Dual/6Quad processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 34 lists the timing parameters.

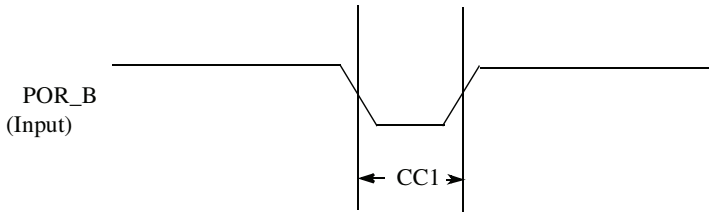

Figure 8. Reset Timing Diagram

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 38 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

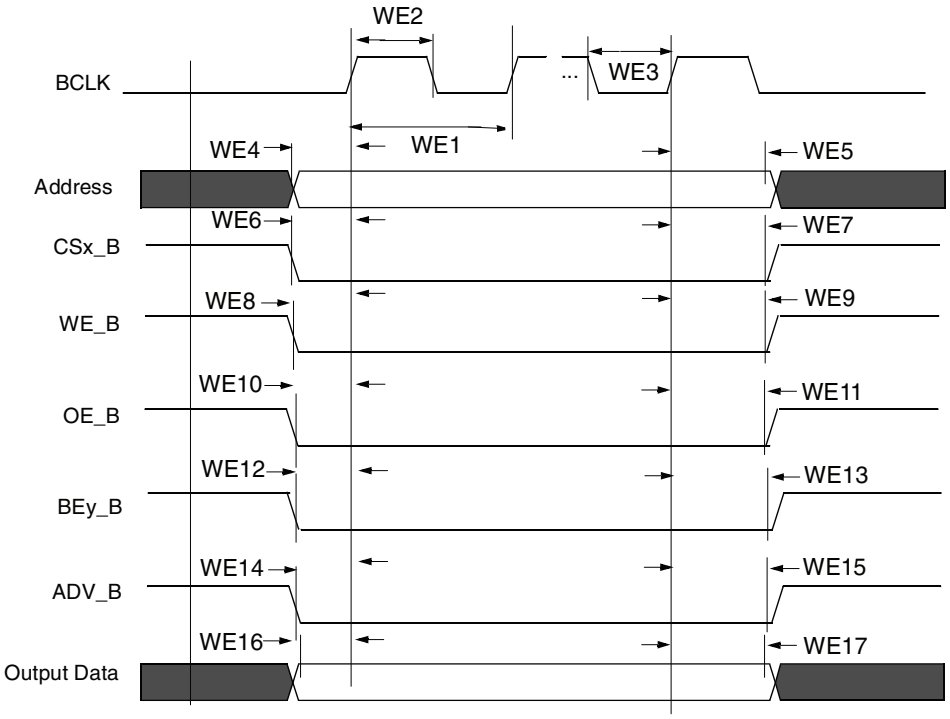

Figure 10. EIM Output Timing Diagram

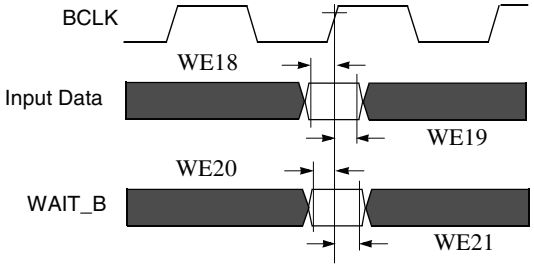

Figure 11. EIM Input Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 38. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	BCLK cycle time[2]	t*(k+1)	—	ns
WE2	BCLK high level width	0.4*t*(k+1)	—	ns

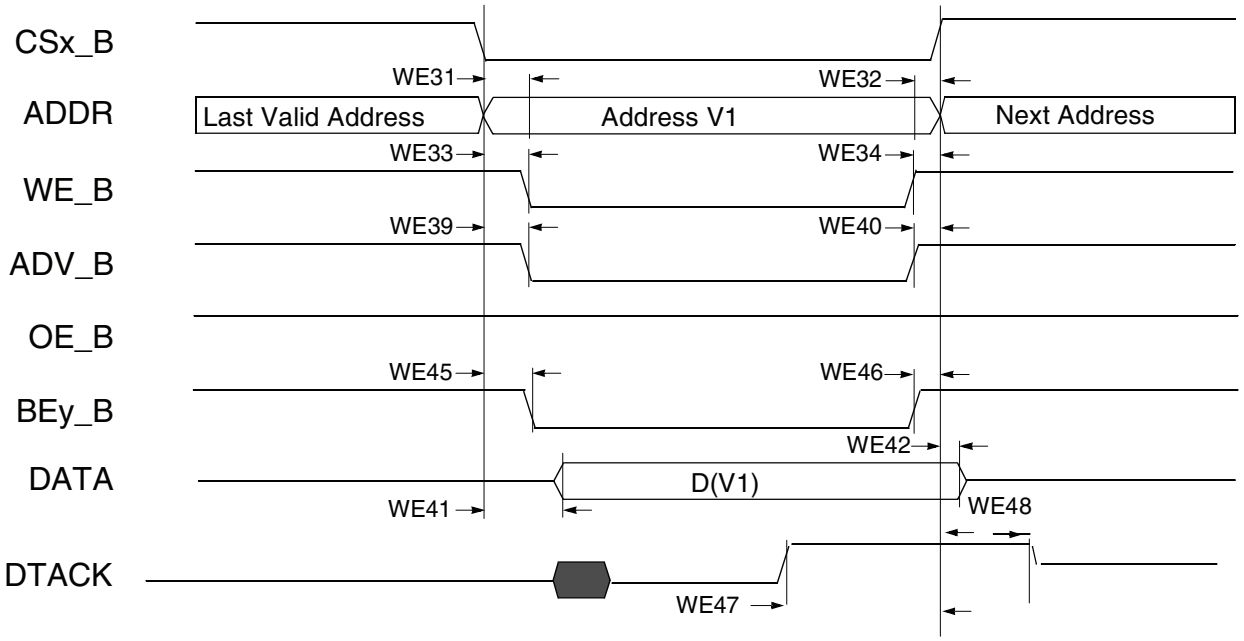

Figure 21. DTACK Write Access (DAP=0)

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A (muxed A/D)	CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+AD H+1-RCSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 43.

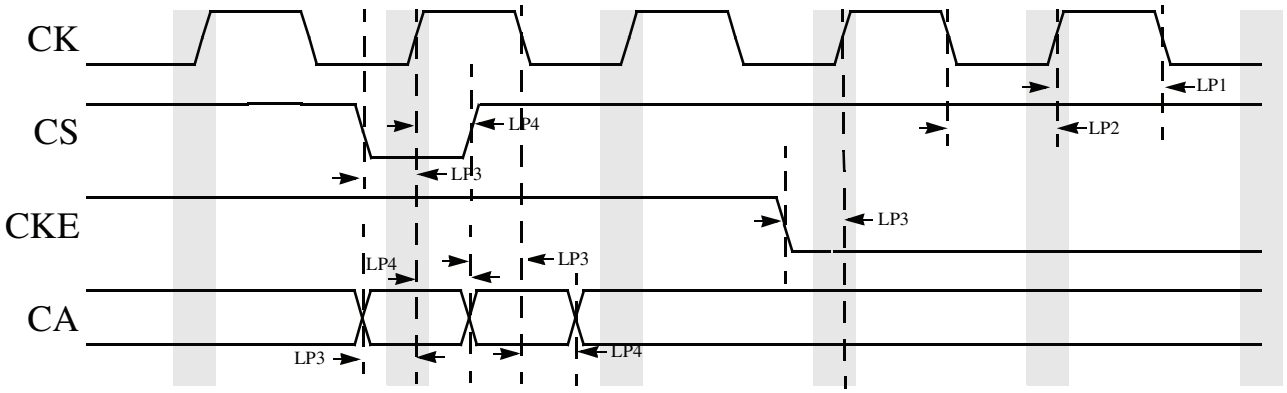

Figure 25. LPDDR2 Command and Address Timing Diagram

Table 43. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	CS, CKE setup time	t_{IS}	270	—	ps
LP4	CS, CKE hold time	t_{IH}	270	—	ps
LP3	CA setup time	t_{IS}	230	—	ps
LP4	CA hold time	t_{IH}	230	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

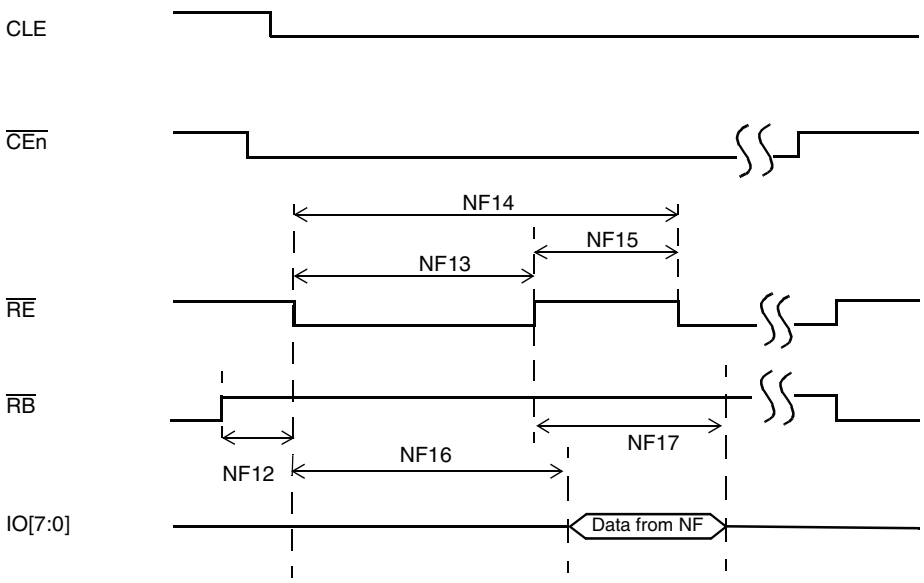

Figure 32. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 46. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T[2] = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS[3]+1)*T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1)*T	—	20	—	ns
NF3	$\overline{\text{CE}}$n setup time	tCS	(AS+1)*T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1)*T	—	20	—	ns
NF5	$\overline{\text{WE}}$ pulse width	tWP	DS*T		10		ns
NF6	ALE setup time	tALS	(AS+1)*T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1)*T	—	20	—	ns
NF8	Data setup time	tDS	DS*T	—	10	—	ns
NF9	Data hold time	tDH	DH*T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH)*T		20		ns
NF11	$\overline{\text{WE}}$ hold time	tWH	DH*T		10		ns
NF12	Ready to $\overline{\text{RE}}$ low	tRR	(AS+1)*T	—	10	—	ns
NF13	$\overline{\text{RE}}$ pulse width	tRP	DS*T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH)*T	—	20	—	ns
NF15	$\overline{\text{RE}}$ high hold time	tREH	DH*T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

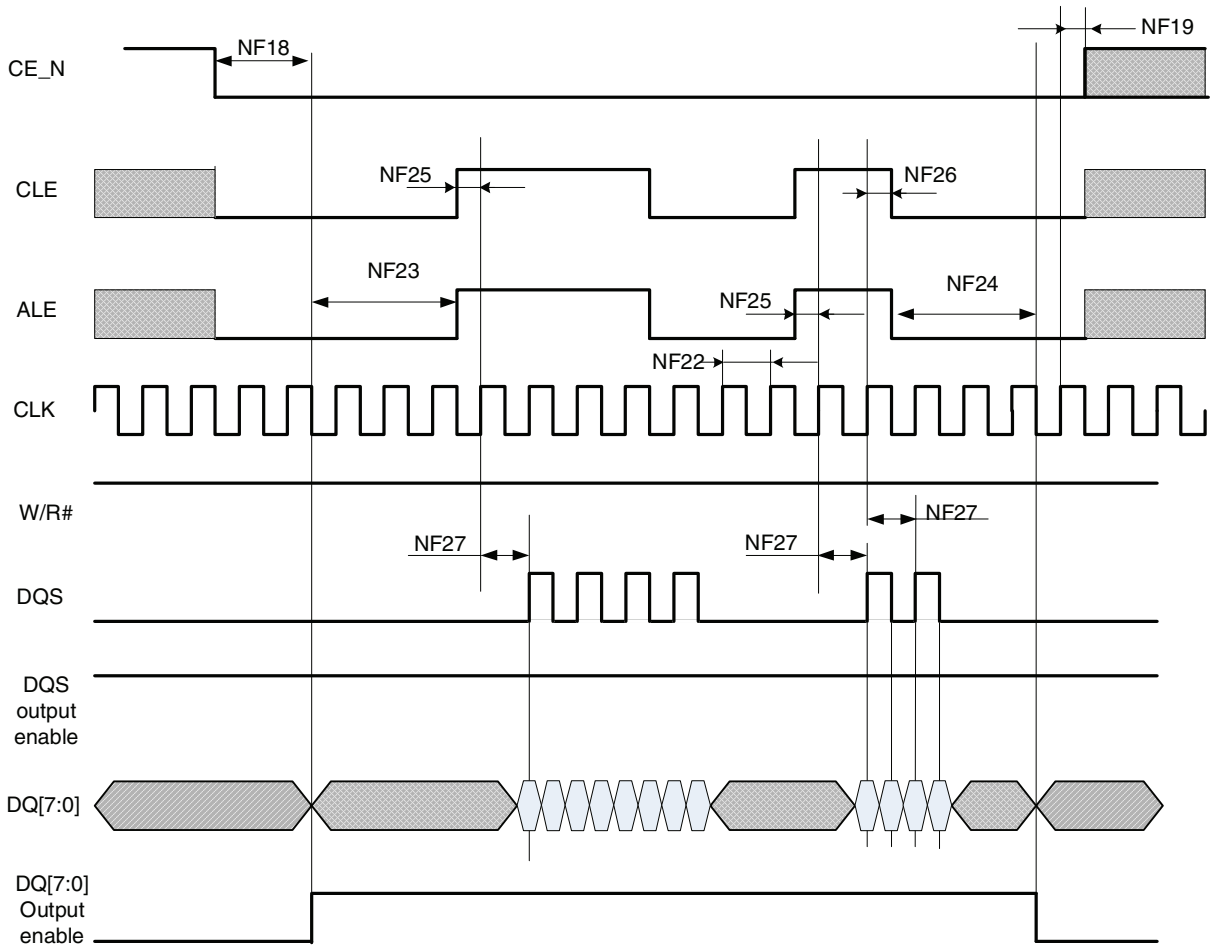

Figure 34. Source Synchronous Mode Data Write Timing Diagram

Table 47. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

[1] GPMI's Source sync mode output timing could be controlled by module's internal register, say GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

Figure 36 shows the timing diagram of DQS/DQ read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 43 depicts the timing of SD/eMMC4.3, and Table 52 lists the SD/eMMC4.3 timing characteristics.

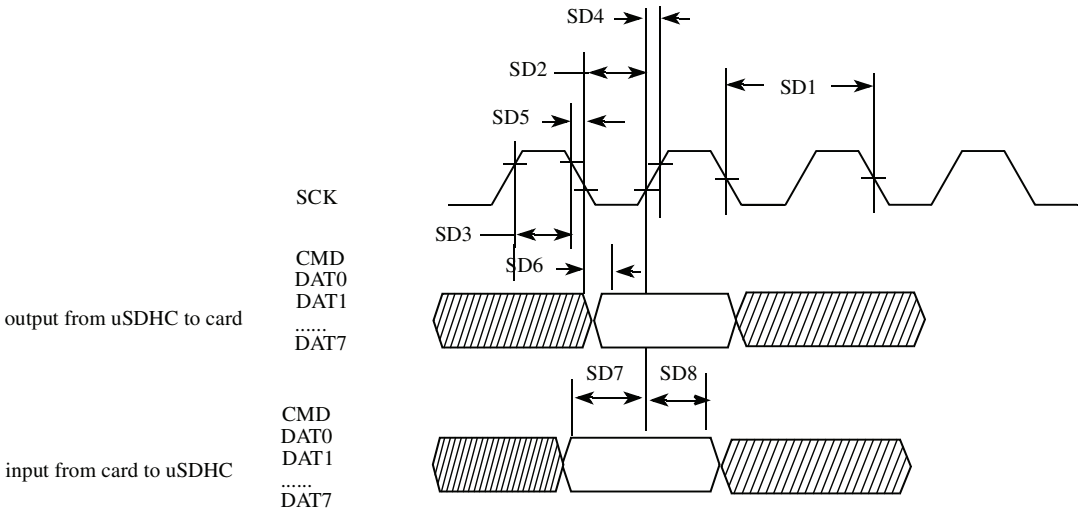

Figure 43. SD/eMMC4.3 Timing

Table 52. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

Table 66. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment[1]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
DIx_DISP_CLK	PixCLK							—
DIx_PIN1	—							May be required for anti-tearing
DIx_PIN2	HSYNC							—
DIx_PIN3	VSYNC							VSYNC out
DIx_PIN4	—							Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—							
DIx_PIN6	—							
DIx_PIN7	—							
DIx_PIN8	—							
DIx_D0_CS	—							—
DIx_D1_CS	—							Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—							—
DIx_PIN12	—							—
DIx_PIN13	—							Register select signal
DIx_PIN14	—							Optional RS2
DIx_PIN15	DRDY/DV							Data validation/blank, data enable
DIx_PIN16	—							Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q							

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 68 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

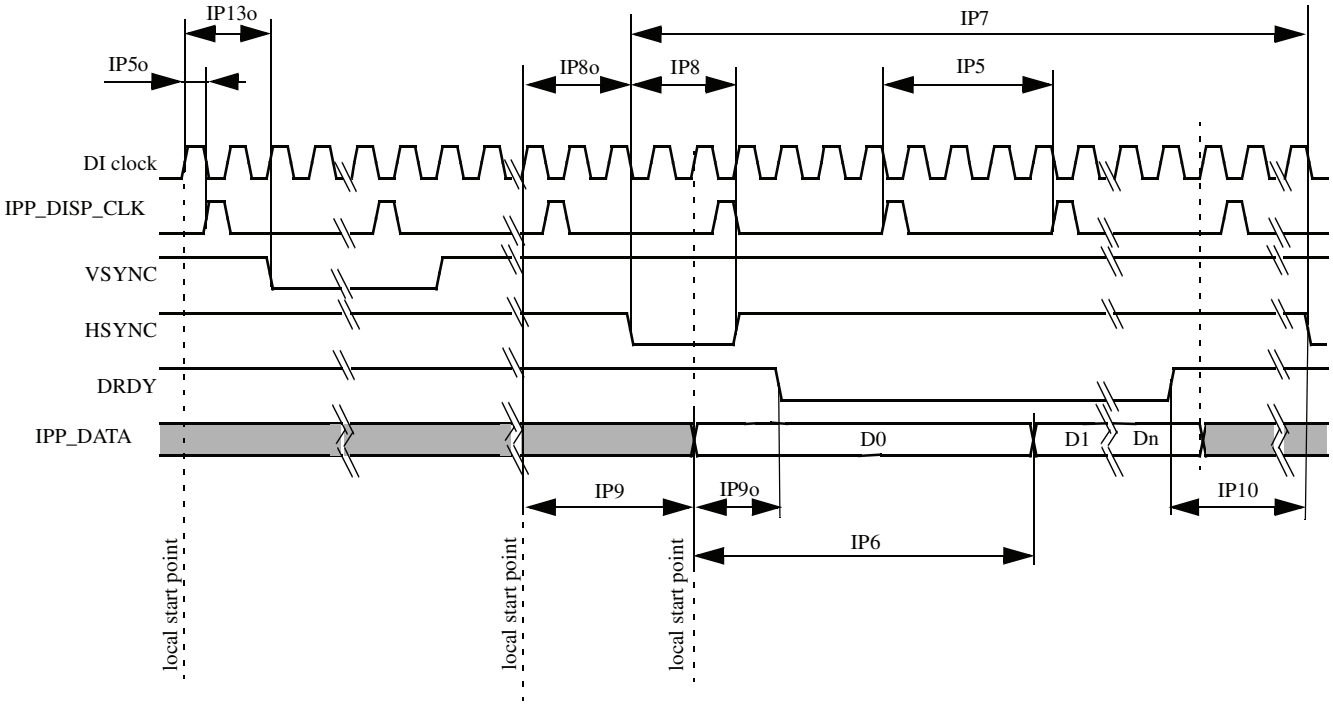

Figure 68. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 69 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

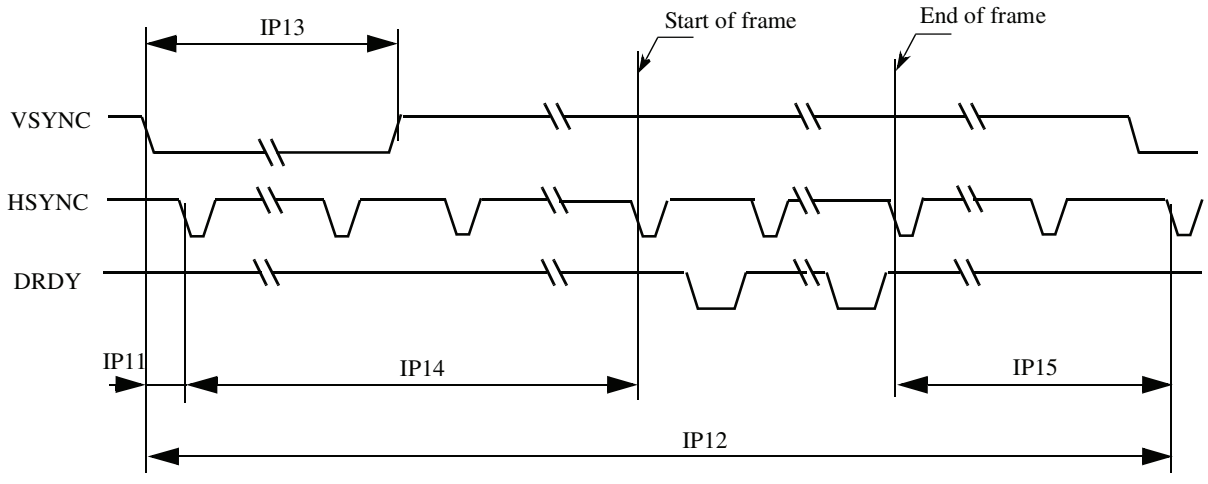

Figure 69. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 67 shows timing characteristics of signals presented in Figure 68 and Figure 69.

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	Width of second vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

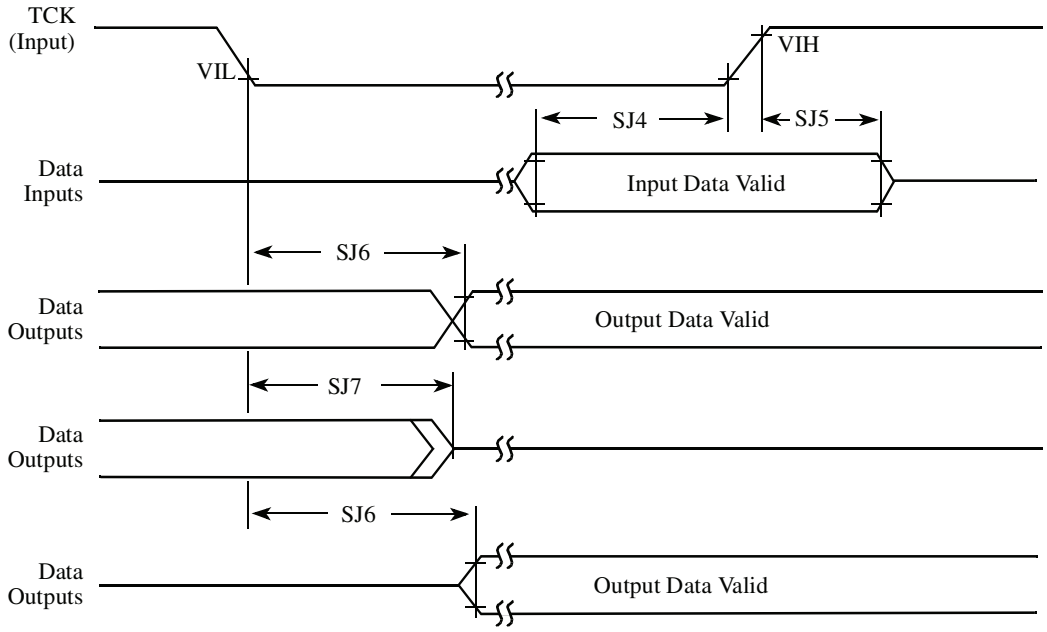

Figure 88. Boundary Scan (JTAG) Timing Diagram

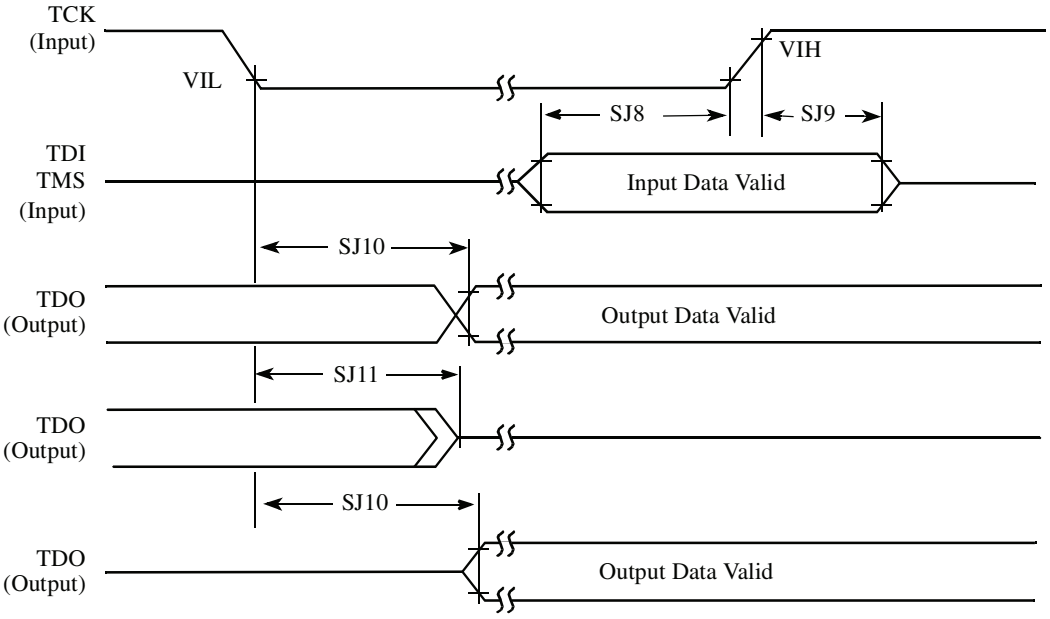

Figure 89. Test Access Port Timing Diagram

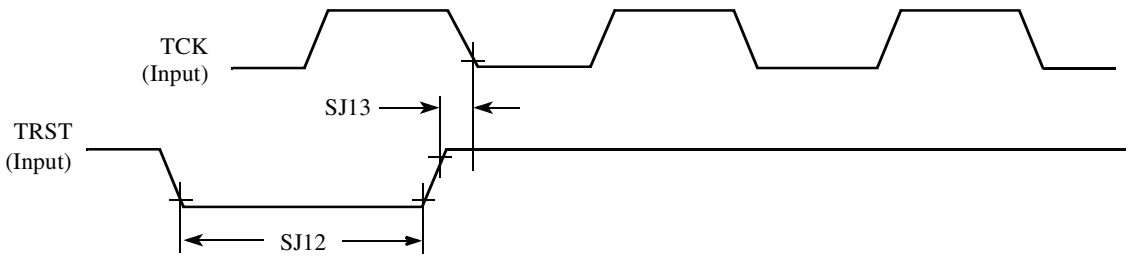

Figure 90. $\overline{\text{TRST}}$ Timing Diagram

Table 76. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.11.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 77 and Figure 91 and Figure 92 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.20 UART I/O Configuration and Timing Parameters

4.11.20.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Dual/6Quad UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 83 shows the UART I/O configuration based on the enabled mode.

Table 83. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 90 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Dual/6Quad Fuse Map document and the System Boot chapter of the i.MX 6Dual/6Quad reference manual.

Table 90. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	Boot Mode Selection	Boot Mode selection
BOOT_MODE0	Input	Boot Mode Selection	Boot Mode Selection

Table 90. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
EIM_DA0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_DA1	Input	BOOT_CFG1[1]	
EIM_DA2	Input	BOOT_CFG1[2]	
EIM_DA3	Input	BOOT_CFG1[3]	
EIM_DA4	Input	BOOT_CFG1[4]	
EIM_DA5	Input	BOOT_CFG1[5]	
EIM_DA6	Input	BOOT_CFG1[6]	
EIM_DA7	Input	BOOT_CFG1[7]	
EIM_DA8	Input	BOOT_CFG2[0]	
EIM_DA9	Input	BOOT_CFG2[1]	
EIM_DA10	Input	BOOT_CFG2[2]	
EIM_DA11	Input	BOOT_CFG2[3]	
EIM_DA12	Input	BOOT_CFG2[4]	
EIM_DA13	Input	BOOT_CFG2[5]	
EIM_DA14	Input	BOOT_CFG2[6]	
EIM_DA15	Input	BOOT_CFG2[7]	
EIM_A16	Input	BOOT_CFG3[0]	
EIM_A17	Input	BOOT_CFG3[1]	
EIM_A18	Input	BOOT_CFG3[2]	
EIM_A19	Input	BOOT_CFG3[3]	
EIM_A20	Input	BOOT_CFG3[4]	
EIM_A21	Input	BOOT_CFG3[5]	
EIM_A22	Input	BOOT_CFG3[6]	
EIM_A23	Input	BOOT_CFG3[7]	
EIM_A24	Input	BOOT_CFG4[0]	
EIM_WAIT	Input	BOOT_CFG4[1]	
EIM_LBA	Input	BOOT_CFG4[2]	
EIM_EB0	Input	BOOT_CFG4[3]	
EIM_EB1	Input	BOOT_CFG4[4]	
EIM_RW	Input	BOOT_CFG4[5]	
EIM_EB2	Input	BOOT_CFG4[6]	
EIM_EB3	Input	BOOT_CFG4[7]	

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm_PMIC_VSTBY_REQ	Output	0
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src_POR_B	Input	PU (100K)
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[25]	Input	PU (100K)
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[27]	Input	PU (100K)
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[28]	Input	PU (100K)
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[29]	Input	PU (100K)
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[24]	Input	PD (100K)
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[30]	Input	PD (100K)
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[20]	Input	PU (100K)
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[21]	Input	PU (100K)
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[22]	Input	PU (100K)
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[23]	Input	PU (100K)
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[26]	Input	PD (100K)
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[19]	Input	PD (100K)
RTC_XTALI	D9	VDD_SNVS_CAP			RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP			RTC_XTALO	—	—
SATA_RXM	A14	SATA_VPH			SATA_RXM	—	—
SATA_RXP	B14	SATA_VPH			SATA_RXP	—	—
SATA_TXM	B12	SATA_VPH			SATA_TXM	—	—
SATA_TXP	A12	SATA_VPH			SATA_TXP	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[20]	Input	PU (100K)
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[18]	Input	PU (100K)
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[16]	Input	PU (100K)
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[17]	Input	PU (100K)
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[19]	Input	PU (100K)
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[21]	Input	PU (100K)
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[10]	Input	PU (100K)
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[11]	Input	PU (100K)
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[15]	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[14]	Input	PU (100K)

Table 95. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

H	G	F	E	D	C	B
DSI_D1P	DSI_D0P	CSI_D3P	CSI_D2M	CSI_D1M	GND	PCIE_RXM
DSI_D1M	DSI_D0M	CSI_D3M	CSI_D2P	CSI_D1P	JTAG_TRSTB	PCIE_RXP
DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P	GND	JTAG_TMS	PCIE_TXP
DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M	CSI_REXT	GND	GND
JTAG_TCK	JTAG_TDI	GND	GND	CLK2_P	CLK2_N	VDD_FA
JTAG_MOD	JTAG_TDO	GND	GND	GND	GND	USB_OTG_DN
PCIE_VP	PCIE_VPH	GND	GND	CLK1_P	CLK1_N	XTALO
GND	PCIE_VPTX	GND	NVCC_PLL_OUT	GND	GPANAIO	USB_OTG_CHD_B
VDDHIGH_IN	VDD_SNVS_CAP	VDDUSB_CAP	USB_OTG_VBUS	RTC_XTALI	RTC_XTALO	MLB_SP[1]
VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP	USB_H1_VBUS	GND	MLB_DN[1]
VDDARM23_CAP	VDD_SNVS_IN	PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ	POR_B	MLB_CP[1]
GND	SATA_VPH	BOOT_MODE1	TEST_MODE	ONOFF	BOOT_MODE0	SATA_TXM
VDDARM_CAP	SATA_VP	SD3_DAT7	SD3_DAT6	SD3_DAT4	SD3_DAT5	SD3_CMD
VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0	SD3_CLK	SATA_REXT	SATA_RXP
GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B	SD3_RST	NANDF_CLE	SD3_DAT3
VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK	NANDF_CS3	NANDF_CS1	NANDF_RB0
VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6	NANDF_D3	NANDF_D1	SD4_CMD
GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4	SD4_DAT0	NANDF_D7	NANDF_D5
EIM_A25	GND	SD2_CMD	SD1_DAT2	SD4_DAT7	SD4_DAT5	SD4_DAT1
EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1	SD1_CLK	SD1_DAT1	SD4_DAT6
EIM_D31	EIM_D19	EIM_D17	RGMII_TD2	RGMII_TXC	SD2_CLK	SD1_CMD
EIM_A20	EIM_D25	EIM_D24	EIM_EB2	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3
EIM_A21	EIM_D28	EIM_EB3	EIM_D22	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1
EIM_CS0	EIM_A17	EIM_A22	EIM_D26	EIM_D18	RGMII_RD0	RGMII_RD2
EIM_A16	EIM_A19	EIM_A24	EIM_D27	EIM_D23	EIM_D16	RGMII_RXC