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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q5eym10ac

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 7, "Operating Ranges," on page 23
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LVDDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6Dual/6Quad specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC-level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card Detection” and “Write Protection” pads and do not support hardware reset. • Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
VDOA	VDOA	Multimedia Peripherals	The Video Data Order Adapter (VDOA) is used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.MX 6Dual/6Quad reference manual for complete list of VPU’s decoding/encoding capabilities.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.

[2] Per JEDEC JESD51-3 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

[3] Per JEDEC JESD51-6 with the board horizontal.

[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Table 10. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_DRAM	—	—[4]	
NVCC_ENET	N=10	Use maximal IO equation[5]	
NVCC_LCD	N=29	Use maximal IO equation[5]	
NVCC_GPIO	N=24	Use maximal IO equation[5]	
NVCC_CSI	N=20	Use maximal IO equation[5]	
NVCC_EIM0	N=19	Use maximal IO equation[5]	
NVCC_EIM1	N=14	Use maximal IO equation[5]	
NVCC_EIM2	N=20	Use maximal IO equation[5]	
NVCC_JTAG	N=6	Use maximal IO equation[5]	
NVCC_RGMII	N=12	Use maximal IO equation[5]	
NVCC_SD1	N=6	Use maximal IO equation[5]	
NVCC_SD2	N=6	Use maximal IO equation[5]	
NVCC_SD3	N=11	Use maximal IO equation[5]	
NVCC_NANDF	N=26	Use maximal IO equation[5]	
NVCC_MIPI	—	25.5	mA
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS2P5, NVCC_MIPI, or HDMI, PCIe, and SATA VPH supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination.
See the i.MX 6Dual/6Quad Power Consumption Measurement Application Note (AN4509) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximal power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

- When the SATA interface is not used, the SATA_VP and SATA_VPH supplies should be grounded. The input and output supplies for rest of the ports (SATA_REFCLKM, SATA_REFCLKP, SATA_REXT, SATA_RXM, SATA_RXP, and SATA_TXM) can be left floating. It is recommended not to turn OFF the SATA_VPH supply while the SATA_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, SATA_VP and SATA_VPH must remain powered.
- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RXM, PCIE_RXP, PCIE_TXM, and PCIE_TXP) can be left floating. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6Dual/6Quad reference manual for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see Table 7 for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDDHIGH_IN (see Table 7 for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 2.25V or 2.75V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the

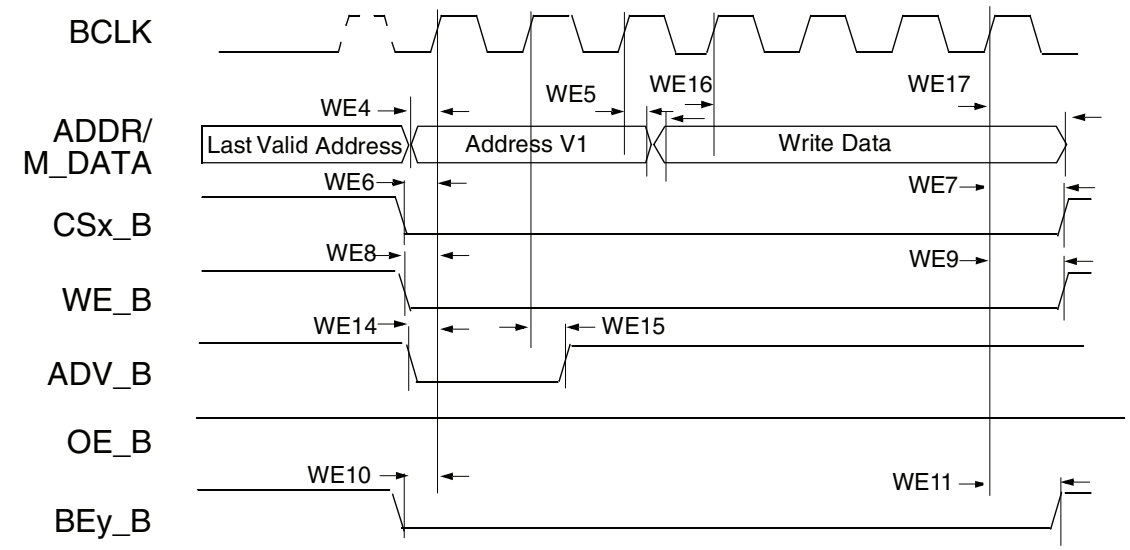

Figure 14. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

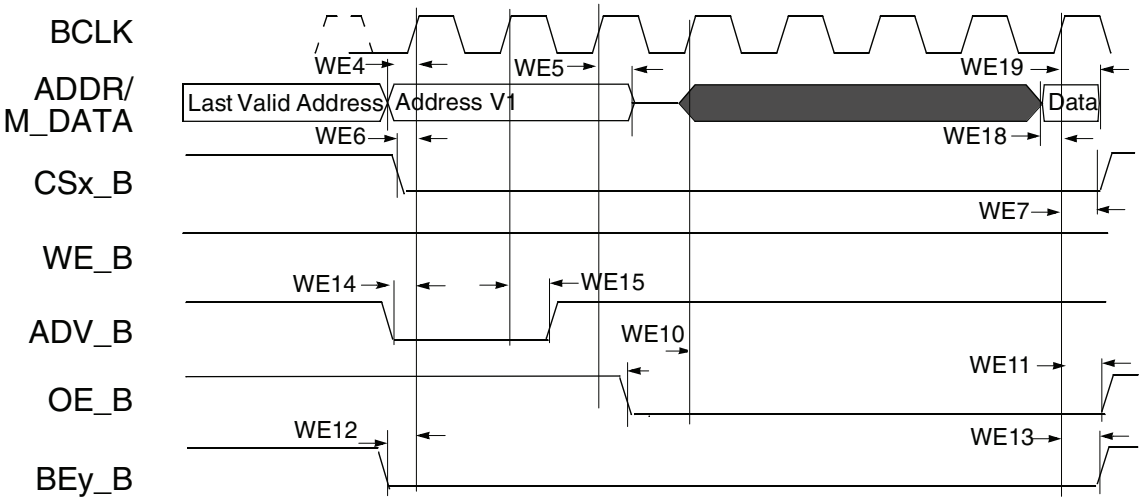

Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 43.

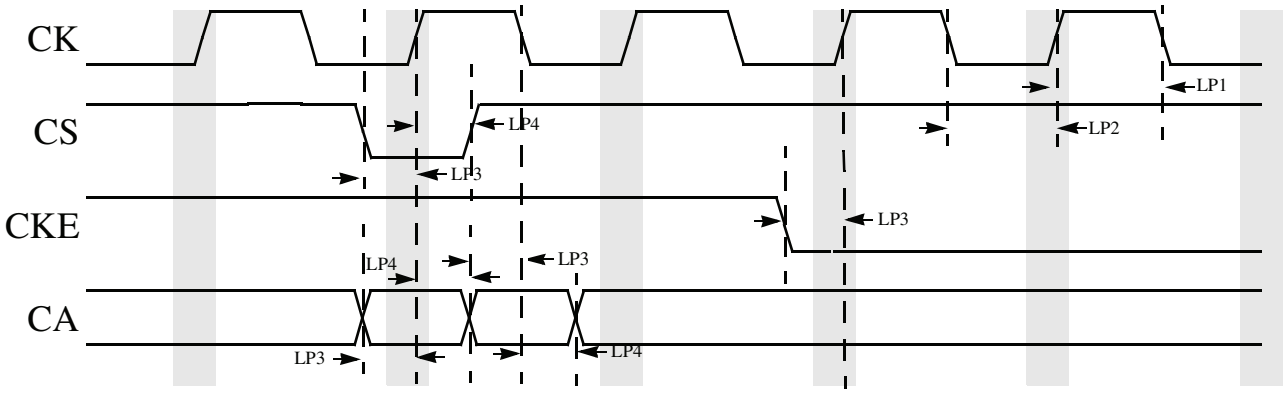

Figure 25. LPDDR2 Command and Address Timing Diagram

Table 43. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	CS, CKE setup time	t_{IS}	270	—	ps
LP4	CS, CKE hold time	t_{IH}	270	—	ps
LP3	CA setup time	t_{IS}	230	—	ps
LP4	CA hold time	t_{IH}	230	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Table 47. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

[1] GPMI's Source sync mode output timing could be controlled by module's internal register, say GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

Figure 36 shows the timing diagram of DQS/DQ read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

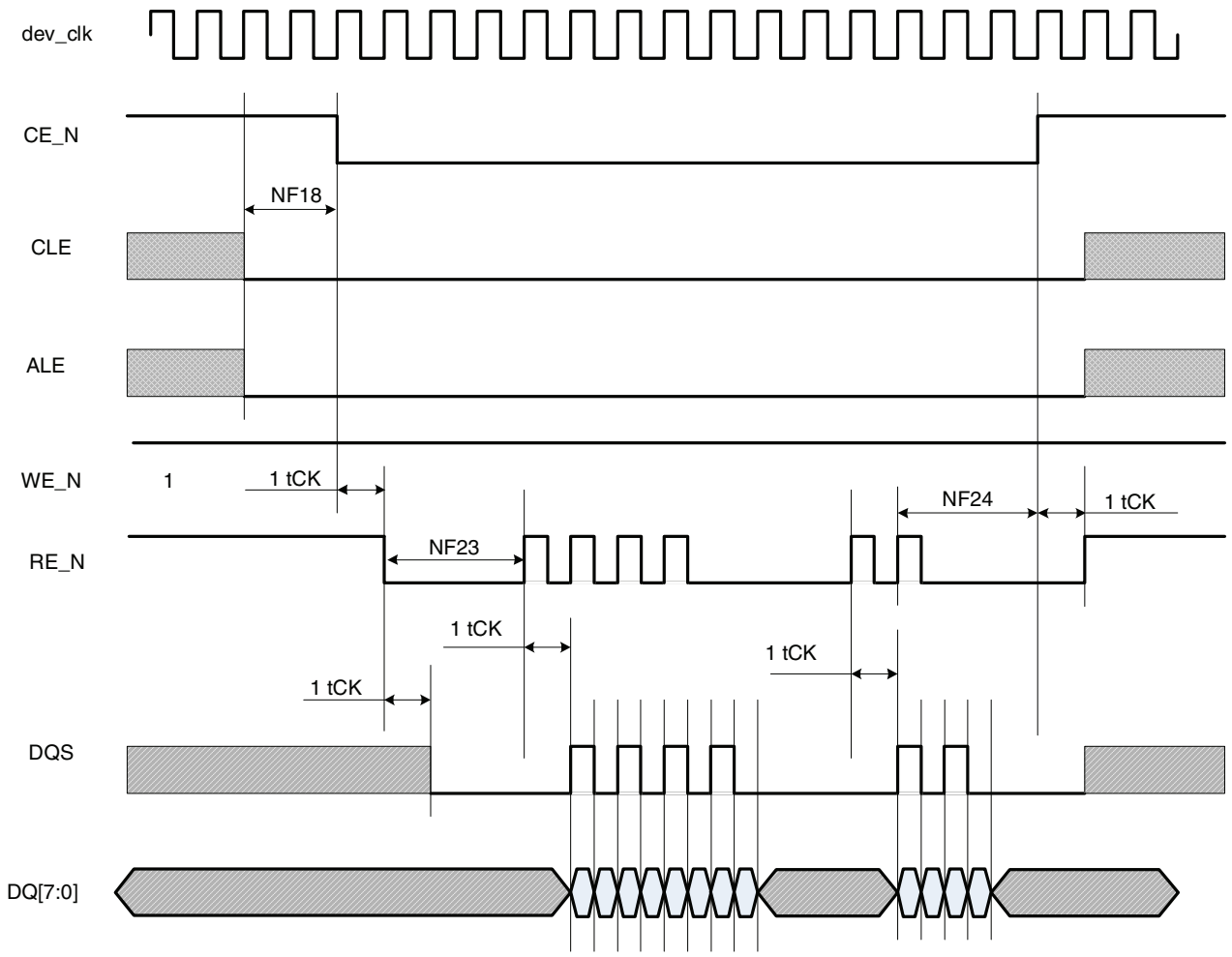

Figure 38. Samsung Toggle Mode Data Read Timing

Table 48. Samsung Toggle Mode Timing Parameters

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	7.5	--	ns
NF23	preamble delay	tPRE	(PRE_DELAY+1)*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns

4.11.13.5 Stream Transmission Mode Frame Transfer

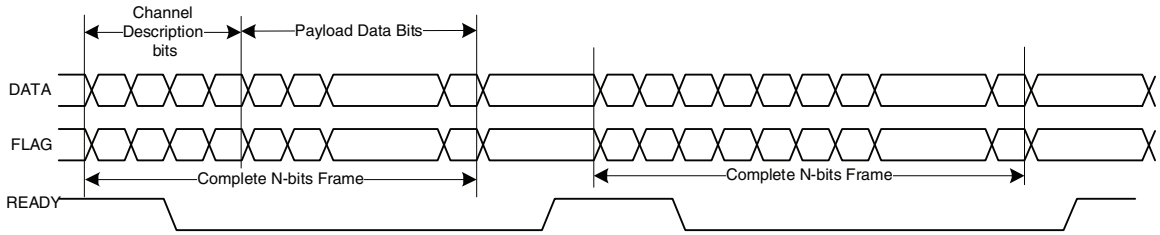

Figure 82. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

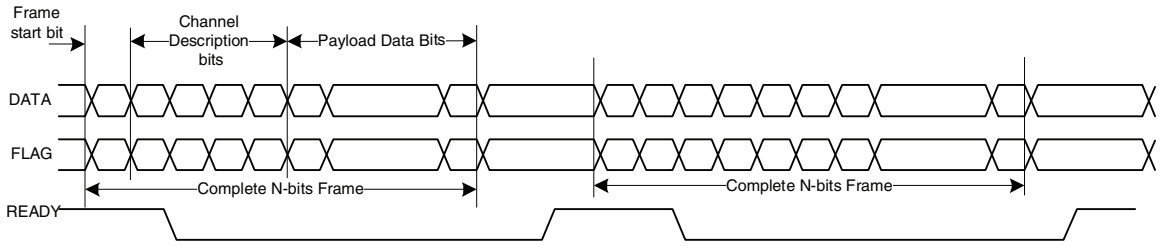

Figure 83. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

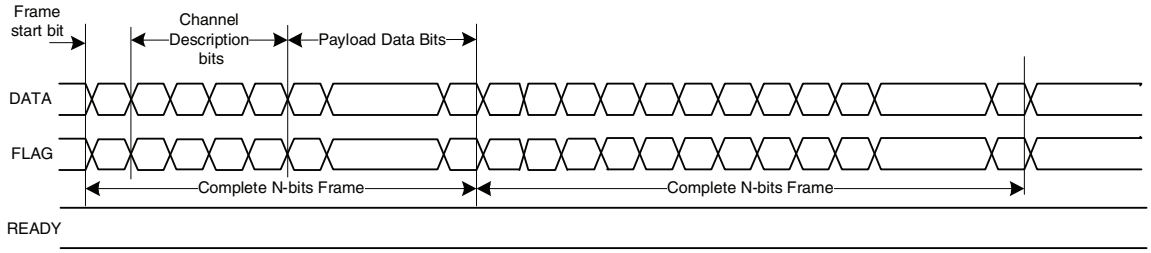

Figure 84. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 72. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2 ns	2 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50 ns	0.5 ns

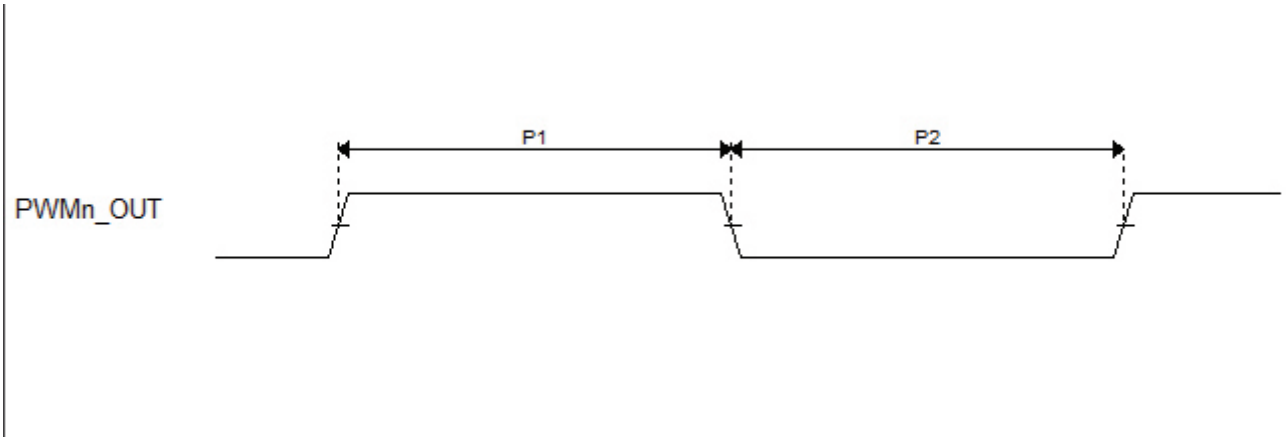

Figure 86. PWM Timing

Table 73. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15		ns
P2	PWM output pulse width low	15		ns

4.11.16 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.11.16.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

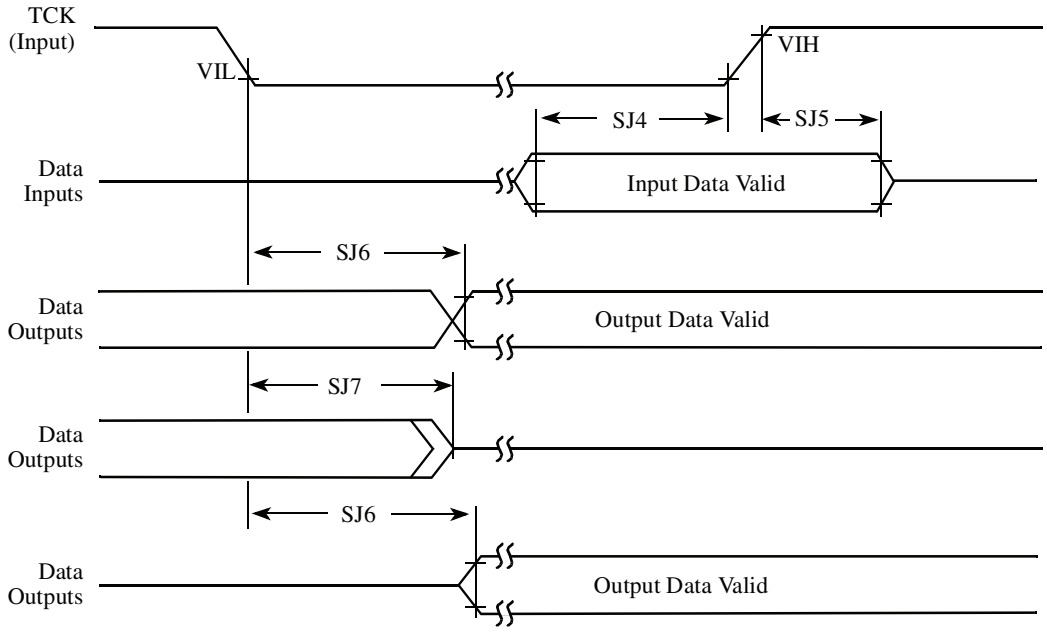

Figure 88. Boundary Scan (JTAG) Timing Diagram

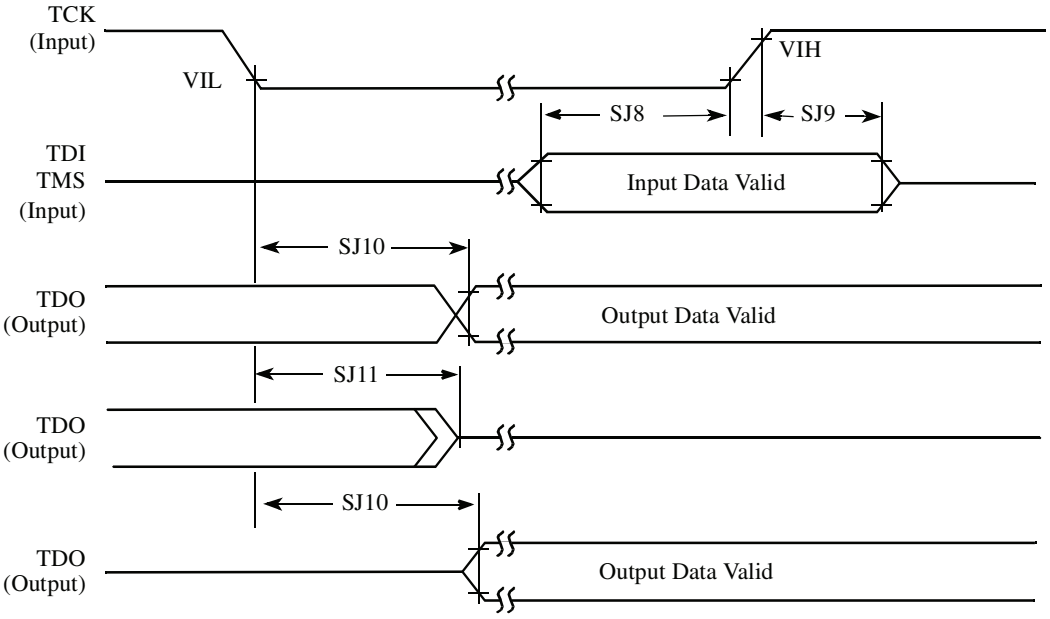

Figure 89. Test Access Port Timing Diagram

Table 80. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.3 SSI Transmitter Timing with External Clock

Figure 95 depicts the SSI transmitter external clock timing and Table 81 lists the timing parameters for the transmitter timing with the external clock.

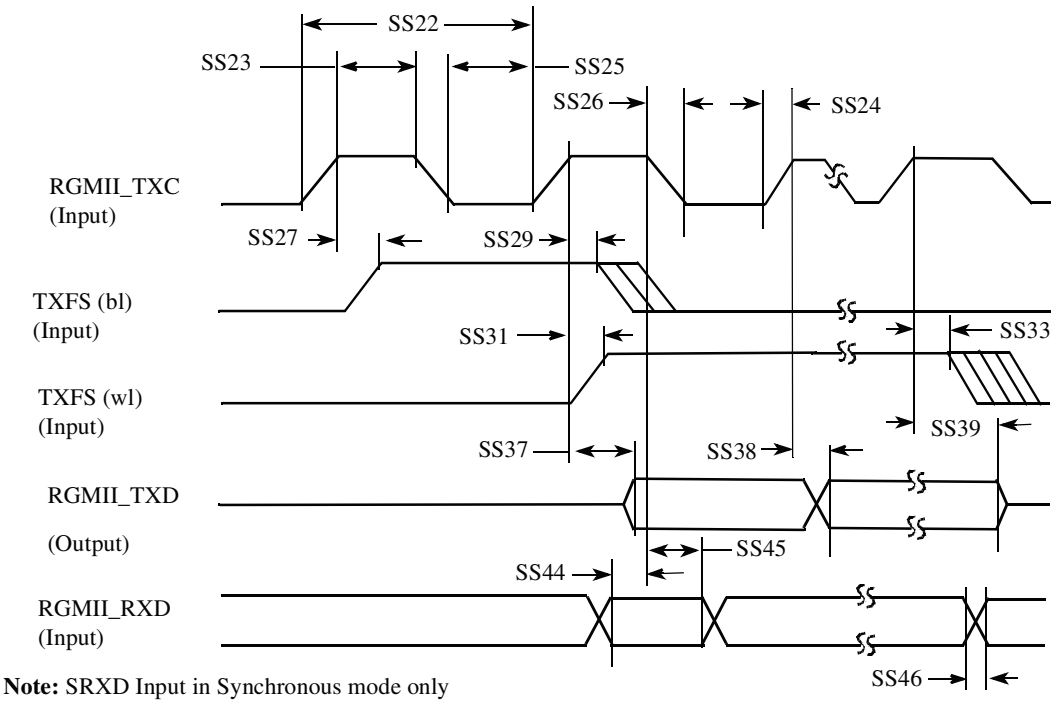

Figure 95. SSI Transmitter External Clock Timing Diagram

Table 81. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Figure 103 shows the top, bottom, and side views of the 21 × 21 mm bare die package.

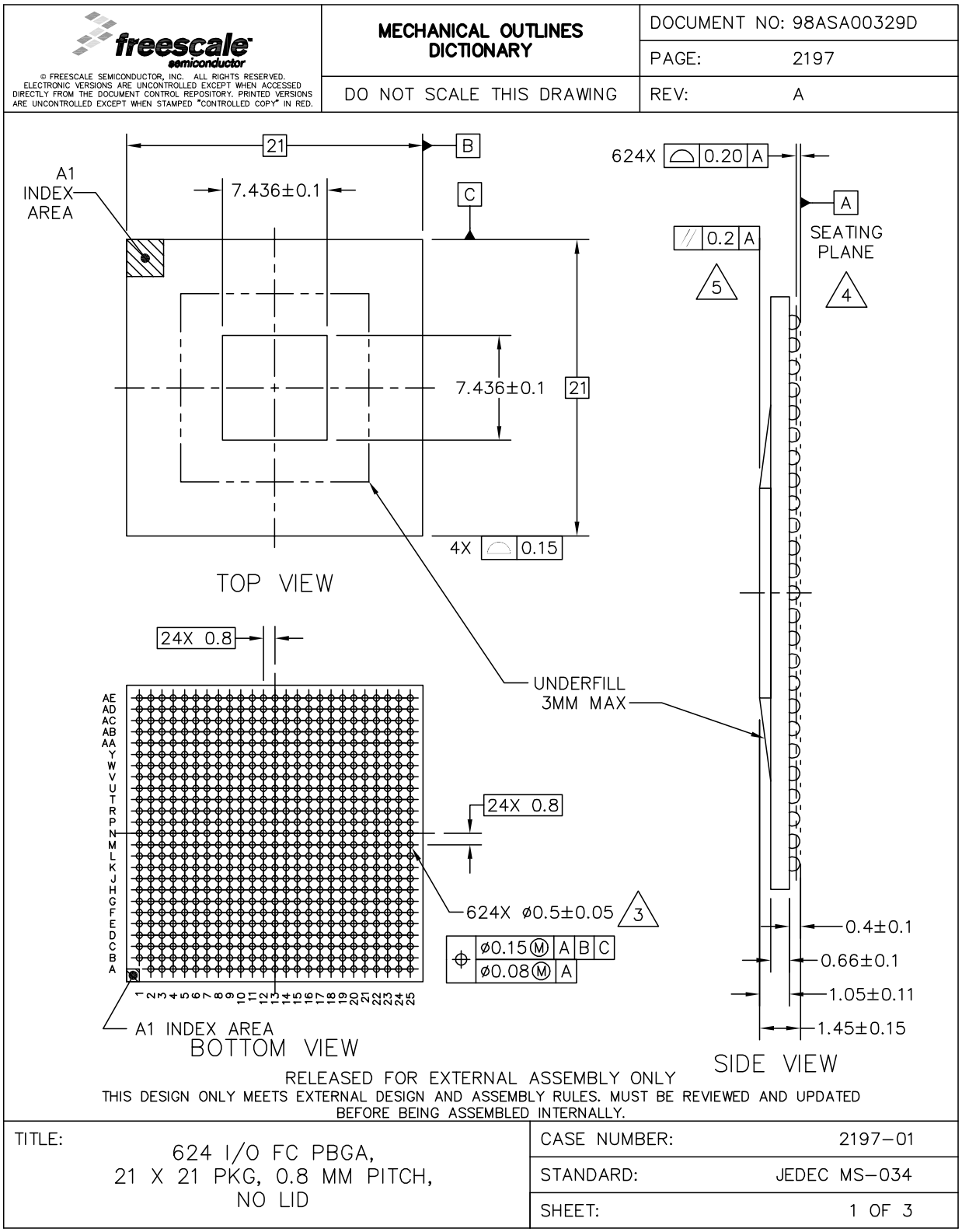

Table 92. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	

Table 93 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 93. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	PD (100K)
CLK1_N	C7	VDDHIGH_CAP			CLK1_N	—	—
CLK1_P	D7	VDDHIGH_CAP			CLK1_P	—	—
CLK2_N	C5	VDDHIGH_CAP			CLK2_N	—	—
CLK2_P	D5	VDDHIGH_CAP			CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI			CSI_CLK0M	—	—
CSI_CLK0P	F3	NVCC_MIPI			CSI_CLK0P	—	—
CSI_D0M	E4	NVCC_MIPI			CSI_D0M	—	—
CSI_D0P	E3	NVCC_MIPI			CSI_D0P	—	—
CSI_D1M	D1	NVCC_MIPI			CSI_D1M	—	—
CSI_D1P	D2	NVCC_MIPI			CSI_D1P	—	—
CSI_D2M	E1	NVCC_MIPI			CSI_D2M	—	—
CSI_D2P	E2	NVCC_MIPI			CSI_D2P	—	—
CSI_D3M	F2	NVCC_MIPI			CSI_D3M	—	—

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	PD (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[11]	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[12]	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[13]	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[5]	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	PU (100K)
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[7]	Input	PU (100K)
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[8]	Input	PU (100K)
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[9]	Input	PU (100K)
HDMI_CLKM	J5	HDMI_VPH			HDMI_VPH_CLKM	—	—
HDMI_CLKP	J6	HDMI_VPH			HDMI_CLKP	—	—
HDMI_D0M	K5	HDMI_VPH			HDMI_D0M	—	—
HDMI_D0P	K6	HDMI_VPH			HDMI_D0P	—	—
HDMI_D1M	J3	HDMI_VPH			HDMI_D1M	—	—
HDMI_D1P	J4	HDMI_VPH			HDMI_D1P	—	—
HDMI_D2M	K3	HDMI_VPH			HDMI_D2M	—	—
HDMI_D2P	K4	HDMI_VPH			HDMI_D2P	—	—
HDMI_DDCCEC	K2	HDMI_VPH			HDMI_DDCCEC	—	—
HDMI_HPD	K1	HDMI_VPH			HDMI_HPD	—	—
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	sjc_MOD	Input	PU (100K)
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	sjc_TCK	Input	PU (47K)
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	sjc_TDI	Input	PU (47K)
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	sjc_TDO	Output	Keeper
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	sjc_TMS	Input	PU (47K)
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	sjc_TRSTB	Input	PU (47K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[6]	Input	PU (100K)
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[8]	Input	PU (100K)
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[10]	Input	PU (100K)
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[12]	Input	PU (100K)
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[14]	Input	PU (100K)
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[7]	Input	PU (100K)
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[9]	Input	PU (100K)
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[11]	Input	PU (100K)
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[13]	Input	PU (100K)
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[15]	Input	PD (100K)
LVDS0_CLK_N	V4	NVCC_LVDS2P5	LVDS		LVDS0_CLK_N	—	—
LVDS0_CLK_P	V3	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_CLK	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS2P5	LVDS		LVDS0_TX0_N	—	—
LVDS0_TX0_P	U1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX0	Input	Keeper
LVDS0_TX1_N	U4	NVCC_LVDS2P5	LVDS		LVDS0_TX1_N	—	—
LVDS0_TX1_P	U3	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5	LVDS		LVDS0_TX2_N	—	—
LVDS0_TX2_P	V1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5	LVDS		LVDS0_TX3_N	—	—
LVDS0_TX3_P	W1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5	LVDS		LVDS1_CLK_N	—	—
LVDS1_CLK_P	Y4	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5	LVDS		LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5	LVDS		LVDS1_TX1_N	—	—
LVDS1_TX1_P	AA1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS2P5	LVDS		LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5	LVDS		LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX3	Input	Keeper