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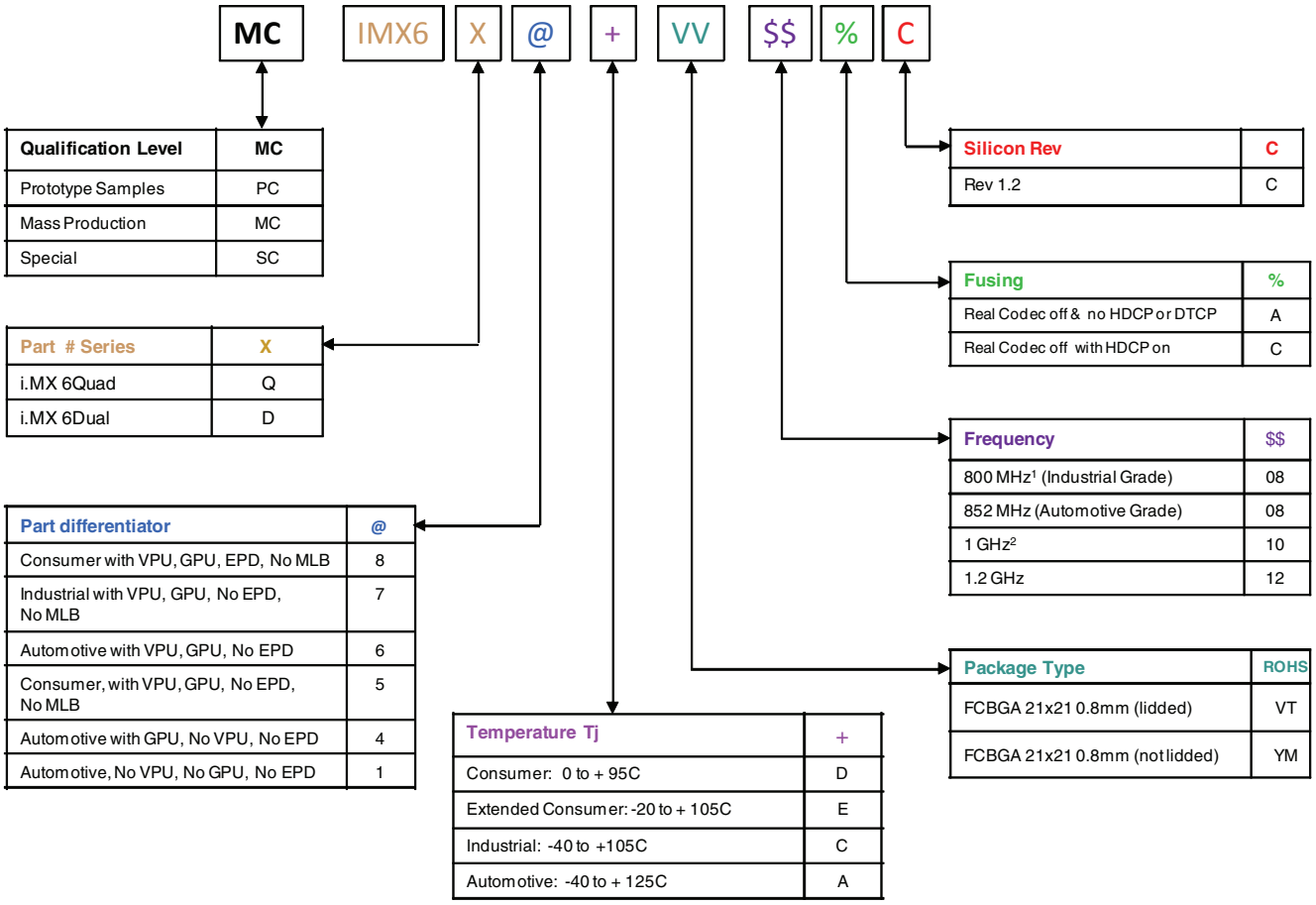
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q5eym10acr



1. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6Quad and i.MX 6Dual

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 7, "Operating Ranges," on page 23
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LVDDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface		The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

4.1.6 Low Power Mode Supply Currents

Table 11 shows the current core consumption (not including I/O) of i.MX 6Dual/6Quad processors in selected low power modes.

Table 11. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDDARM_IN (1.4 V)	6	mA
		VDDSoC_IN (1.4 V)	23	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDDARM_IN (1.4 V)	7.5	mA
		VDDSoC_IN (1.4 V)	22	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDDARM_IN (1.4 V)	7.5	mA
		VDDSoC_IN (1.4 V)	13.5	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL is enabled	VDDARM_IN (0.9 V)	0.1	mA
		VDDSoC_IN (0.9 V)	13	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL and bandgap are disabled	VDDARM_IN (0.9 V)	0.1	mA
		VDDSoC_IN (0.9 V)	2	mA
		VDDHIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 33 shows DDR I/O output buffer impedance of i.MX 6Dual/6Quad processors.

Table 33. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			Ω
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Dual/6Quad processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 34 lists the timing parameters.

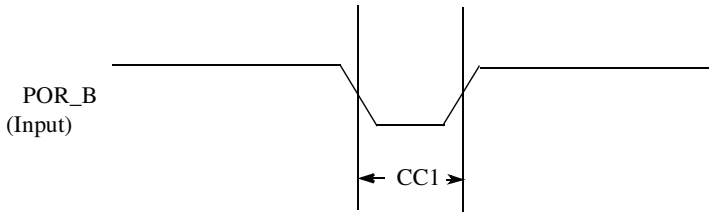


Figure 8. Reset Timing Diagram

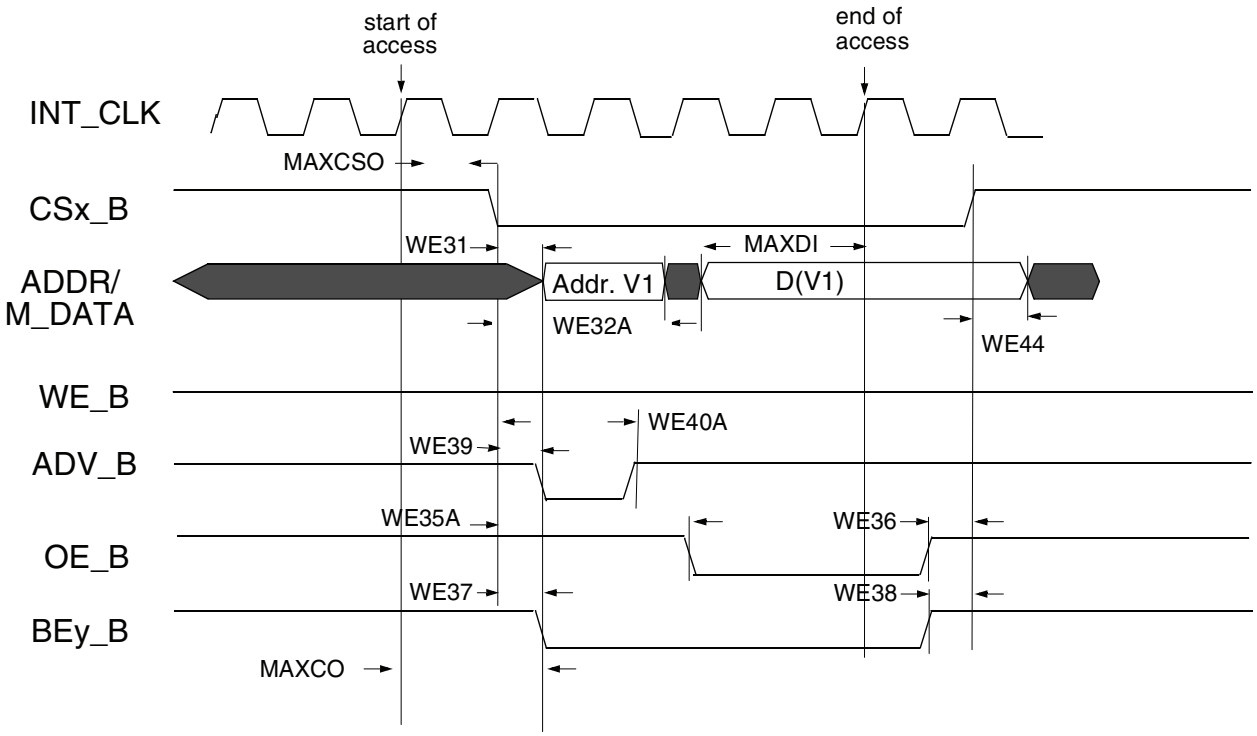


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

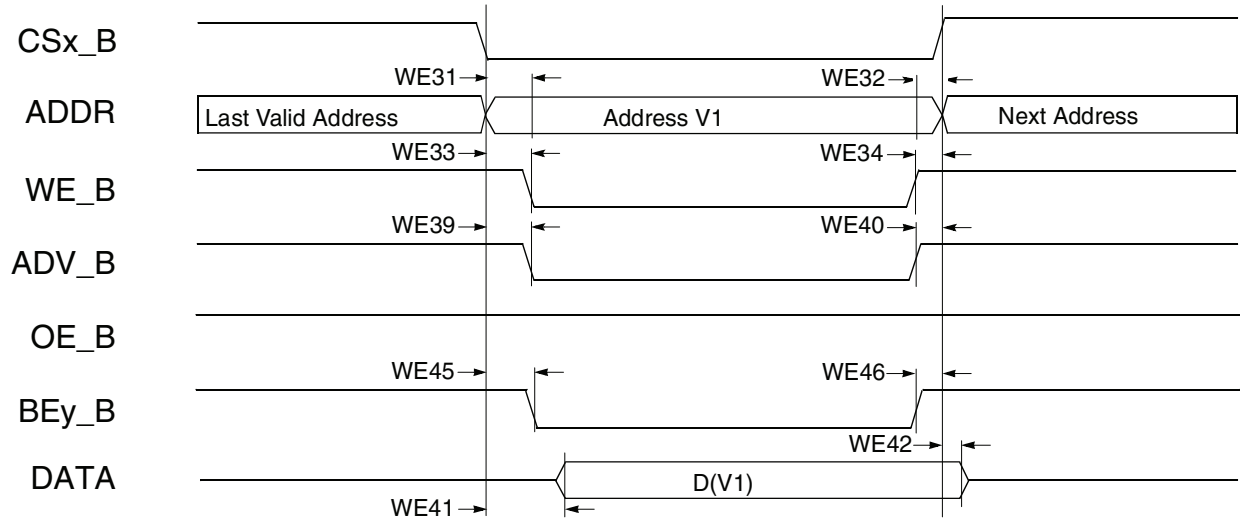


Figure 18. Asynchronous Memory Write Access

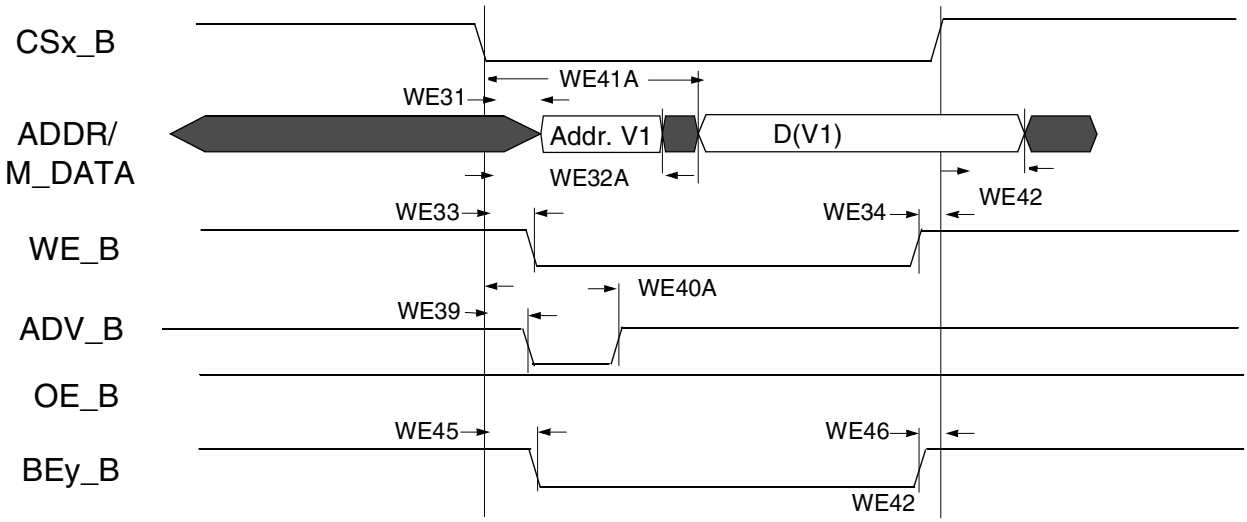


Figure 19. Asynchronous A/D Muxed Write Access

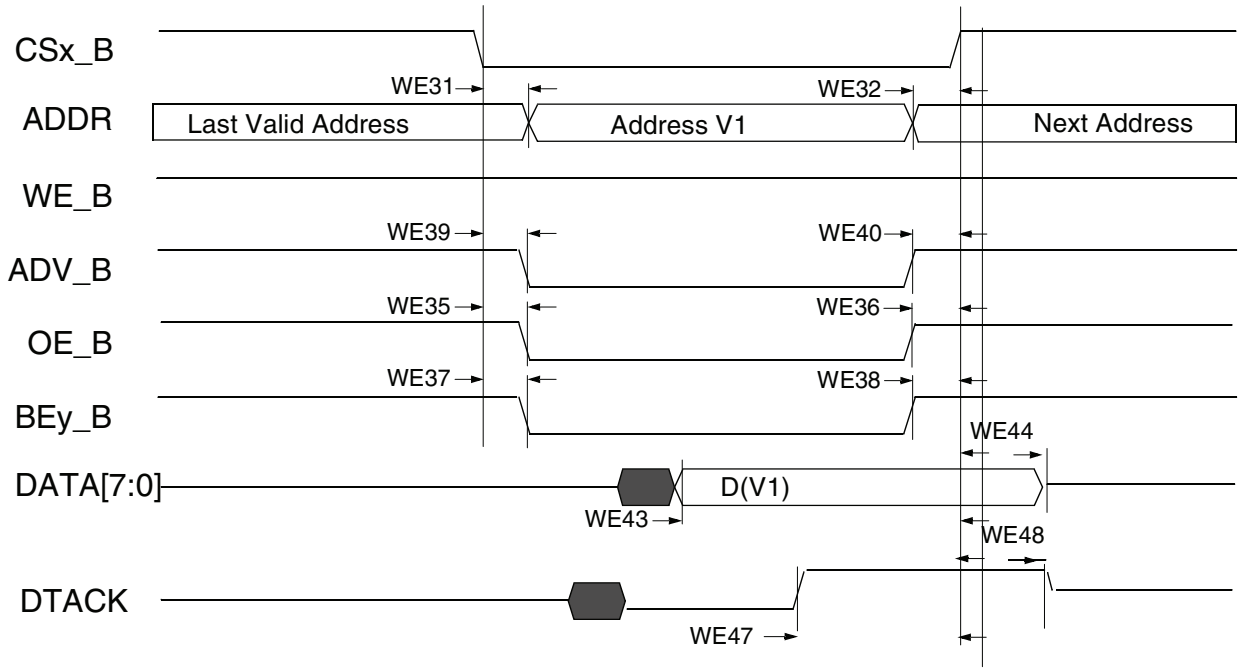


Figure 20. DTACK Read Access (DAP=0)

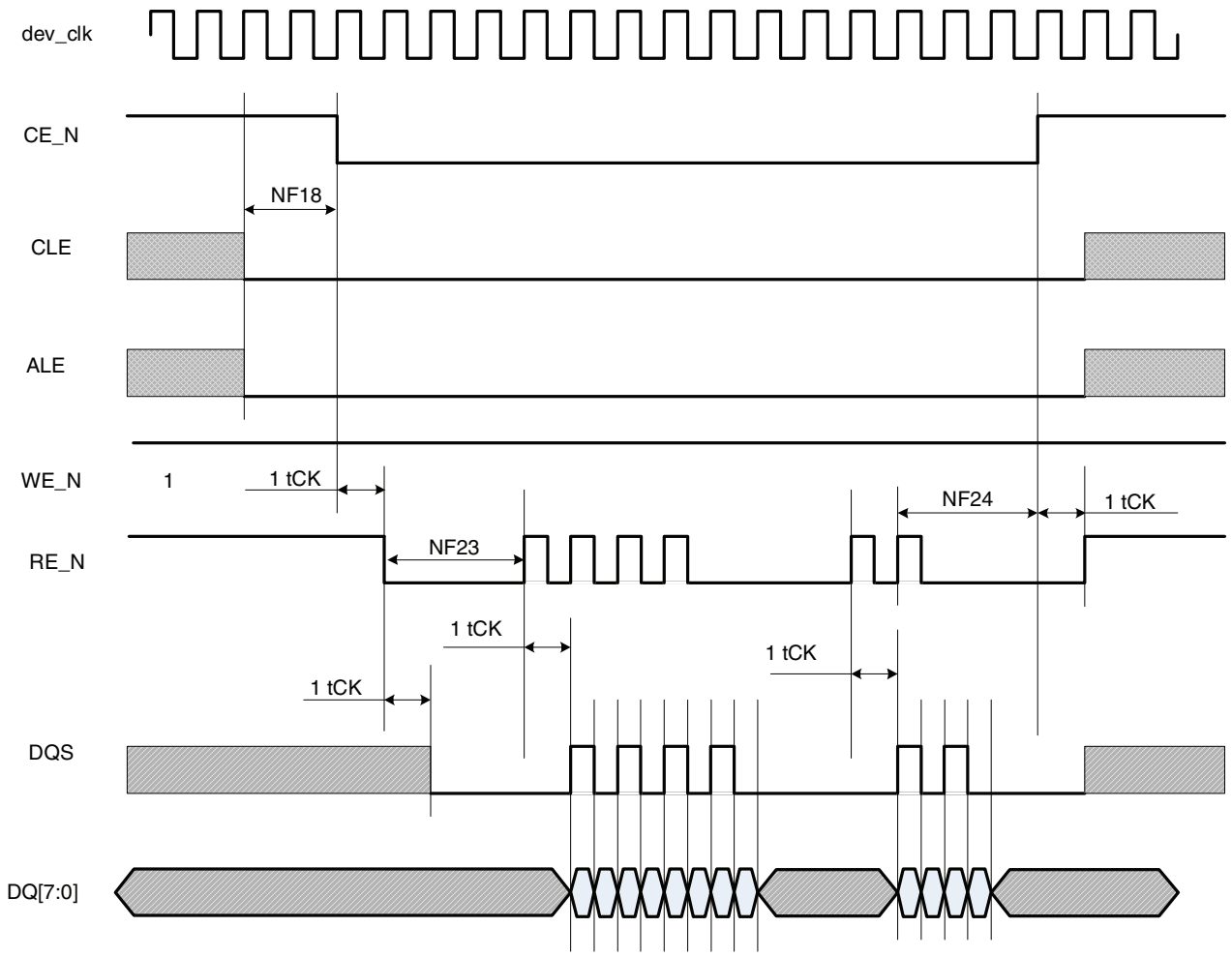


Figure 38. Samsung Toggle Mode Data Read Timing

Table 48. Samsung Toggle Mode Timing Parameters

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	7.5	--	ns
NF23	preamble delay	tPRE	(PRE_DELAY+1)*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 48 shows MII asynchronous input timings. Table 57 describes the timing parameter (M9) shown in the figure.

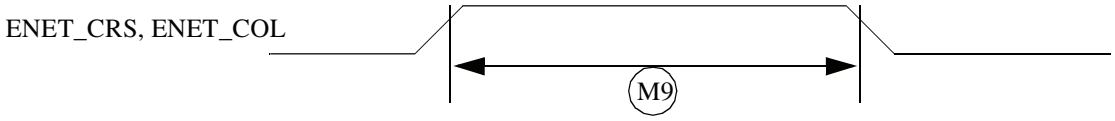


Figure 48. MII Async Inputs Timing Diagram

Table 57. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 49 shows MII asynchronous input timings. Table 58 describes the timing parameters (M10–M15) shown in the figure.

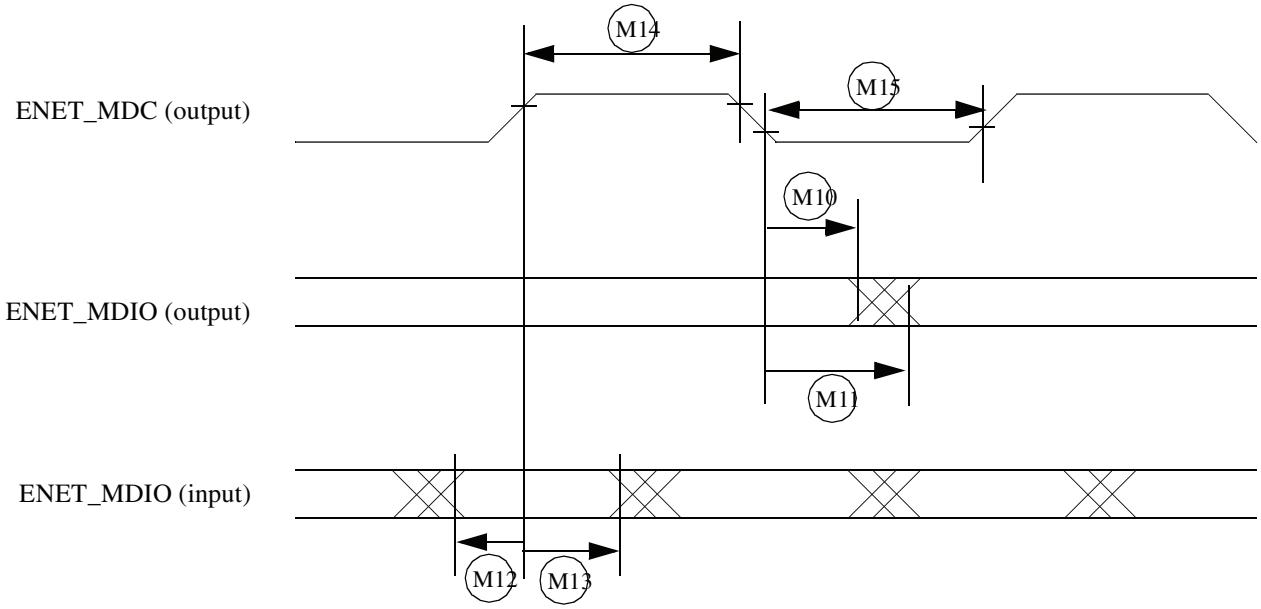


Figure 49. MII Serial Management Channel Timing Diagram

Table 58. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

Figure 50 shows RMII mode timings. Table 59 describes the timing parameters (M16–M21) shown in the figure.

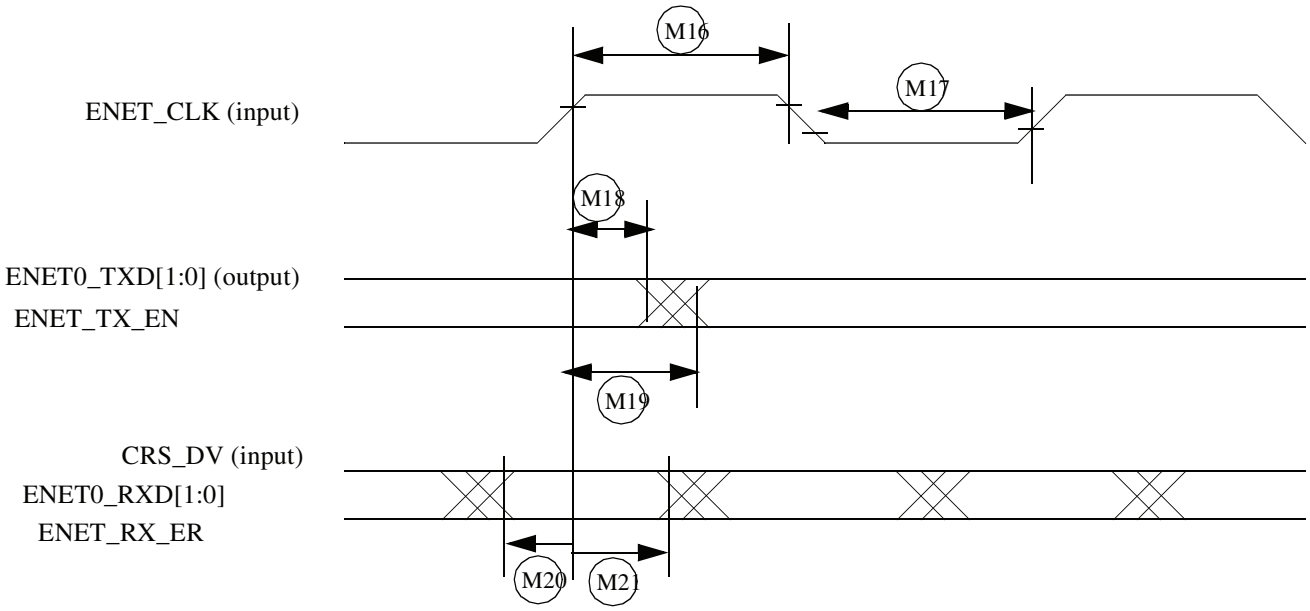


Figure 50. RMII Mode Signal Timing Diagram

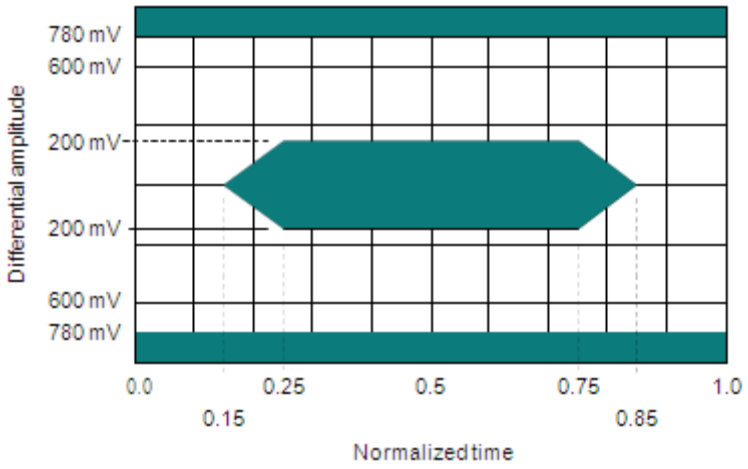


Figure 58. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

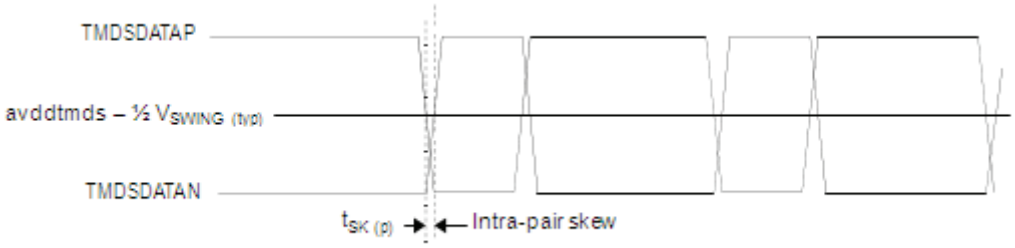


Figure 59. Intra-Pair Skew Definition

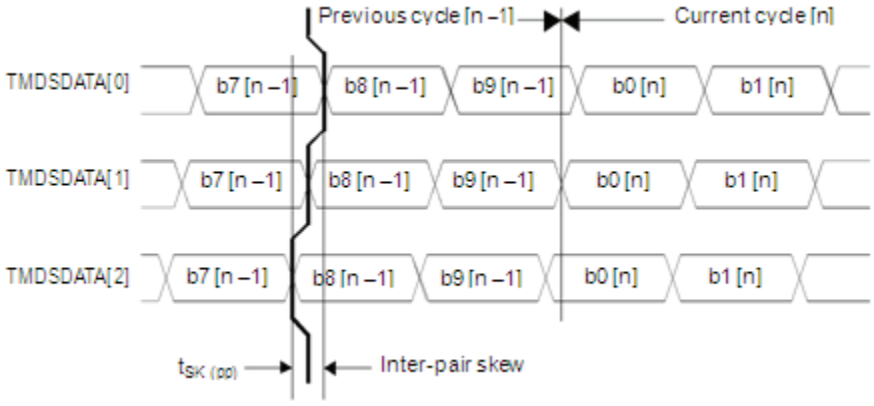


Figure 60. Inter-Pair Skew Definition

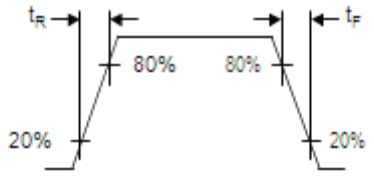


Figure 61. TMDS Output Signals Rise and Fall Time Definition

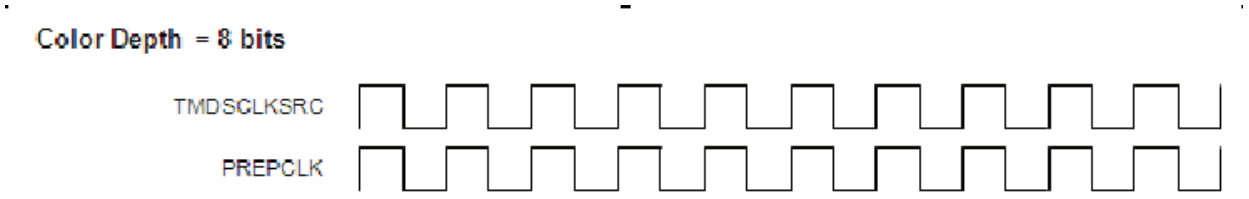


Figure 62. PREPCLK Frequencies

Table 62. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 57.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 57.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 57.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 57.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 59.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 60.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 61.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 61.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%

Table 67 shows timing characteristics of signals presented in Figure 68 and Figure 69.

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	Width of second vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_DOWN}{DI\_CLK\_PERIOD}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_UP}{DI\_CLK\_PERIOD}\right]\right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits."

Table 69. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	mV
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	mV
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and I/O supply voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 70. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
Input DC Specifications - Apply to CLKP/N and DATAP/N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV

Table 71. Electrical and Timing Information

L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

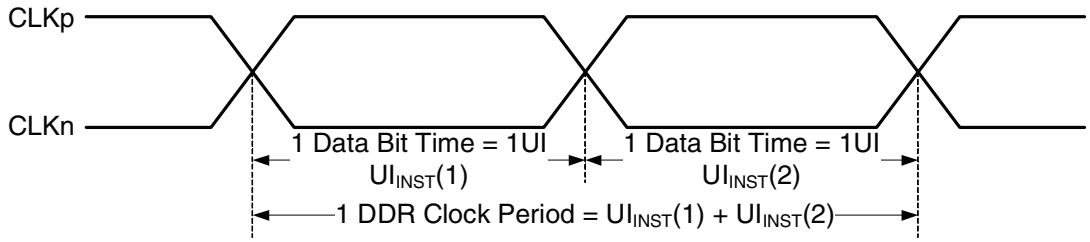


Figure 74. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 75:

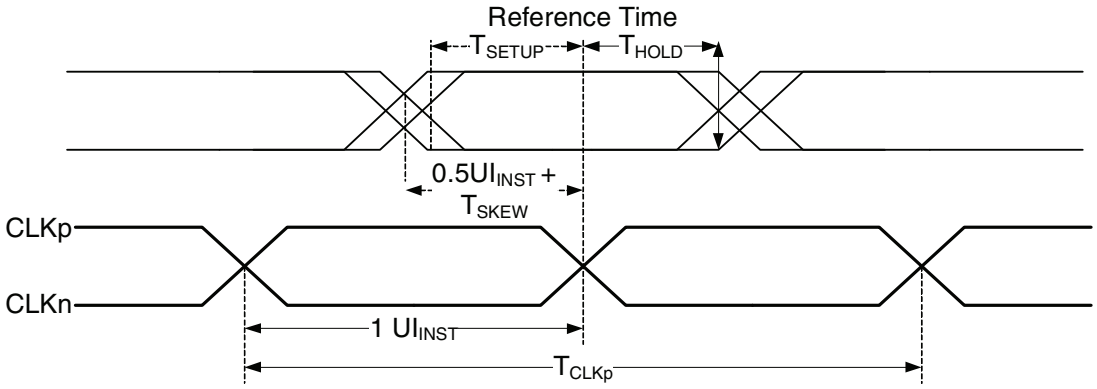


Figure 75. Data to Clock Timing Definitions

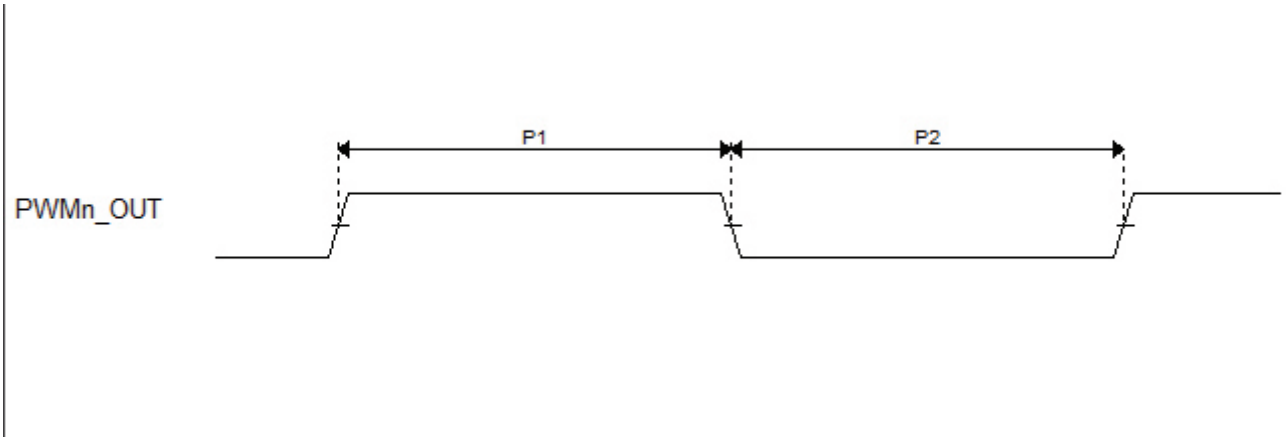


Figure 86. PWM Timing

Table 73. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15		ns
P2	PWM output pulse width low	15		ns

4.11.16 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.11.16.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

4.11.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 99 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 86 lists the transmit timing characteristics.

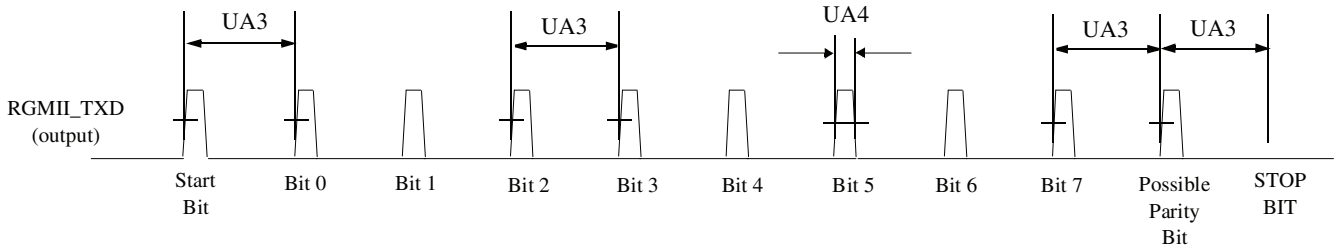


Figure 99. UART IrDA Mode Transmit Timing Diagram

Table 86. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16)*(1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 100 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 87 lists the receive timing characteristics.

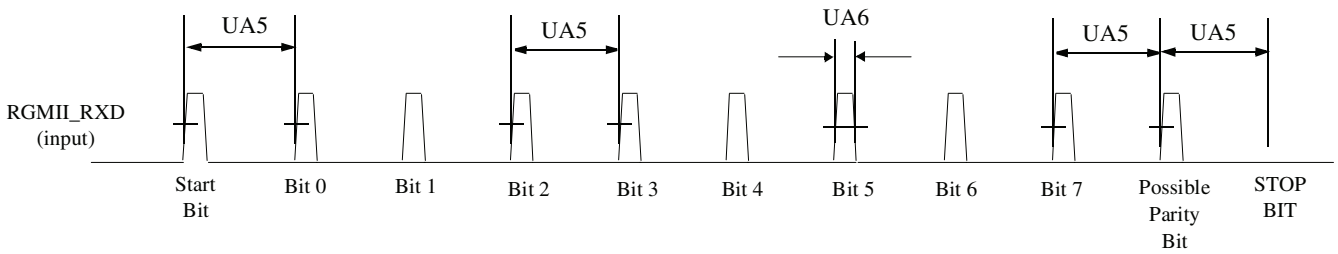


Figure 100. UART IrDA Mode Receive Timing Diagram

Table 87. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16)*(1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 95. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

R	P	N	M	L	K	J
GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF
GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12	GND	HDMI_DDCCEC	GND
GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M
GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P
GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM
GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG
GND	GND	GND	GND	GND	GND	GND
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDHIGH_IN
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP
VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
GND	GND	VDD_CACHE_CAP	GND	GND	GND	GND
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
GND	GND	GND	GND	GND	GND	GND
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	GND	GND	GND	GND	GND	GND
NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM2	NVCC_EIM1	NVCC_EIM0	EIM_D29
DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30
DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE
DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1

Table 98. i.MX 6Dual/6Quad Datasheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 0	09/2012	Initial public release.

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Document Number: IMX6DQCEC
Rev. 1
11/2012