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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q5eym10adr

- Nettops (Internet desktop devices)
- High-end mobile Internet devices (MID)
- High-end PDAs
- High-end portable media players (PMP) with HD video capability
- Gaming consoles
- Portable navigation devices (PND)

The i.MX 6Dual/6Quad processors have some very exciting features, for example:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MT/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, SATA-II, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual. Contact your local Freescale representative for more information.

MC IMX6 X @ + VV $$ % C

Qualification Level	MC
Prototype Samples	PC
Mass Production	MC
Special	SC

Part # Series	X
i.MX 6Quad	Q
i.MX 6Dual	D

Part differentiator	@
Consumer with VPU, GPU, EPD, No MLB	8
Industrial with VPU, GPU, No EPD, No MLB	7
Automotive with VPU, GPU, No EPD	6
Consumer, with VPU, GPU, No EPD, No MLB	5
Automotive with GPU, No VPU, No EPD	4
Automotive, No VPU, No GPU, No EPD	1

Temperature Tj	+
Consumer: 0 to + 95C	D
Extended Consumer: -20 to + 105C	E
Industrial: -40 to +105C	C
Automotive: -40 to + 125C	A

Package Type	ROHS
FCBGA 21x21 0.8mm (lidded)	VT
FCBGA 21x21 0.8mm (not lidded)	YM

Frequency	$$
800 MHz[1] (Industrial Grade)	08
852 MHz (Automotive Grade)	08
1 GHz[2]	10
1.2 GHz	12

Fusing	%
Real Codec off & no HDCP or DTCP	A
Real Codec off with HDCP on	C

Silicon Rev	C
Rev 1.2	C

1. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6Quad and i.MX 6Dual

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 7, "Operating Ranges," on page 23
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066, LVDDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

[3] Recommended nominal frequency 32.768 kHz.
[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 9 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, an internal ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator.
  - If no external crystal is present, then the ring oscillator is utilized.

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 10 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Dual/6Quad Power Consumption Measurement Application Note (AN4509) for more details on typical power consumption under various use case definitions.

Table 10. Maximal Supply Currents

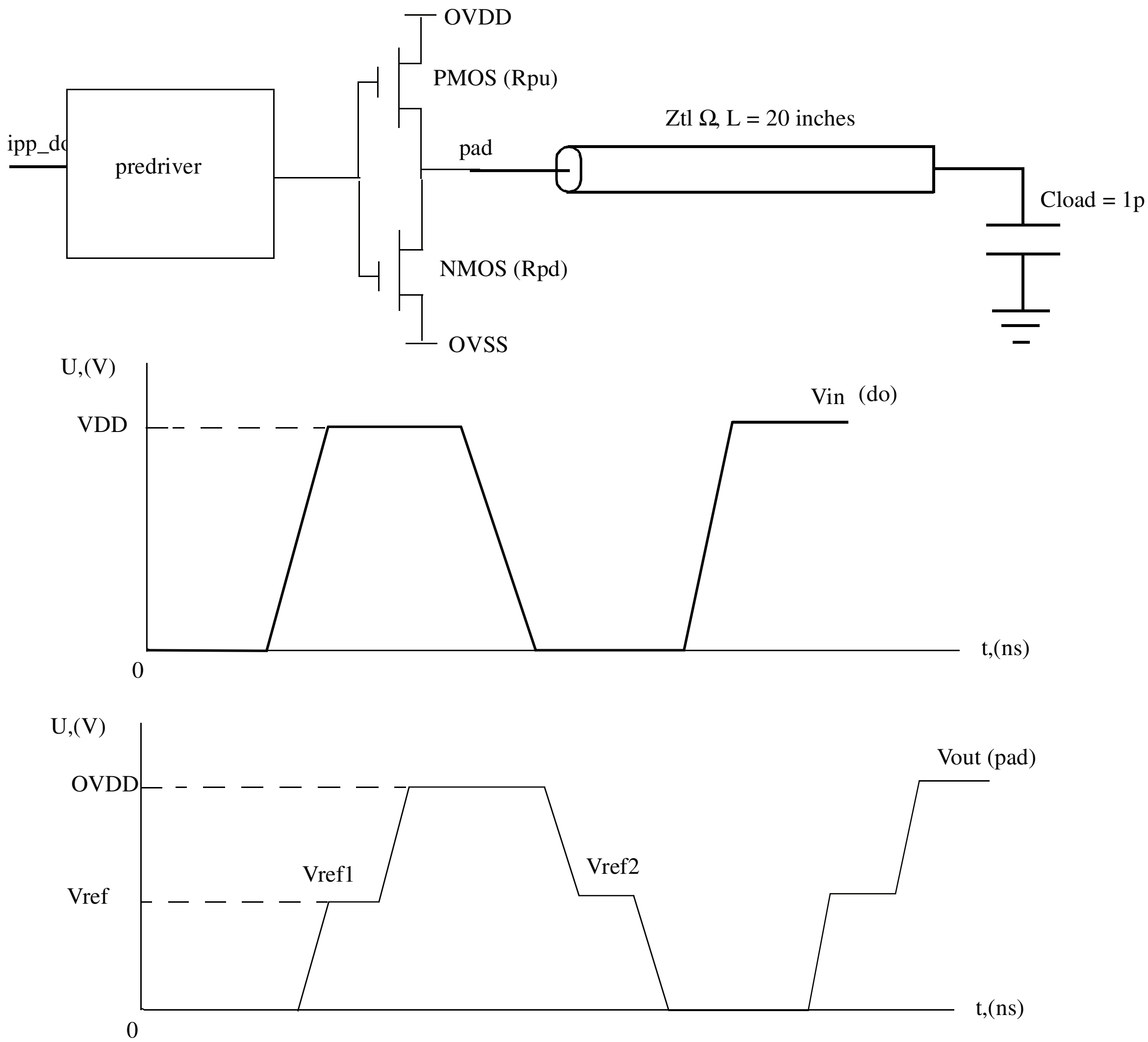
Power Line	Conditions	Max Current	Unit
VDDARM_IN+VDDARM23_IN	996 MHz ARM clock based on Power Virus operation	3920	mA
VDDSOC_IN	996 MHz ARM clock	1890	mA
VDDHIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	275[2]	µA
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)	—	25[3]	mA
Primary Interface (IO) Supplies			

4.1.10 HDMI Maximum Power Consumption

Table 15 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data pattern and Power-down modes.

Table 15. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down		HDMI_VPH	49	µA
		HDMI_VP	1100	µA



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 7. Impedance Matching Load for Measurement

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCSO	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.
2 In this table, CSA means WCSA when write operation or RCSA when read operation.
3 In this table, CSN means WCSN when write operation or RCSN when read operation.
4 t is axi_clk cycle time.
5 In this table, ADVN means WADVN when write operation or RADVN when read operation.

Table 40. DDR3/DDR3L Timing Parameter Table (continued)

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR6	Address output setup time	tIS	500	—	ps
DDR7	Address output hold time	tIH	400	—	ps

1 All measurements are in reference to Vref level.
2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 23 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram appear in Table 41.

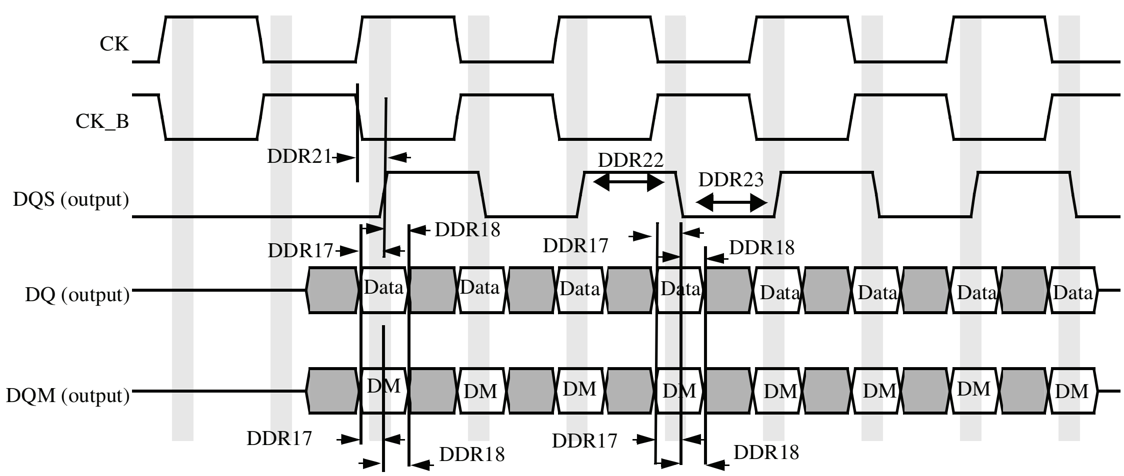


Figure 23. DDR3/DDR3L Write Cycle

Table 41. DDR3/DDR3L Write Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	240	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR23	DQS low level width	tDQSL	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.
2 All measurements are in reference to Vref level.
3 Measurements were taken using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 43.

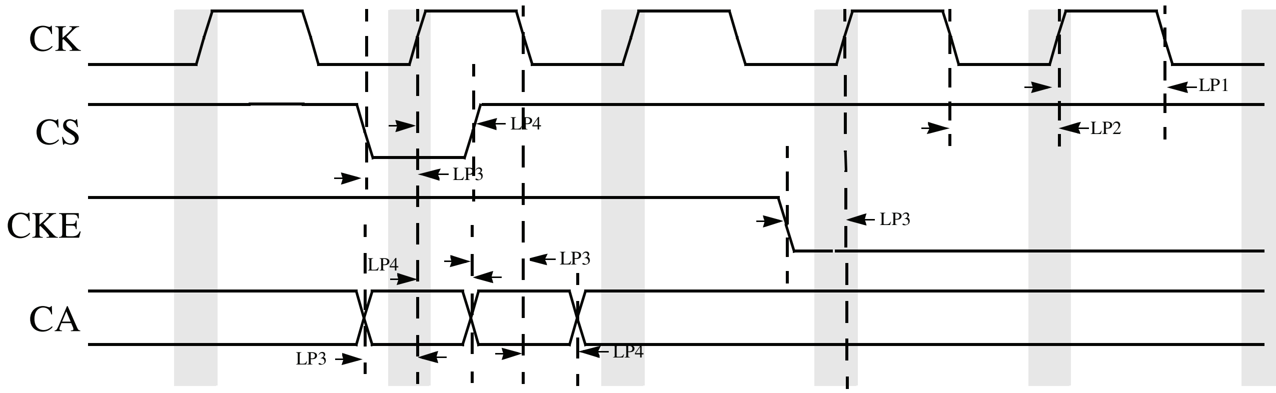


Figure 25. LPDDR2 Command and Address Timing Diagram

Table 43. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	tCH	0.45	0.55	tCK
LP2	SDRAM clock low-level width	tCL	0.45	0.55	tCK
LP3	CS, CKE setup time	tIS	270	—	ps
LP4	CS, CKE hold time	tIH	270	—	ps
LP3	CA setup time	tIS	230	—	ps
LP4	CA hold time	tIH	230	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 43 depicts the timing of SD/eMMC4.3, and Table 52 lists the SD/eMMC4.3 timing characteristics.

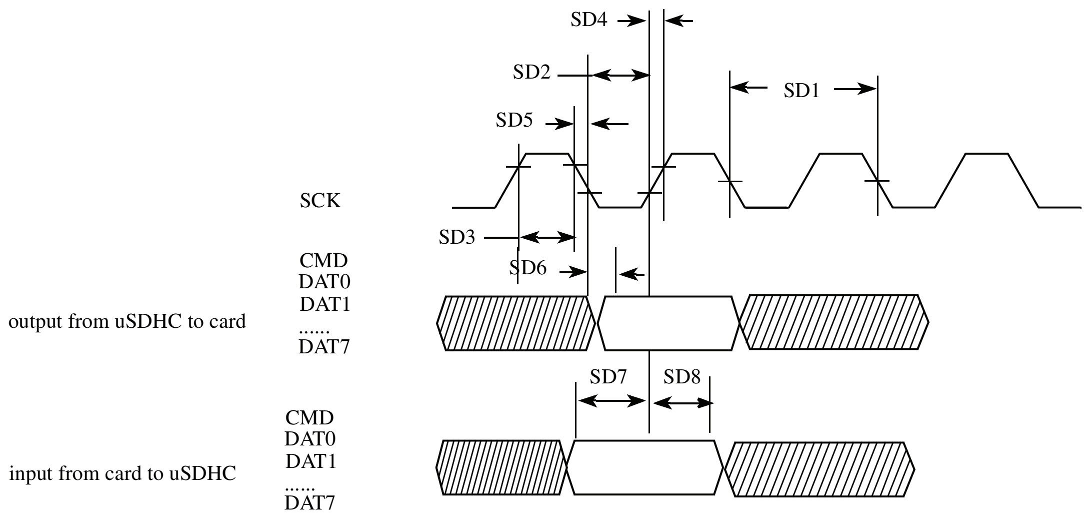


Figure 43. SD/eMMC4.3 Timing

Table 52. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns

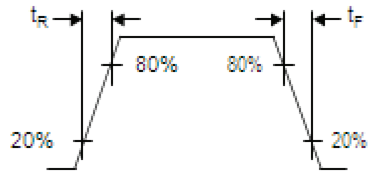


Figure 61. TMDS Output Signals Rise and Fall Time Definition

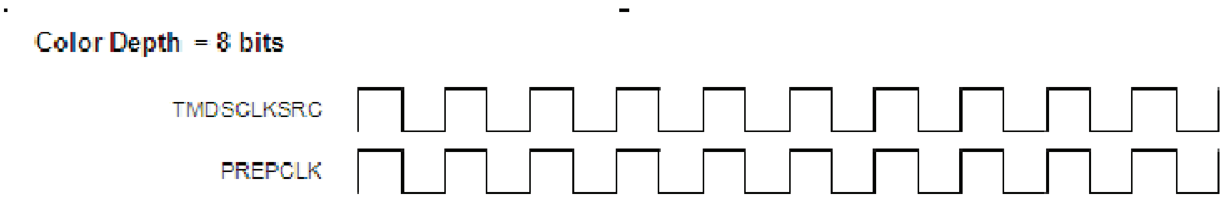


Figure 62. PREPCLK Frequencies

Table 62. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 57.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 57.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 57.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 57.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 59.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 60.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 61.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 61.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, “Gated Clock Mode,”) except for the CSIx_HSYNC signal, which is not used (see Figure 65). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

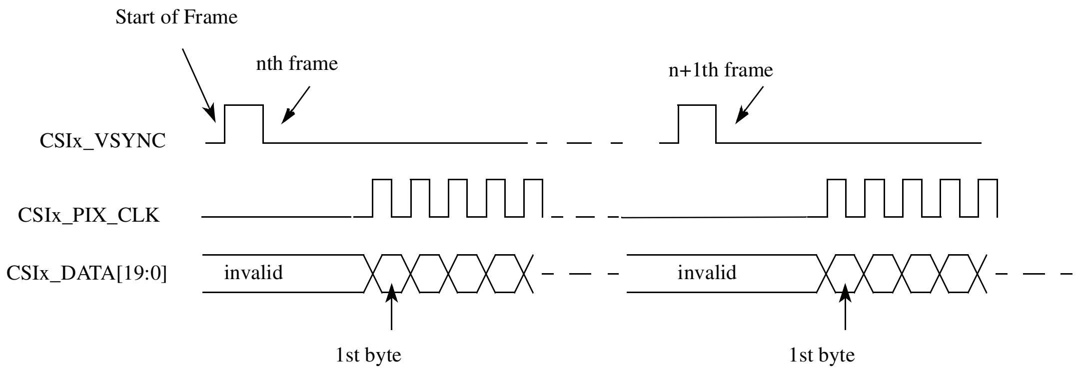


Figure 65. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 65 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered CSIx_VSYNC; active-high/low CSIx_HSYNC; and rising/falling-edge triggered CSIx_PIX_CLK.

NOTE

Table 66 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent waveform.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYCN) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

1 Display interface clock period immediate value.

$$\mathrm{Tdicp} = \begin{cases} T_{\mathrm{diclk}} \times \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}, & \text{for integer } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \\ T_{\mathrm{diclk}}\left(\mathrm{floor}\left[\dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \dfrac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\bar{T}\mathrm{dicp} = T_{\mathrm{diclk}} \times \frac{\mathrm{DISP\_CLK\_PERIOD}}{\mathrm{DI\_CLK\_PERIOD}}$$

2 DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$\mathrm{Accuracy} = (0.5 \times T_{\mathrm{diclk}}) \pm 0.62\mathrm{ns}$$

Table 72. DATA and FLAG Timing (continued)

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns

4.11.13.9 DATA and FLAG Signal Timing

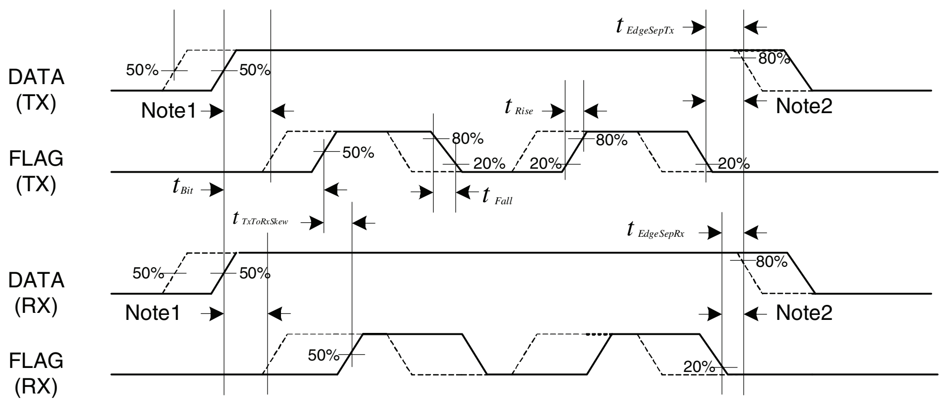


Figure 85. DATA and FLAG Signal Timing

4.11.14 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.14.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.15 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 86 depicts the timing of the PWM, and Table 73 lists the PWM timing parameters.

4.11.16.1.1 SATA PHY Transmitter Characteristics

Table 74 provides specifications for SATA PHY transmitter characteristics.

Table 74. SATA2 PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.11.16.1.2 SATA PHY Receiver Characteristics

Table 75 provides specifications for SATA PHY receiver characteristics.

Table 75. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	175	—	—	mV
Tolerance	PPM	–400	—	400	ppm

4.11.16.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω. 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 87 depicts the SJC test clock input timing. Figure 88 depicts the SJC boundary scan timing. Figure 89 depicts the SJC test access port. Signal parameters are listed in Table 76.

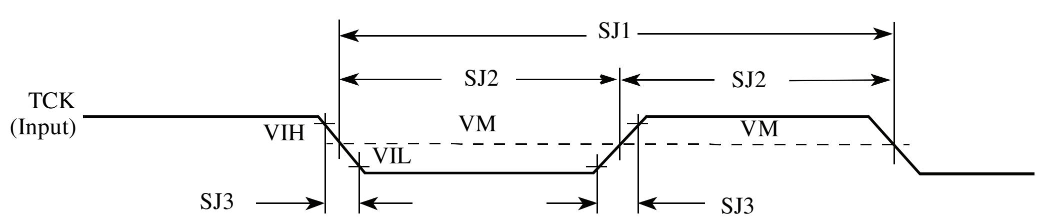


Figure 87. Test Clock Input Timing Diagram

4.11.19.4 SSI Receiver Timing with External Clock

Figure 96 depicts the SSI receiver external clock timing and Table 82 lists the timing parameters for the receiver timing with the external clock.

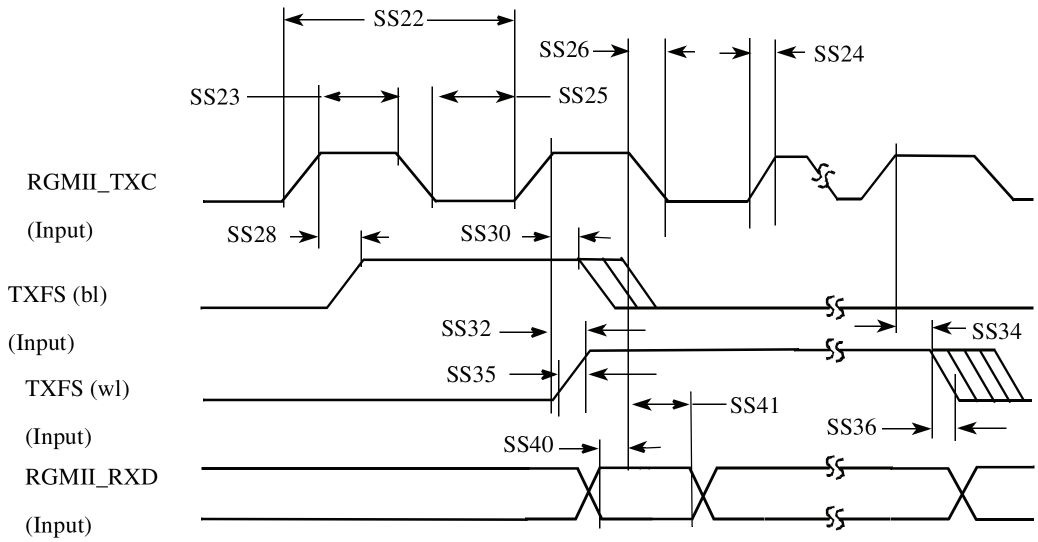


Figure 96. SSI Receiver External Clock Timing Diagram

Table 82. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

Figure 103 shows the top, bottom, and side views of the 21 × 21 mm bare die package.

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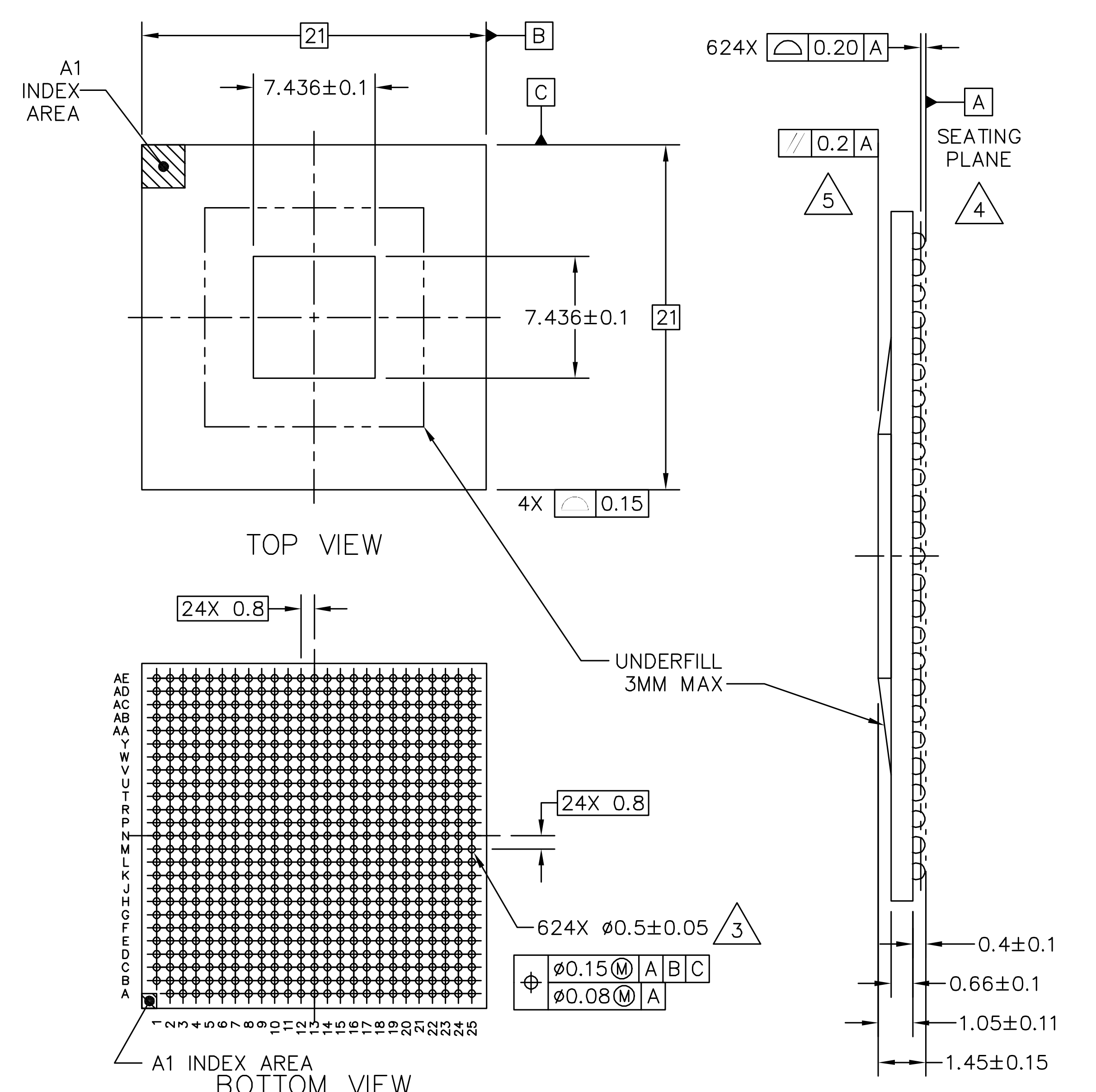

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TITLE: 624 I/O FC PBGA, 21 X 21 PKG, 0.8 MM PITCH, NO LID	CASE NUMBER:	2197–01
	STANDARD:	JEDEC MS–034
	SHEET:	1 OF 3

7 Revision History

Table 98 provides a revision history for this datasheet.

Table 98. i.MX 6Dual/6Quad Datasheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	• Made the following changes throughout the document: —Changed “WEIM” to “EIM” and “weim” to “eim” —Changed “TXC” to “RGMII_TXC” and “RXC” to “RGMII_RXC” —Changed “TXD” to “RGMII_TXD” and “RXD” to “RGMII_RXD” —Changed “TXD[n:0]” to “RGMII_TXDn (n = 0 to 3)” and “RXD[n:0]” to “RGMII_RXDn (n = 0 to 3)” —Changed “TX_CTL” to “RGMII_TX_CTL” and “RX_CTL” to “RGMII_RX_CTL” • Updated Table 1, "Example Consumer Grade Orderable Part Numbers," on page 4. • Updated Figure 1, "Part Number Nomenclature—i.MX 6Quad and i.MX 6Dual," on page 5. • Removed the figure, “Part Number Nomenclature—i.MX 6SoloLite.” • In Section 1.2, “Features:” —Added a new sub-bullet for FlexCAN under the Miscellaneous IPs and interfaces bullet —Added a footnote on the bottom of page 7 to specify performance limitation of 1 Gbps ENET • Updated Figure 2, "i.MX 6Dual/6Quad Consumer Grade System Block Diagram," on page 10 to add the FlexCAN feature. • In Table 2, "i.MX 6Dual/6Quad Modules List," on page 11: —Updated ENET description to specify performance limitation of 1 Gbps ENET —Added a new row to specify the FlexCAN feature —Updated TEMPMON description • Updated Section 3.1, “Special Signal Considerations.” • Updated Section 3.2, “Recommended Connections for Unused Analog Interfaces.” • Updated Table 5, "FCPBGA Package Thermal Resistance Data," on page 21. • In Table 8, "On-Chip LDOs and their On-Chip Loads," on page 25, added a footnote on VDD_CACHE_CAP. • Updated Table 10, "Maximal Supply Currents," on page 26. • Updated Table 11, "Stop Mode Current and Power Consumption," on page 28. • Updated Section 4.1.8, “SATA Typical Power Consumption.” • Updated Section 4.1.9, “PCIe 2.0 Maximum Power Consumption.” • Updated Section 4.1.10, “HDMI Maximum Power Consumption.” • In Table 21, "OSC32K Main Characteristics," on page 38, added 100 kΩ as ESR parameter max value. • Added a Note at the end of Section 4.2.1, “Power-Up Sequence.” • Updated Section 4.2.3, “Power Supplies Usage.” • Updated Table 36, "EIM Signal Cross Reference," on page 51. • Updated Table 37, "EIM Internal Module Multiplexing," on page 51. • Updated Table 39, "EIM Asynchronous Timing Parameters Table Relative Chip Select," on page 59. • In Table 49, "ECSPI Master Mode Timing Parameters," on page 77, updated CS5 min value. • Updated Section 4.11.5, “Ethernet Controller (ENET) AC Electrical Specifications.” • Added Section 4.11.6, “Flexible Controller Area Network (FlexCAN) AC Electrical Specifications.” • Removed figures, “TMDSCLKIN/PCLK Signal Definitions,” “Digital Interface Input Signals Timing Definition,” and “Digital Interface Switching Time Definition.” • Updated Figure 62, "PREPCLK Frequencies," on page 96. • Updated Table 62, "Switching Characteristics," on page 96. • Updated Table 66, "Video Signal Cross-Reference," on page 103. • Removed the section, “Clock Multiplier Switching Characteristics.” • Updated Table 71, "Electrical and Timing Information," on page 114. • Updated Section 4.11.15, “Pulse Width Modulator (PWM) Timing Parameters.” • Added a new bullet to the bullet list of Section 4.11.22, “USB PHY Parameters.” • In Table 93, "21 x 21 mm Functional Contact Assignments," on page 147, removed the row showing the details of ball name, ZQPAD.