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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9302-cqz

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Processor Core - ARM920T

The ARM920T is a Harvard architecture processor with separate 16-kbyte instruction and data caches with an 8-word line length but a unified memory. The processor utilizes a five-stage pipeline consisting of fetch, decode, execute, memory, and write stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- 32-bit Advanced Micro-Controller Bus Architecture (AMBA)
- 16 kbyte Instruction Cache with lockdown
- 16 kbyte Data Cache (programmable write-through or write-back) with lockdown
- MMU for Linux®, Microsoft® Windows® CE and other operating systems
- Translation Look Aside Buffers with 64 Data and 64 Instruction Entries
- Programmable Page Sizes of 1 Mbyte, 64 kbyte, 4 kbyte, and 1 kbyte
- Independent lockdown of TLB Entries

MaverickCrunch™ Math Engine

The MaverickCrunch Engine is a mixed-mode coprocessor designed primarily to accelerate the math processing required to rapidly encode digital audio formats. It accelerates single and double precision integer and floating point operations plus an integer multiply-accumulate (MAC) instruction that is considerably faster than the ARM920T's native MAC instruction. The ARM920T coprocessor interface is utilized thereby sharing its memory interface and instruction stream. Hardware forwarding and interlock allows the ARM to handle looping and addressing while MaverickCrunch handles computation. Features include:

- IEEE-754 single and double precision floating point
- 32 / 64-bit integer
- Add / multiply / compare
- Integer MAC 32-bit input with 72-bit accumulate
- Integer Shifts
- Floating point to/from integer conversion
- Sixteen 64-bit register files
- Four 72-bit accumulators

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID are programmed into the EP9302 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP9302 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

General Purpose Memory Interface (SDRAM, SRAM, ROM, Flash)

The EP9302 features a unified memory address model where all memory devices are accessed over a common address/data bus. Memory accesses are performed via the Processor bus. The SRAM memory controller supports 8 and 16-bit devices and accommodates an internal boot ROM concurrently with 16-bit SDRAM memory.

- 1 to 4 banks of 16-bit ,100-MHz SDRAM
- Address and data bus shared between SDRAM, SRAM, ROM, and FLASH memory
- NOR FLASH memory supported

Table B. General Purpose Memory Interface Pin Assignments

Pin Mnemonic	Pin Description
SDCLK	SDRAM Clock
SDCLKEN	SDRAM Clock Enable
SDCSn[3:0]	SDRAM Chip Selects 3-0
RASn	SDRAM RAS
CASn	SDRAM CAS
SDWEn	SDRAM Write Enable
CSn[7:6] and CSn[3:0]	Chip Selects 7, 6, 3, 2, 1, 0
AD[25:0]	Address Bus 25-0
DA[15:0]	Data Bus 15-0
DQMn[1:0]	SDRAM Output Enables / Data Masks
WRn	SRAM Write Strobe
RDn	SRAM Read / OE Strobe
WAITn	SRAM Wait Input

PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Table J. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Name - Description
XTALI	Main Oscillator Input
XTALO	Main Oscillator Output
VDD_PLL	Main Oscillator Power
GND_PLL	Main Oscillator Ground

Timers

The Watchdog Timer ensures proper operation by requiring periodic attention to prevent a reset-on-time-out.

Two 16-bit timers operate as free running down-counters or as periodic timers for fixed interval interrupts and have a range of 0.03 ms to 4.27 seconds.

One 32-bit timer, plus a 6-bit prescale counter, has a range of 0.03 µs to 73.3 hours.

One 40-bit debug timer, plus 6-bit prescale counter, has a range of 1.0 µs to 12.7 days.

Interrupt Controller

The interrupt controller allows up to 54 interrupts to generate an Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) signal to the processor core. Thirty-two hardware priority assignments are provided for assisting IRQ vectoring, and two levels are provided for FIQ vectoring. This allows time critical interrupts to be processed in the shortest time possible. Internal interrupts may be programmed as active high or active low level sensitive inputs. GPIO pins programmed as interrupts may be programmed as active high level sensitive, active low level sensitive, rising edge triggered, falling edge triggered, or combined rising/falling edge triggered.

- Supports 54 interrupts from a variety of sources (such as UARTs, GPIO and ADC)
- Routes interrupt sources to either the ARM920T's IRQ or FIQ (Fast IRQ) inputs
- Three dedicated off-chip interrupt lines operate as active high level sensitive interrupts
- Any of the 19 GPIO lines maybe configured to generate interrupts
- Software supported priority mask for all FIQs and IRQs

Table K. External Interrupt Controller Pin Assignment

Pin Mnemonic	Pin Name - Description
INT[3] and INT[1:0]	External Interrupts 2, 1, 0

Note: INT[2] is not bonded out.

Dual LED Drivers

Two pins are assigned specifically to drive external LEDs.

Table L. Dual LED Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
GRLED	Green LED	General Purpose I/O
REDLED	Red LED	General Purpose I/O

General Purpose Input/Output (GPIO)

The 16 EGPIO and the 3 FGPIO pins may each be configured individually as an output, an input, or an interrupt input.

There are 10 pins that may alternatively be used as input, output, or open-drain pins, but do not support interrupts. These pins are:

- Ethernet MDIO
- Both LED Outputs
- EEPROM Clock and Data
- HGPIO[5:2]
- CGPIO[0]

6 pins may alternatively be used as inputs only:

- CTSn, DSRn / DCDn
- 3 Interrupt Lines

2 pins may alternatively be used as outputs only:

- RTSn
- ARSTn

Table M. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[3:1]	Expanded General Purpose Input / Output Pins with Interrupts

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 200 MHz (184 MHz for industrial conditions).

Table N. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table O. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-Channel DMA Controller

The DMA module contains 12 separate DMA channels. Ten of these may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Internal Boot ROM

The Internal 16-kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP9301 User's Guide for operational details.

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation	(Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)			-	±10	mA
Output current per pin, DC			-	±50	mA
Digital Input voltage	(Note 2)		-0.3	RVDD+0.3	V
Storage temperature			-40	+125	°C

Note: 1. Includes all power generated by AC and/or DC output loading.
2. The power supply pins are at maximum values listed in "Recommended Operating Conditions", below.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	RVDD CVDD VDD_PLL VDD_ADC	3.0 1.71 1.71 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial	FCLK	-	-	200	MHz
Processor Clock Speed - Industrial	FCLK	-	-	184	MHz
System Clock Speed - Commercial	HCLK	-	-	100	MHz
System Clock Speed - Industrial	HCLK	-	-	92	MHz

DC Characteristics

(T_A = 0 to 70° C; CVDD = VDD_PLL = 1.8; RVDD = 3.3 V;
All grounds = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Max	Unit
High level output voltage	Iout = -4 mA	(Note 3)	V_{oh}	0.85 × RVDD	-	V
Low level output voltage	Iout = 4 mA		V_{ol}	-	0.15 × RVDD	V
High level input voltage		(Note 4)	V_{ih}	0.65 × RVDD	VDD + 0.3	V
Low level input voltage		(Note 4)	V_{il}	–0.3	0.35 × RVDD	V
High level leakage current	Vin = 3.3 V	(Note 4)	I_{ih}	-	10	µA
Low level leakage current	Vin = 0	(Note 4)	I_{il}	-	-10	µA

Parameter		Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded)					
Power Supply Current:	CVDD / VDD_PLL Total RVDD	- -	180 45	230 80	mA mA
Low-Power Mode Supply Current	CVDD / VDD_PLL Total RVDD	- -	2 1.0	3.5 2	mA mA

Note: 3. For open drain pins, high level output voltage is dependent on the external load.
4. All inputs that do not include internal pull-ups or pull-downs, must be externally driven for proper operation (See Table Q on page 39). If an input is not driven, it should be tied to power or ground, depending on the particular function. If an I/O pin is not driven and programmed as an input, it should be tied to power or ground through its own resistor.

Memory Interface

Figure 2 through Figure 5 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK high time	t_{clk_high}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK low time	t_{clk_low}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK rise/fall time	t_{clkrf}	-	2	4	ns
Signal delay from SDCLK rising edge time	t_d	-	-	8	ns
Signal hold from SDCLK rising edge time	t_h	1	-	-	ns
DQMn delay from SDCLK rising edge time	t_{DQd}	-	-	8	ns
DQMn hold from SDCLK rising edge time	t_{DQh}	1	-	-	ns
DA valid setup to SDCLK rising edge time	t_{DAs}	2	-	-	ns
DA valid hold from SDCLK rising edge time	t_{DAh}	3	-	-	ns

SDRAM Load Mode Register Cycle

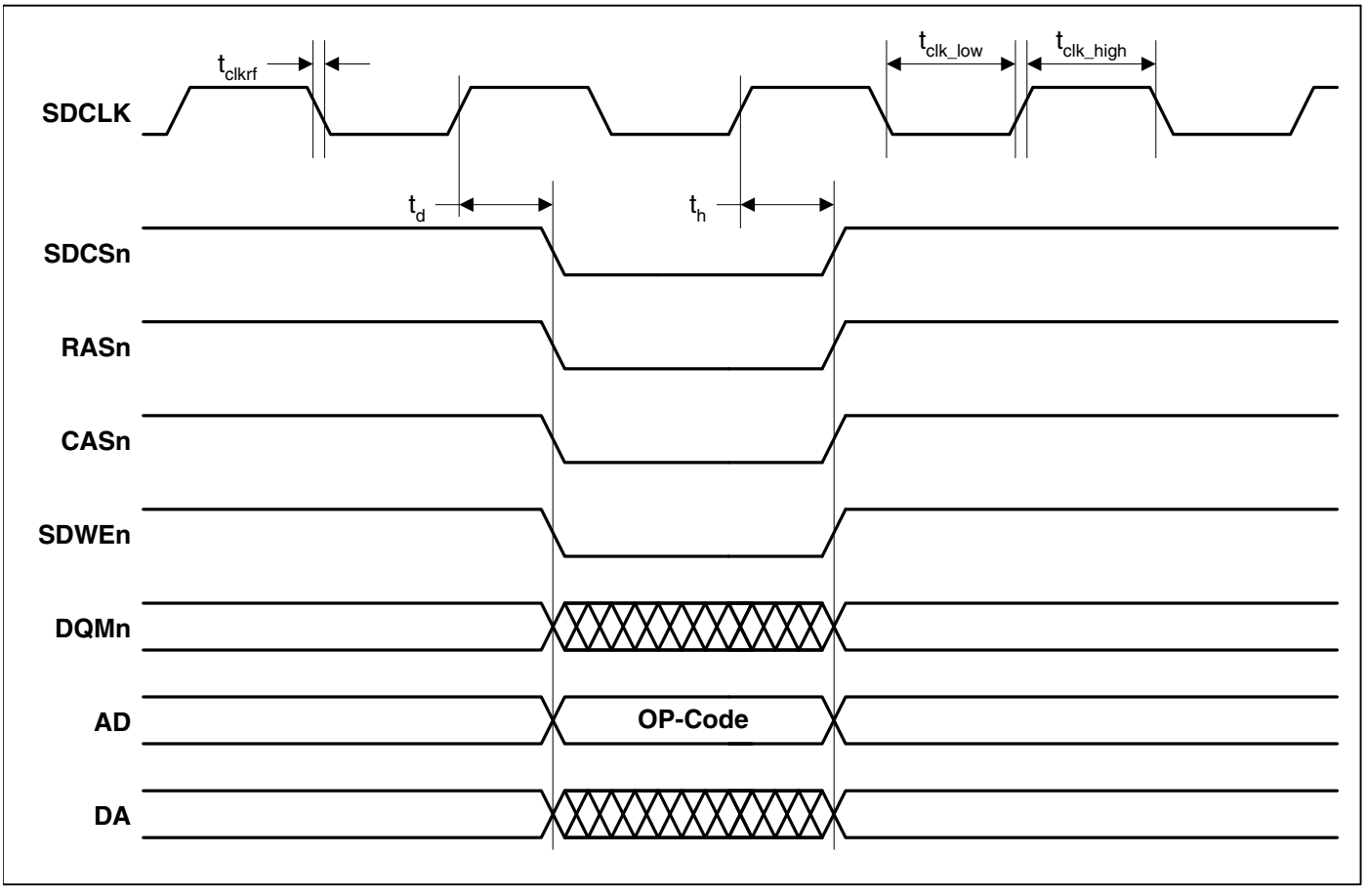

Figure 2. SDRAM Load Mode Register Cycle Timing Measurement

SDRAM Burst Write Cycle

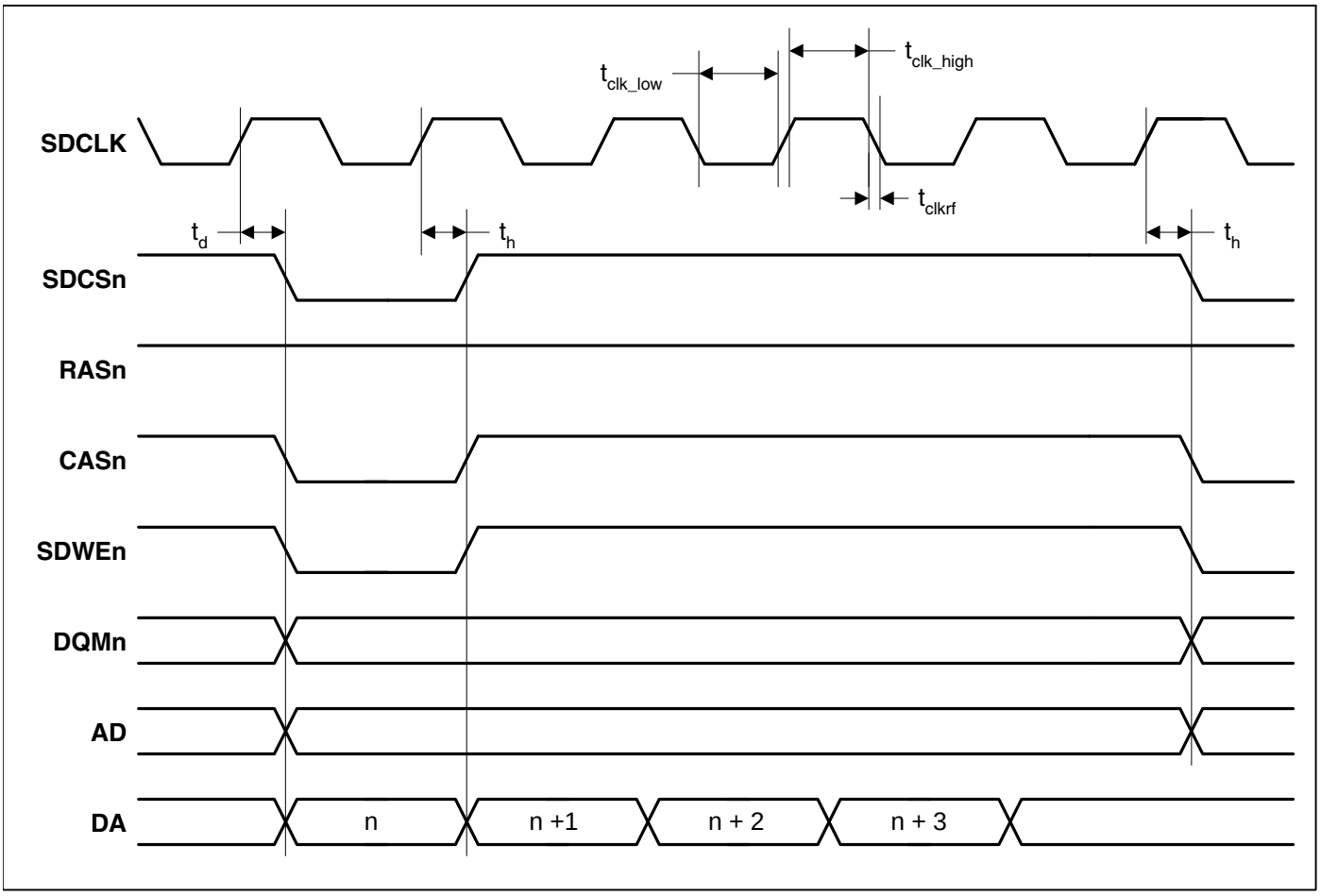

Figure 4. SDRAM Burst Write Cycle Timing Measurement

Static Memory 32-bit Read on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to Address transition time	t_{AD1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{AD2}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{AD3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times (4 \times WST1 + 5)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

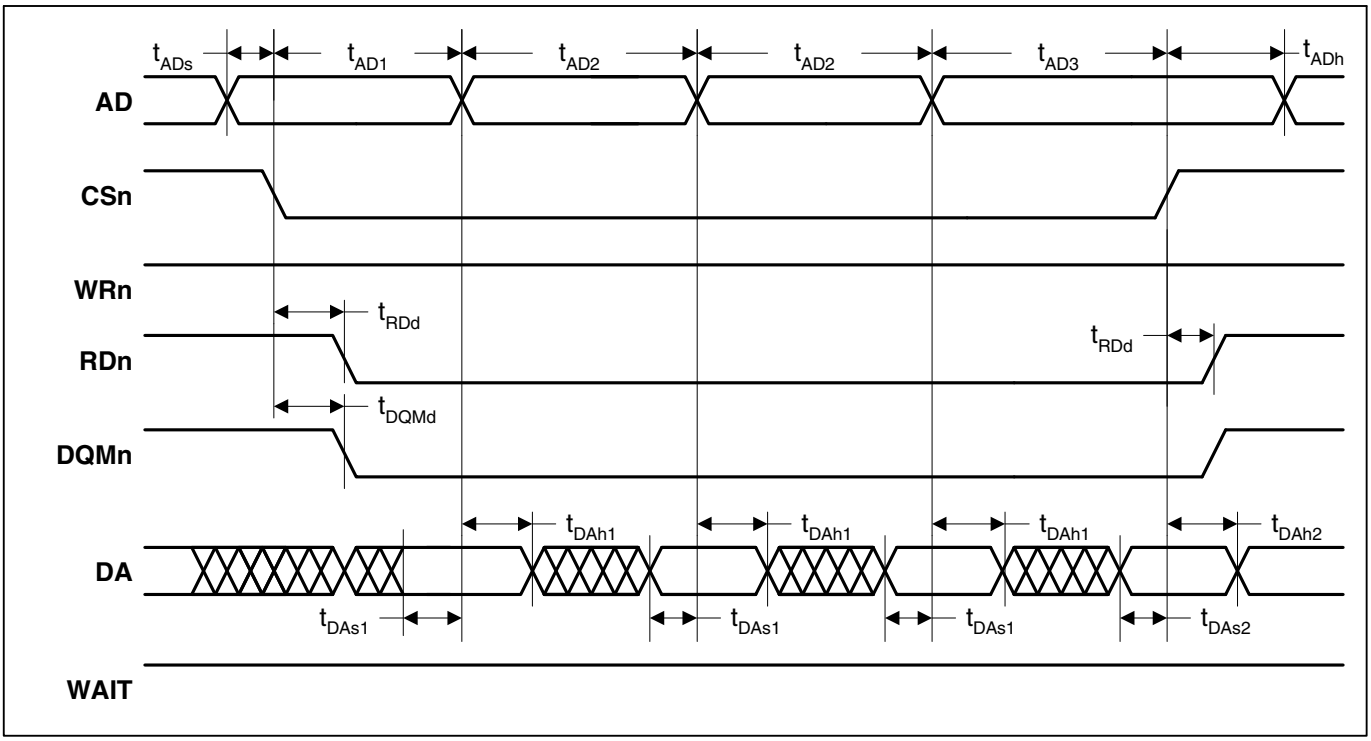

Figure 6. Static Memory Multiple Word Read 8-bit Cycle Timing Measurement

Static Memory 32-bit Write on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	$t_{HCLK} \times 2$	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

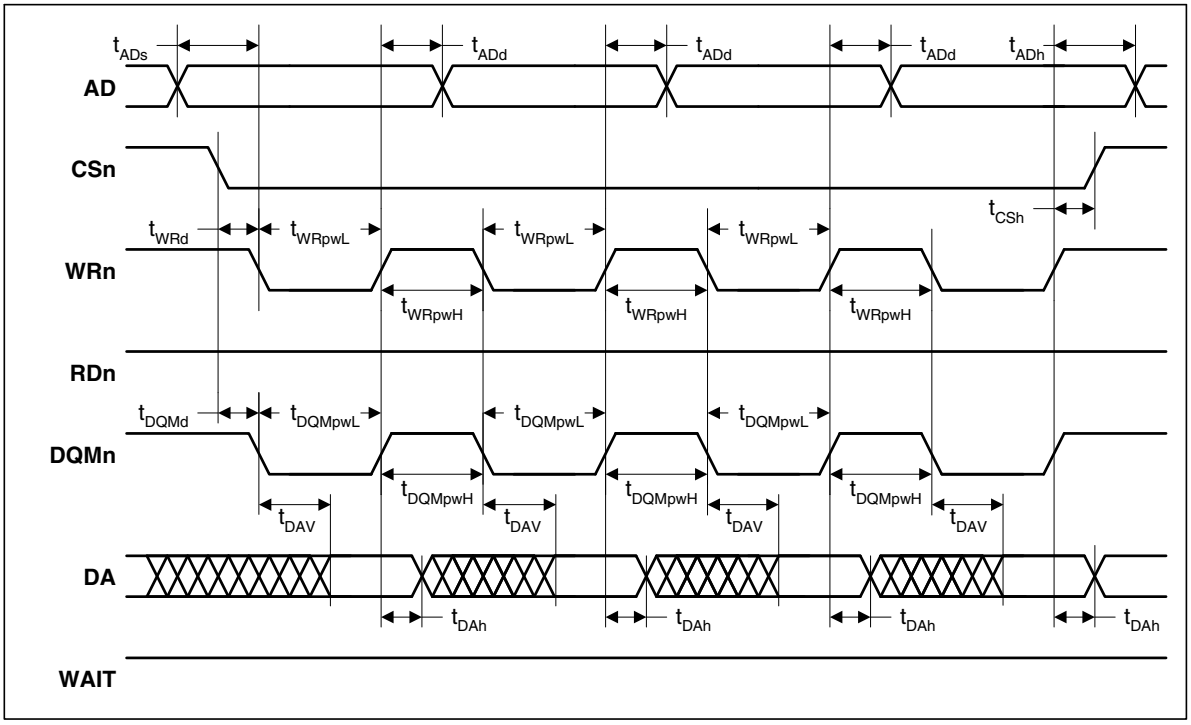

Figure 7. Static Memory Multiple Word Write 8-bit Cycle Timing Measurement

Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

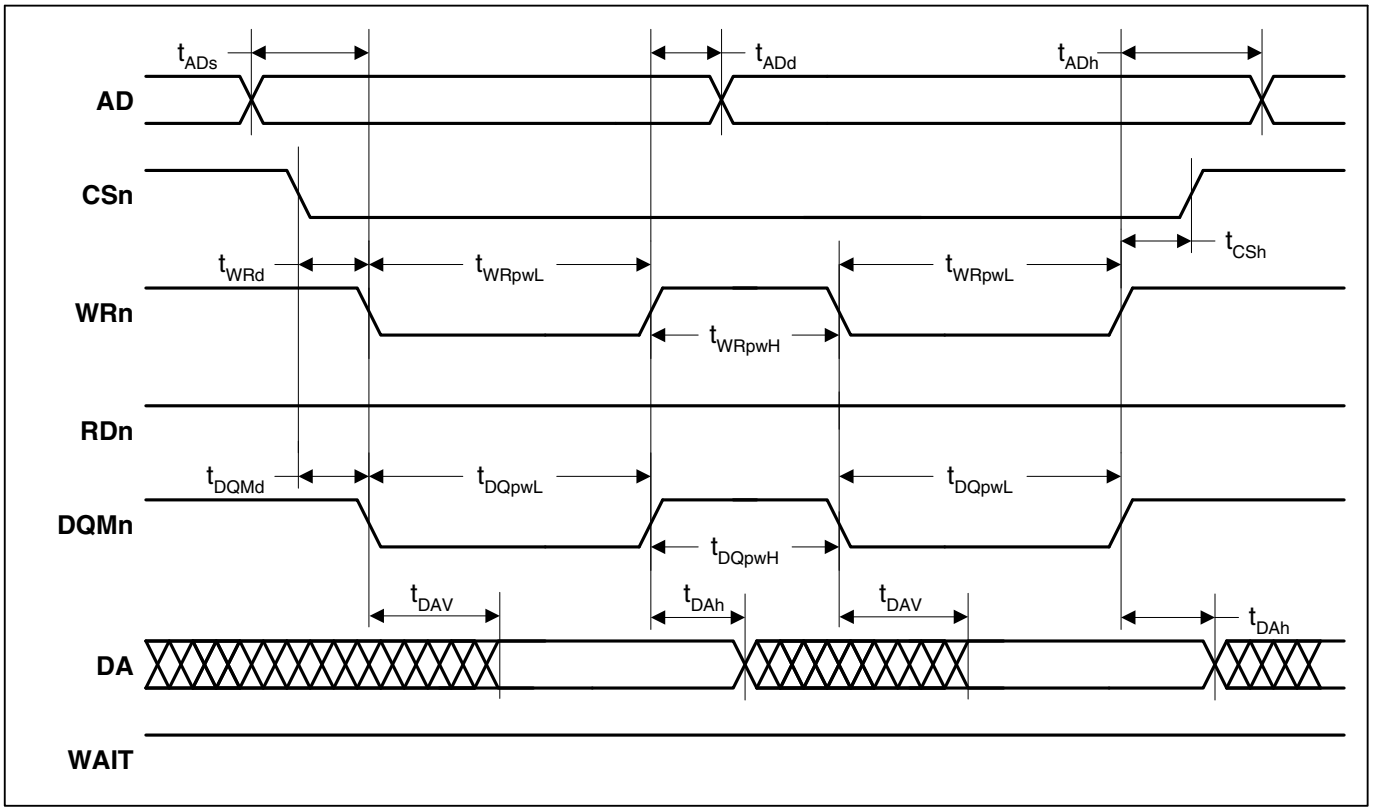

Figure 9. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

Static Memory Burst Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to Address 1 transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{ADd2}	-	$t_{HCLK} \times (WST2 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to CSn deassert time	t_{DAs2}	t_{HCLK} + 12	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

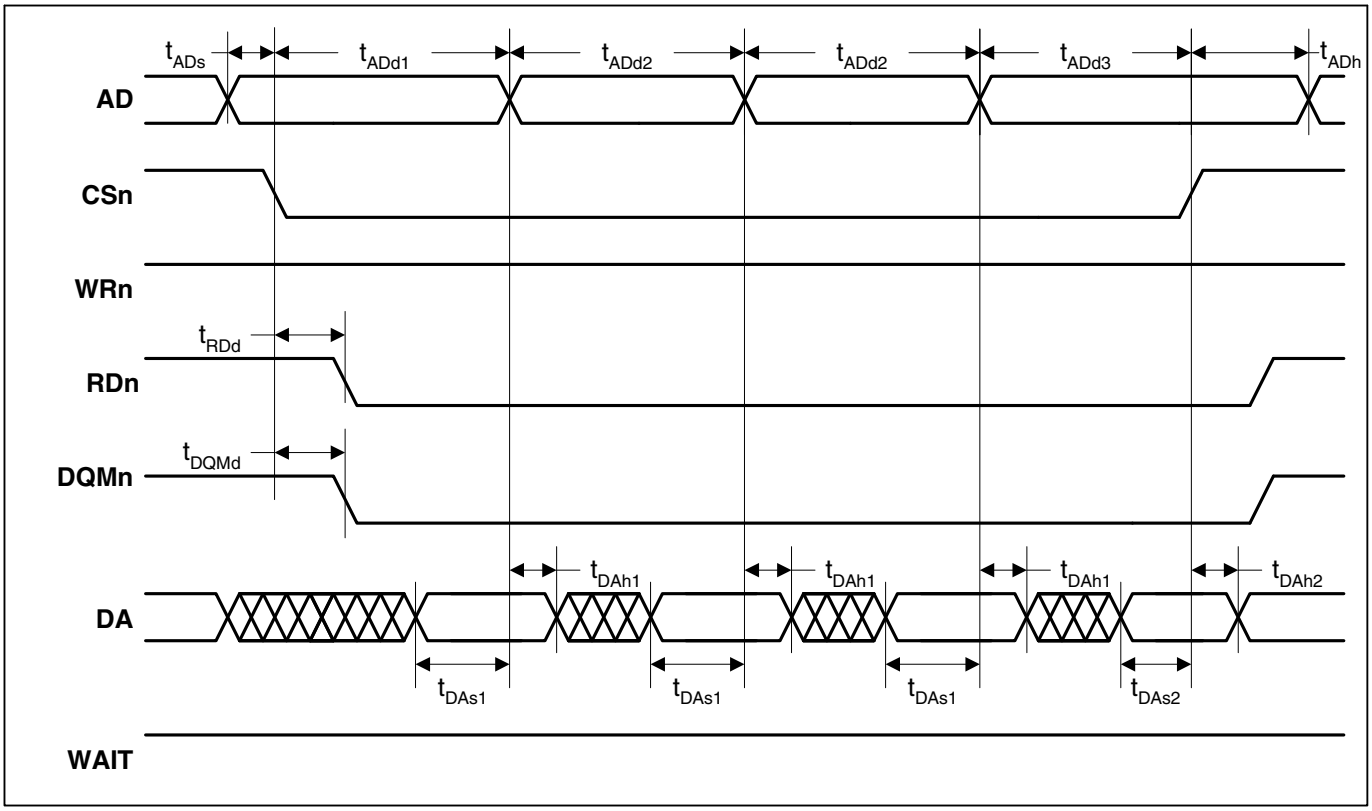

Figure 10. Static Memory Burst Read Cycle Timing Measurement

Static Memory Burst Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$			ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$			ns
WRN/DQMn deassert to AD transition time	t_{ADd}			$t_{HCLK} + 6$	ns
CSn hold from WRn deassert time	t_{CSh}	7			ns
CSn to WRn assert delay time	t_{WRd}			2	ns
CSn to DQMn assert delay time	t_{DQMd}			1	ns
DQMn assert time	t_{DQpwL}		$t_{HCLK} \times (WST1 + 1)$		ns
DQMn deassert time	t_{DQpwH}			$(t_{HCLK} \times 2) + 14$	ns
WRn assert time	t_{WRpwL}		$t_{HCLK} \times (WST1 + 11)$		ns
WRn deassert time	t_{WRpwH}			$(t_{HCLK} \times 2) + 7$	ns
WRn/DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}			ns
WRn/DQMn assert to DA valid time	t_{DAv}			8	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

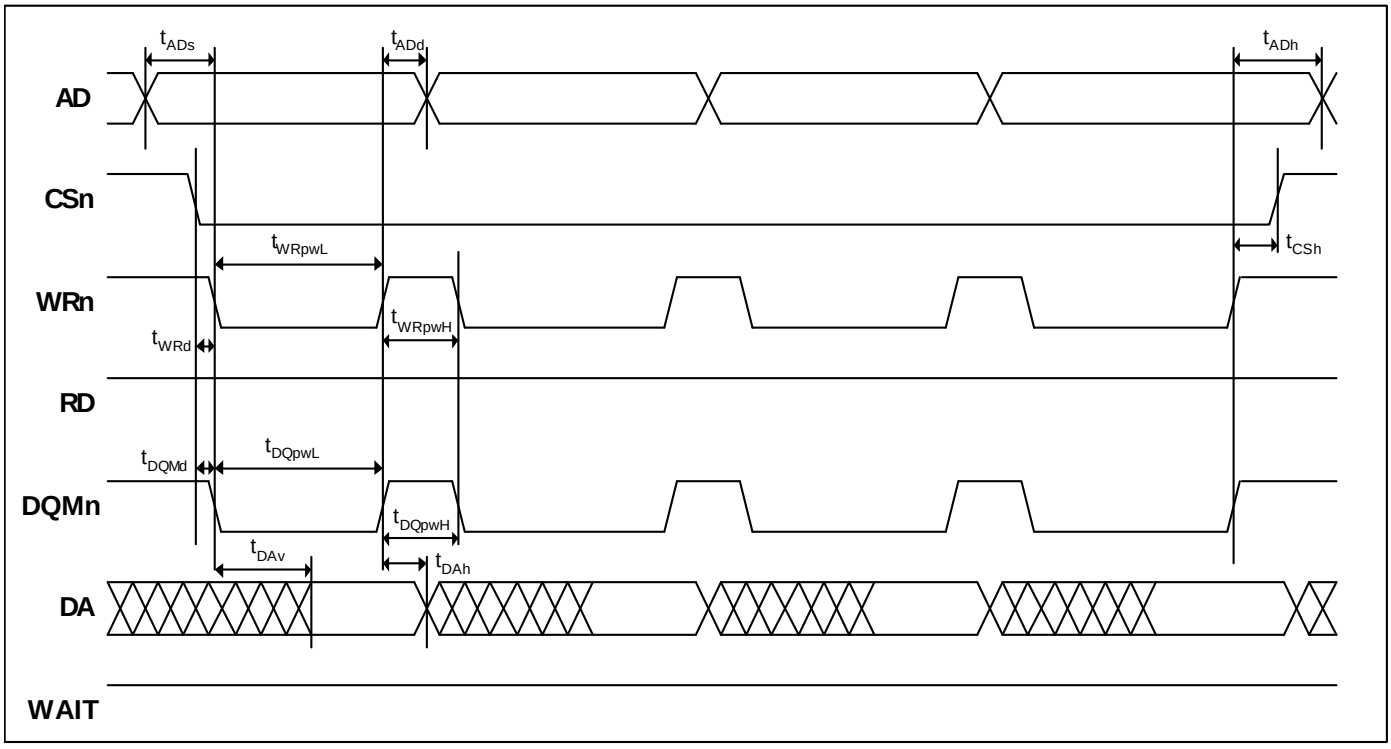

Figure 11. Static Memory Burst Write Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times$ (WST1-2)	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

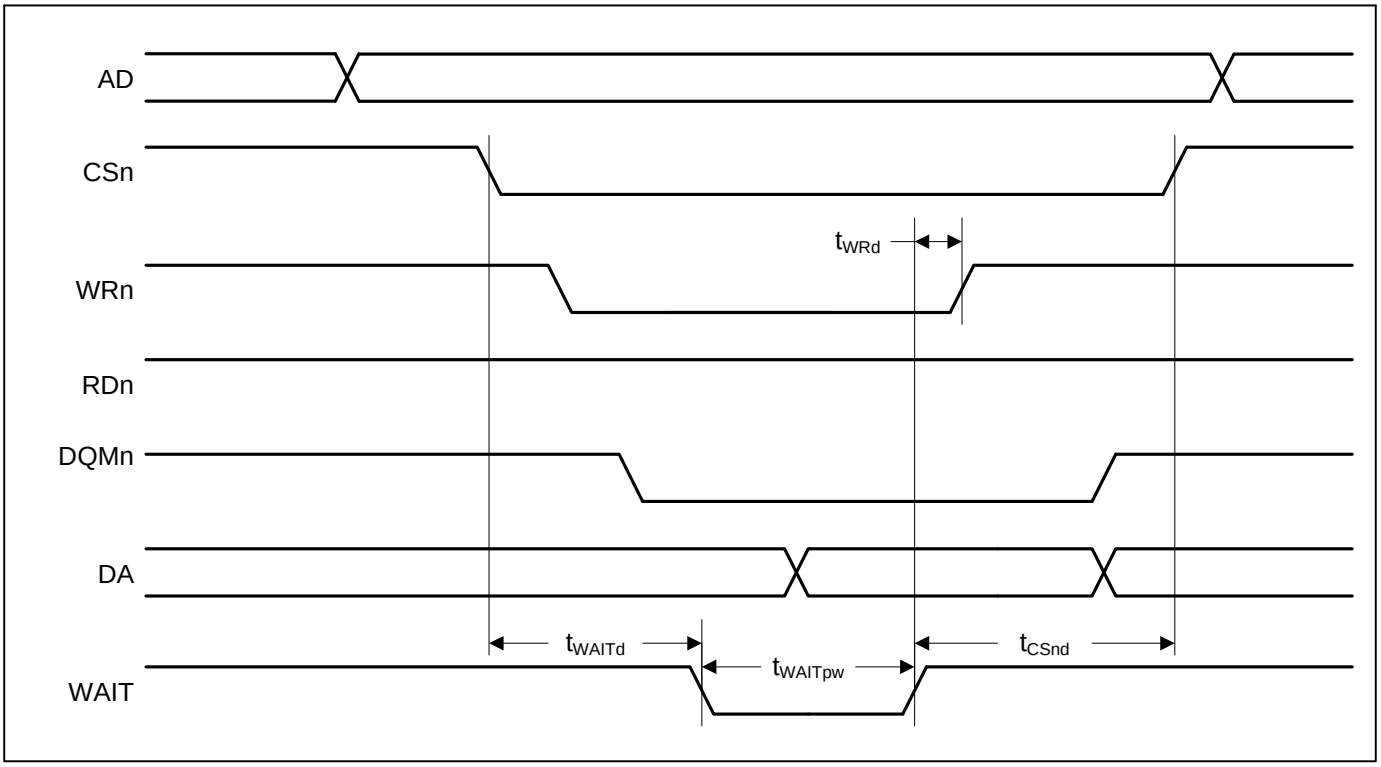

Figure 13. Static Memory Single Write Wait Cycle Timing Measurement

Static Memory Turnaround Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSnX deassert to CSnY assert time	t_{BTcyc}	-	$t_{HCLK} \times (IDCY+1)$	-	ns

Notes: 1. X and Y represent any two chip select numbers.
2. IDCY occurs on read-to-write and write-to-read.
3. IDCY is honored when going from a asynchronous device (CSx) to a synchronous device (/SDCSy).

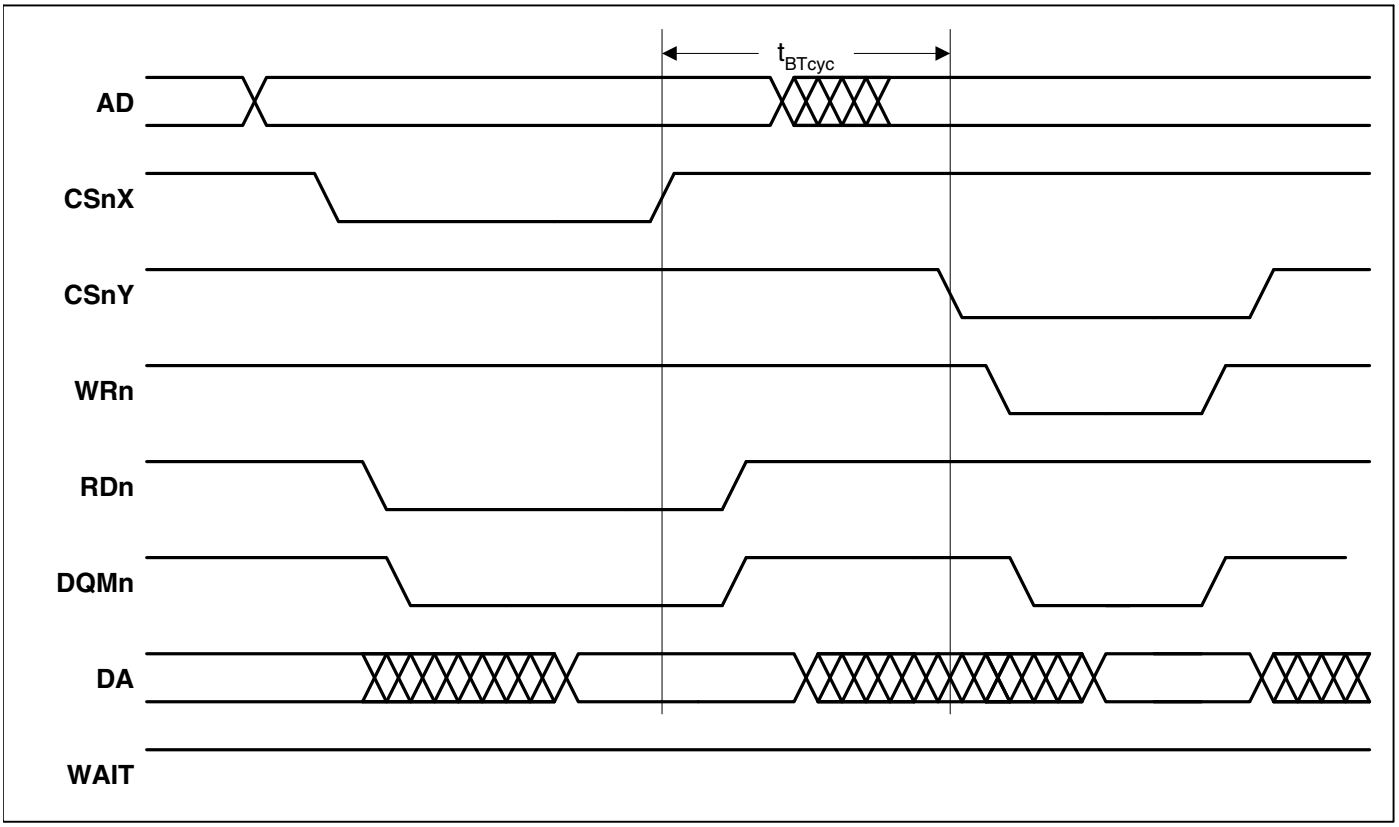

Figure 14. Static Memory Turnaround Cycle Timing Measurement

Inter-IC Sound - I²S

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	t_{i2s_clk}	-	ns
SCLK high time	t_{clk_high}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK low time	t_{clk_low}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK rise/fall time	t_{clkrf}	1	4	8	ns
SCLK to LRCLK assert delay time	t_{LRd}	-	-	3	ns
Hold between SCLK assert then LRCLK deassert *or* Hold between LRCLK deassert then SCLK assert	t_{LRh}	0	-	-	ns
SDI to SCLK deassert setup time	t_{SDIs}	12	-	-	ns
SDI from SCLK deassert hold time	t_{SDIh}	0	-	-	ns
SCLK assert to SDO delay time	t_{SDOd}	-	-	9	ns
SDO from SCLK assert hold time	t_{SDOh}	1	-	-	ns

Note: t_{i2s_clk} is programmable by the user.

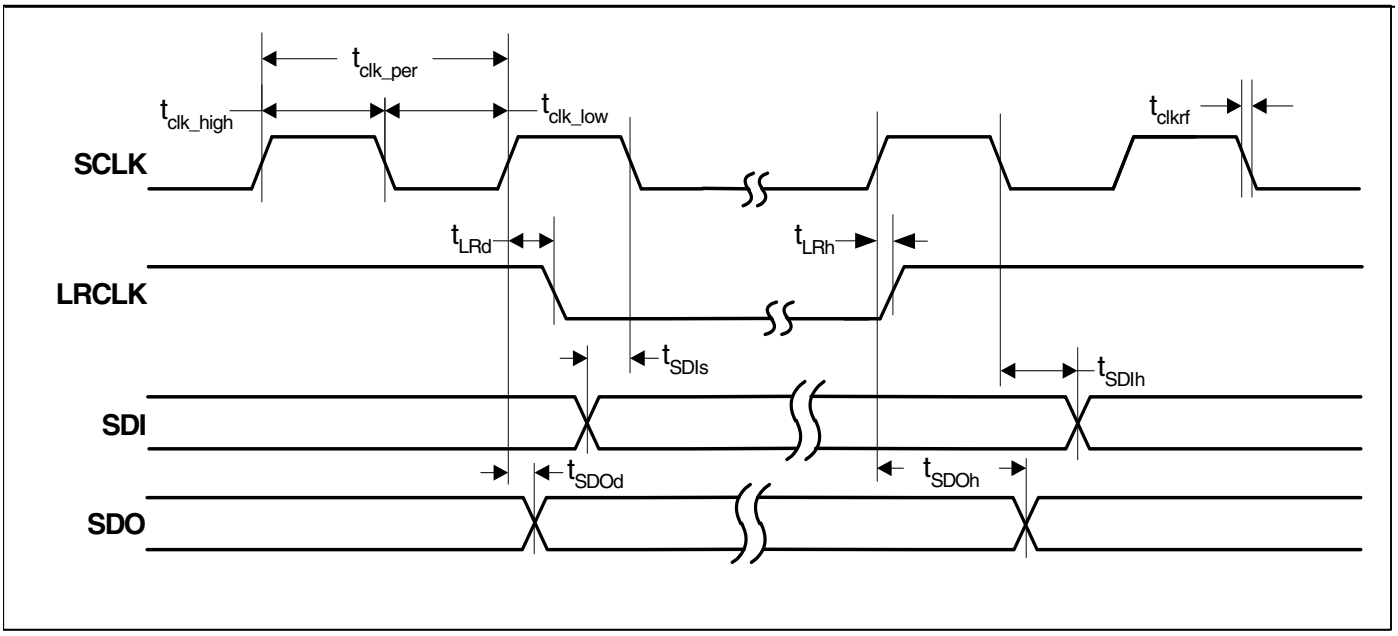

Figure 19. Inter-IC Sound (I^2S) Timing Measurement

JTAG

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	100	-	ns
TCK clock high time	t_{clk_high}	50	-	ns
TCK clock low time	t_{clk_low}	50	-	ns
TMS / TDI to clock rising setup time	t_{JPs}	20	-	ns
Clock rising to TMS / TDI hold time	t_{JPh}	45	-	ns
JTAG port clock to output	t_{JPco}	-	30	ns
JTAG port high impedance to valid output	t_{JPzx}	-	30	ns
JTAG port valid output to high impedance	t_{JPxz}	-	30	ns

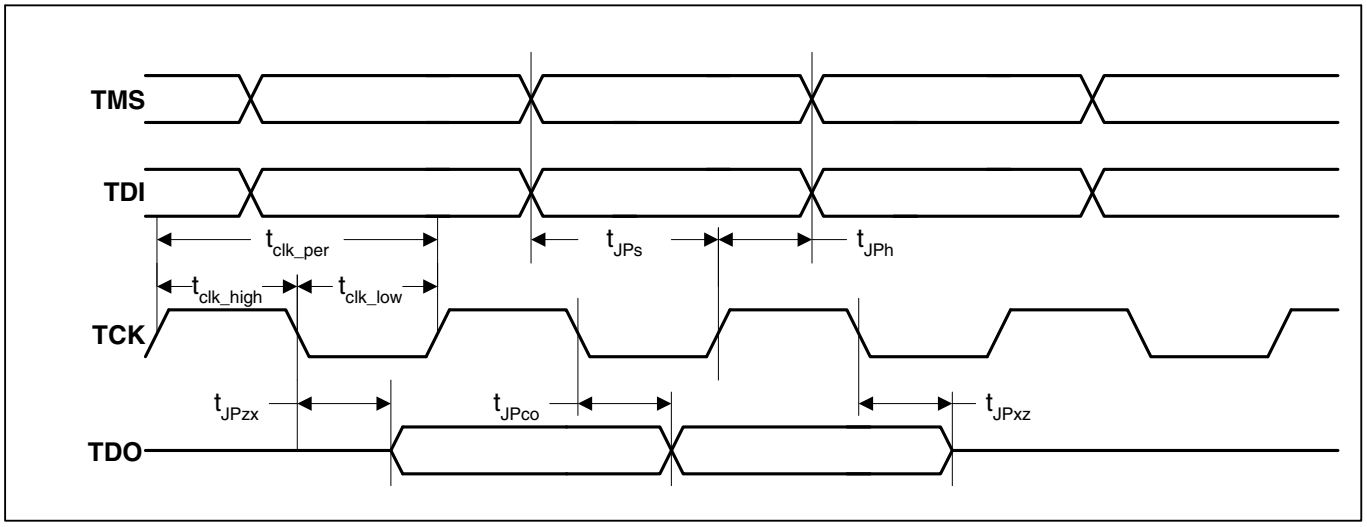

Figure 22. JTAG Timing Measurement

Table R illustrates the pin signal multiplexing and configuration options.

Table R. Pin Multiplex Usage Information

Physical Pin Name	Description	Multiplex signal name
EGPIO[0]	Ring Indicator Input	RI
EGPIO[1]	1Hz clock monitor	CLK1HZ
EGPIO[3]	HDLC Clock	HDLCCLK1
EGPIO[4]	I2S Transmit Data 1	SDO1
EGPIO[5]	I2S Receive Data 1	SDI1
EGPIO[6]	I2S Transmit Data 2	SDO2
EGPIO[7]	DMA Request 0	DREQ0
EGPIO[8]	DMA Acknowledge 0	DACK0
EGPIO[9]	DMA EOT 0	DEOT0
EGPIO[10]	DMA Request 1	DREQ1
EGPIO[11]	DMA Acknowledge 1	DACK1
EGPIO[12]	DMA EOT 1	DEOT1
EGPIO[13]	I2S Receive Data 2	SDI2
EGPIO[14]	PWM1 Output	PWMOUT1
EGPIO[15]	Device active / present	DASP
ABITCLK	I2S Serial clock	SCLK
ASYNC	I2S Frame Clock	LRCK
ASDO	I2S Transmit Data 0	SDO0
ASDI	I2S Receive Data 0	SDI0
ARSTn	I2S Master clock	MCLK
SCLK1	I2S Serial clock	SCLK
SFRM1	I2S Frame Clock	LRCK
SSPTX1	I2S Transmit Data 0	SDO0
SSPRX1	I2S Receive Data 0	SDI0

Acronyms and Abbreviations

The following tables list abbreviations and acronyms used in this data sheet.

Term	Definition
ADC	Analog-to-Digital Converter
ALT	Alternative
AMBA	Advanced Micro-controller Bus Architecture
ATAPI	ATA Packet Interface
CODEC	COder / DECoder
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct-Memory Access
EBUS	External Memory Bus
EEPROM	Electronically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
FIFO	First In / First Out
FIQ	Fast Interrupt Request
FLASH	Flash memory
GPIO	General Purpose I/O
HDLC	High-level Data Link Control
I/F	Interface
I^2S	Inter-IC Sound
IC	Integrated Circuit
ICE	In-Circuit Emulator
IDE	Integrated Drive Electronics
IEEE	Institute of Electronics and Electrical Engineers
IrDA	Infrared Data Association
IRQ	Standard Interrupt Request
ISO	International Standards Organization
JTAG	Joint Test Action Group
LFSR	Linear Feedback Shift Register
MII	Media-independent Interface
MMU	Memory Management Unit
OHCI	Open Host Controller Interface
PHY	Ethernet PHYsical layer interface
PIO	Programmed I/O
RISC	Reduced Instruction Set Computer
SDMI	Secure Digital Music Initiative
SDRAM	Synchronous Dynamic RAM
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STA	Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium
TFT	Thin Film Transistor
TLB	Translation Lookaside Buffer
USB	Universal Serial Bus

Units of Measurement

Symbol	Unit of Measure
^{o}C	degree Celsius
Hz	Hertz = cycle per second
kbps	kilobits per second
kbyte	kilobyte
kHz	kiloHertz = 1000 Hz
Mbps	Megabits per second
MHz	MegaHertz = 1,000 KiloHertz
µA	microAmpere = 10^{-6} Ampere
µs	microsecond = 1,000 nanoseconds = 10^{-6} seconds
mA	milliAmpere = 10^{-3} Ampere
ms	millisecond = 1,000 microseconds = 10^{-3} seconds
mW	milliWatt = 10^{-3} Watts
ns	nanosecond = 10^{-9} seconds
pF	picoFarad = 10^{-12} Farads
V	Volt
W	Watt