Understanding [Embedded - DSP (Digital Signal Processors)](#)

[Embedded - DSP (Digital Signal Processors)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP (Digital Signal Processors)](#)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	External Peripheral Interface
Clock Rate	20MHz
Non-Volatile Memory	OTP (8kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937120fsc00tr

GENERAL DESCRIPTION (Continued)

Note: All signals with an $\overline{\text{overline}}$ are active Low. For example in RD/$\overline{\text{WR}}$, RD is active High and $\overline{\text{WR}}$ is active Low.

The power connections follow the convention described below:

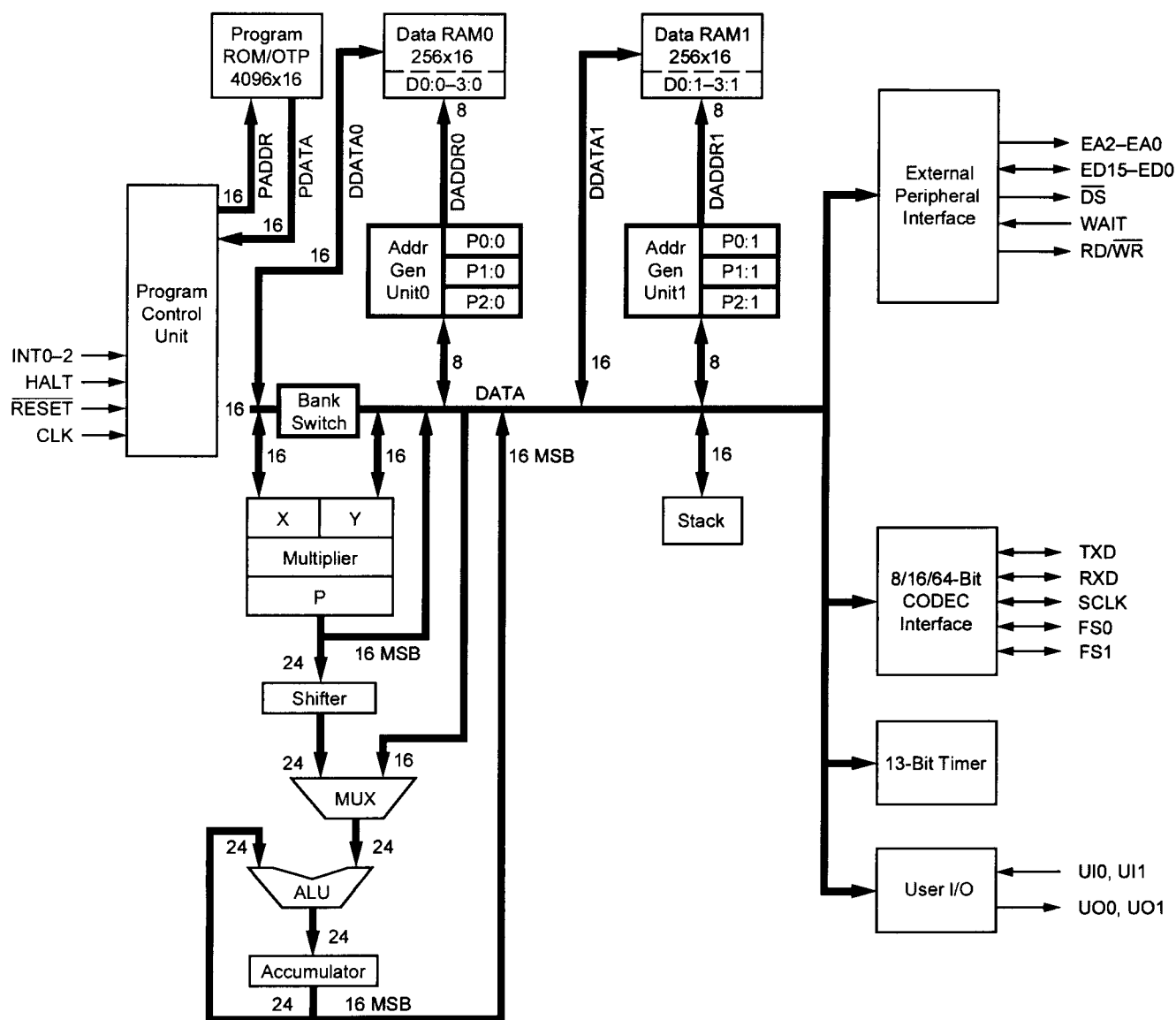| Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 1. Z893x1 Functional Block Diagram

PIN FUNCTIONS

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are *"external"* to the DSP core, and are used to access internal and external peripherals.
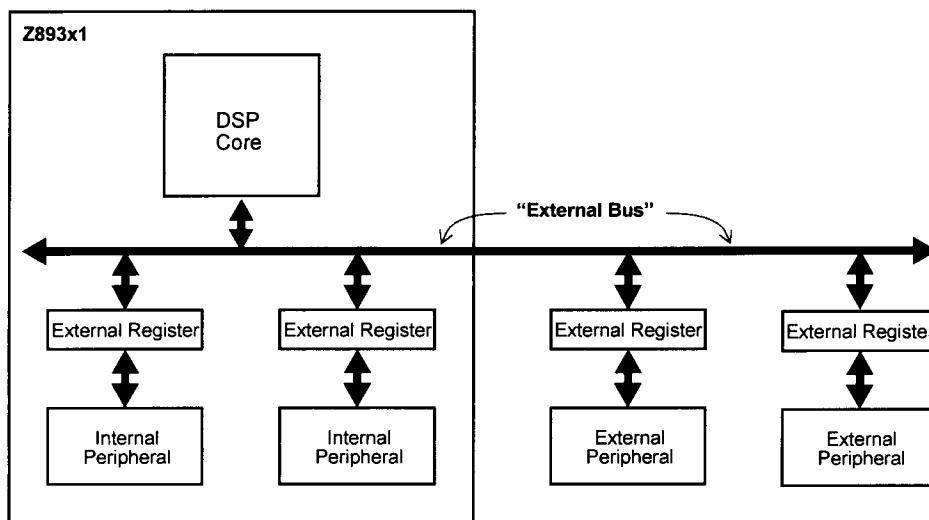

Figure 2. "External" Bus

EA2–EA0. External Address Bus (output).These pins control the user-defined register address output (latched). This bus is driven during both internal and external accesses. One of seven user-defined external registers is selected by the processor for reads or writes. External registers EXT0–EXT3 are always available to the user. External registers EXT4–EXT6 are used internally by the processor, or optionally by the user, if the pertinent internal peripherals are disabled. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers. The pins are normally tri-stated, except when these registers are specified as destination registers in a write instruction to an external peripheral. This bus uses the control signals RD/WR, DS, WAIT and the address pins EA2–EA0.

Note: The ED Bus was known as the EXT Bus in earlier versions of this document, and may be referred to as the EXT Bus, pins EXT15–EXT0, in other older related documents.

DS. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. DS is active for transfers to/from external peripherals only.

RD/WR. Read/Write Select (output). This pin controls the data direction signal for the ED Bus. Data is available from the processor on ED15–ED0 when this signal and DS are both Low.

WAIT. WAIT State (input). The wait signal is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin has an internal pull-down.

HALT. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains at the same value when this pin is held High. This pin has an internal pull-down.

INT0–INT2. Interrupts (input, positive edge triggered). These pins control interrupt requests 0–2. Interrupts are generated on the rising edge of the input signal. The DSP
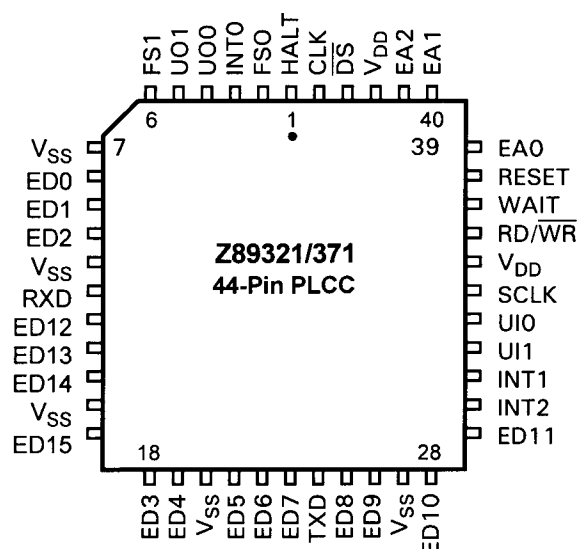
PIN DESCRIPTION (Continued)

Figure 4. Z89321/371 44-Pin PLCC Pin Assignments

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
1	HALT	Stop execution	Input
2	FS0	Frame Sync–CODEC Ch. 0	Output
3	INT0	Interrupt	Input
4	UO0	User Output	Output
5	UO1	User Output	Output
6	FS1	Frame Sync–CODEC Ch. 1	Output
7	V_{SS}	Ground	
8	ED0	External Data Bus	In/Out
9	ED1	External Data Bus	In/Out
10	ED2	External Data Bus	In/Out
11	V_{SS}	Ground	
12	RXD	Serial Input Data	Input
13	ED12	External Data Bus	In/Out
14	ED13	External Data Bus	In/Out
15	ED14	External Data Bus	In/Out
16	V_{SS}	Ground	
17	ED15	External Data Bus	In/Out
18	ED3	External Data Bus	In/Out
19	ED4	External Data Bus	In/Out
20	V_{SS}	Ground	
21	ED5	External Data Bus	In/Out
22	ED6	External Data Bus	In/Out

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
23	ED7	External Data Bus	In/Out
24	TXD	Serial Output Data	Output
25	ED8	External Data Bus	In/Out
26	ED9	External Data Bus	In/Out
27	V_{SS}	Ground	
28	ED10	External Data Bus	In/Out
29	ED11	External Data Bus	In/Out
30	INT2	Interrupt	Input
31	INT1	Interrupt	Input
32	UI1	User Input	Input
33	UI0	User Input	Input
34	SCLK	CODEC Serial Clock	Output
35	V_{DD}	Power Supply	Input
36	RD/$\overline{WR}$	Read/Write select for ED bus	Output
37	WAIT	Wait state	Input
38	RESET	Reset	Input
39	EA0	External Address bus	Output
40	EA1	External Address bus	Output
41	EA2	External Address bus	Output
42	V_{DD}	Power Supply	Input
43	$\overline{DS}$	Data Strobe for ED Bus	Output
44	CLK	Clock	Input

P R E L I M I N A R Y

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{DD}	Supply voltage with respect to V_{SS}	−0.3	7.0	V
T_{STG}	Storage Temperature	−65	150	°C
T_A	Ambient Operating Temperature			
	"S" device	0	70	°C
	"E" device	−40	85	°C

Stresses greater than those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground.

Positive current $I_{(+)}$ flows into the referenced pin.

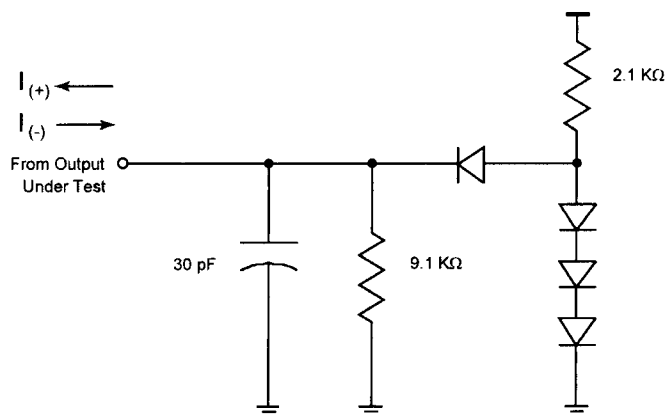Negative current $I_{(-)}$ flows out of the referenced pin.

Figure 6. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Table 4. V_{DD} = 5V ±10%, TA = 0°C to +70°C for "S" Temperature Range
(T_A = −40°C to +85°C for "E" temperature range, unless otherwise noted)

| Sym	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Supply Current	V_{DD} = 5.5V		70.0	TBD	mA
I_{DC}	DC Power Consumption	V_{DD} = 5.0V and CLK stopped High		5.0	TBD	mA
V_{IH}	Input High Level		2.7			V
V_{IL}	Input Low Level				0.8	V
I_L	Input Leakage				10	µA
V_{OH}	Output High Voltage	I_{OH} = −100 µA	V_{DD}−0.2			V
		I_{OH} = −160 µA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
		I_{OL} = 2.0 mA			0.5	V
I_{FL}	Output Floating Leakage Current				10	µA

TIMING DIAGRAMS
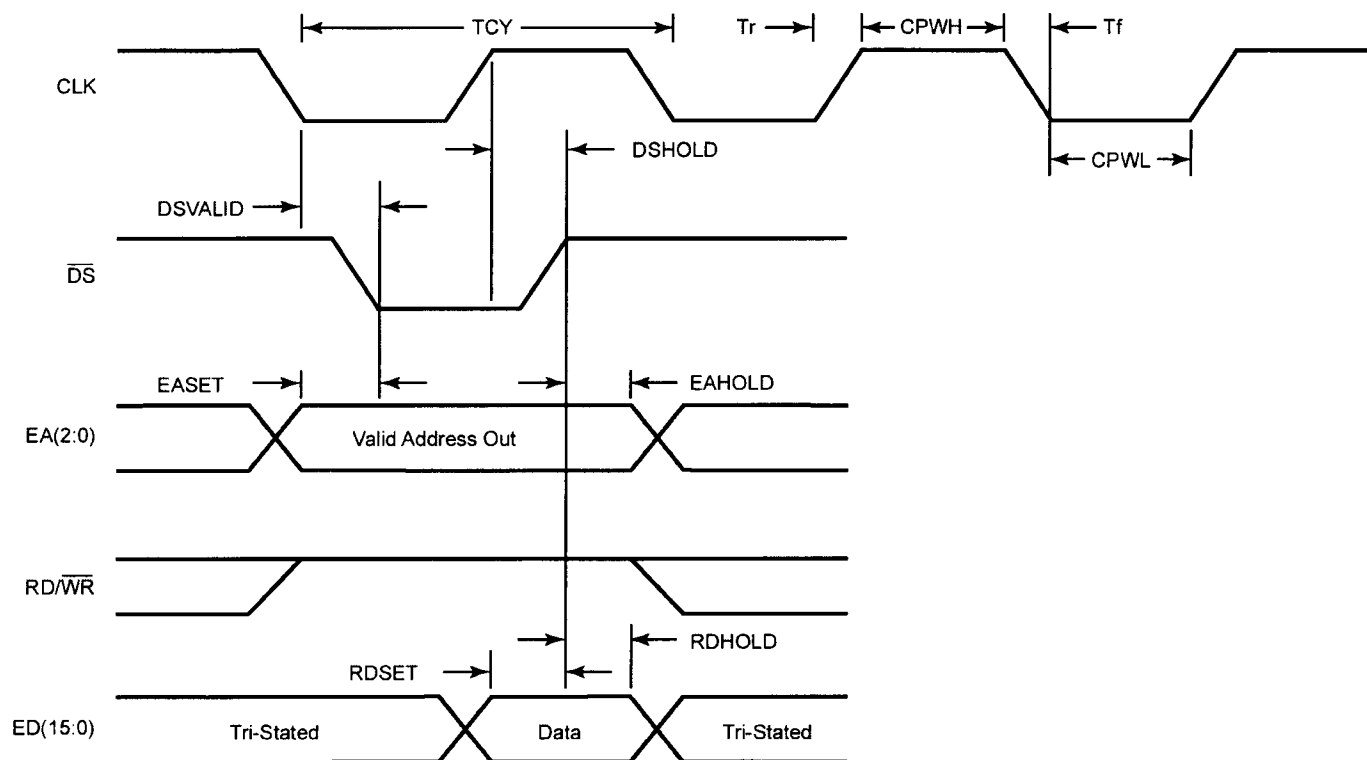
Figure 7. Read Timing
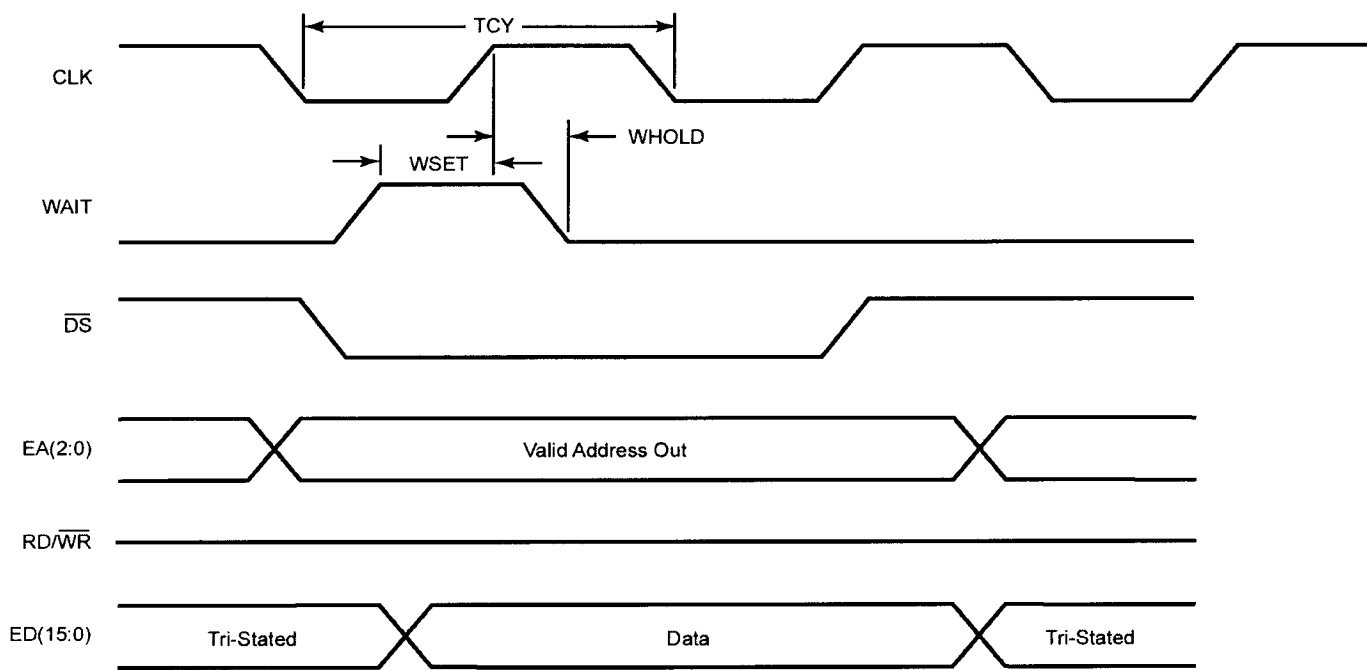
Figure 8. External Data (ED) Bus Read Timing Using WAIT Pin
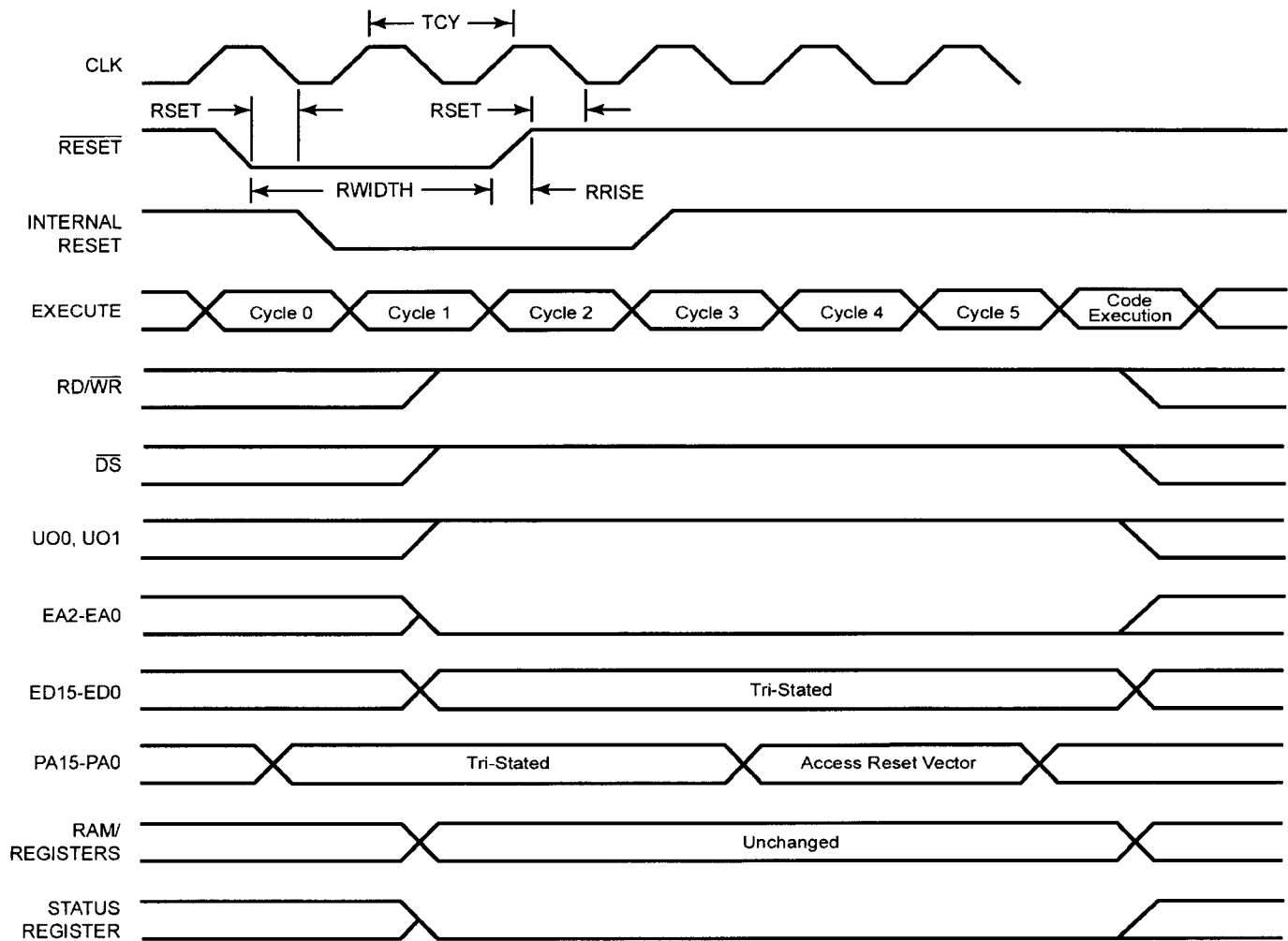
Figure 13. Synchronous Reset Timing

Interrupts. The Z893x1 has three positive edge-triggered interrupt inputs. An interrupt is serviced at the end of an instruction execution. Two machine cycles are required to enter an interrupt instruction sequence. The PC is pushed onto the stack. At the end of the interrupt service routine, a RET instruction is used to pop the stack into the PC. The priority of the interrupts is INT0 = highest, INT2 = lowest. When those peripherals are enabled, INT1 is dedicated to the CODEC Interface and INT2 is dedicated to the 13-bit timer.

The Set-Interrupt-Enable-Flag (SIEF) instruction enables the interrupts. Interrupts are automatically disabled when entering an interrupt service routine. Before exiting an interrupt service routine, the SIEF instruction can be used to re-enable interrupts.

Registers. The Z893x1 has 19 internal registers and up to seven user-defined 16-bit external registers (EXT0–EXT6). The external register address space for EXT4–EXT6 is used by the Z893x1 internal peripherals. Disabling a peripheral allows access to these addresses for general-purpose use.

External Register Usage. The external registers EXT0–EXT6 are accessed using the External Address Bus EA2–EA0, the External Data Bus (ED Bus) ED15–ED0, and control signals $\overline{DS}$, WAIT, and RD/$\overline{WR}$. These registers provide a convenient data transfer capability with external peripherals. Data transfers can be performed in a single-cycle. An internal Wait-State generator is provided to accommodate slower external peripherals. A single wait state can be implemented through control register EXT7–2. For ad-

ditional wait states, the WAIT pin can be used. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals on the ED bus.

Wait-State Generator. An internal Wait-State generator is provided to accommodate slow external peripherals. A single Wait-State can be implemented through a control register. For additional states, a dedicated pin (WAIT) can be held Low. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals (ED bus).

CODEC Interface. The CODEC Interface provides the necessary control signals for transmission of CODEC information to/from the processor. The CODEC Interface accommodates external 8-bit PCM or 16/64-bit linear CODECs. The CODEC Interface can also be used with external A/D and D/A converters. The interface can also be used as a high-speed serial port.

µ-Law Compression. The CODEC Interface provides optional hardware µ-Law compression from 13-bit format to 8-bit format. Decompression is performed in software using a 128-word lookup table.

Timers. Two programmable timers, a general purpose 13-bit Timer, and a dedicated 12-bit Counter/Timer are provided to support the CODEC Interface. The 13-bit Timer can be operated in either continuous or one-shot mode. If the CODEC Interface is not enabled, its 12-bit Counter/Timer is also available for general-purpose use.

REGISTERS

The internal registers are defined in Table 6 below:

Table 6. Register Definitions

Register	Definition
X	Multiplier X Input, 16-bits
Y	Multiplier Y Input, 16-bits
P	Multiplier Output, 24-bits
A	Accumulator, 24-bits
Pn:b	Six Data RAM Pointers, 8-bits each
PC	Program Counter, 16-bits
SR	Status Register, 16-bits
EXT4	13-bit Timer Configuration Register
EXT5–1	CODEC Interface Channel 0 Data
EXT5–2	CODEC Interface Channel 0 Data
EXT6–1	CODEC Interface Channel 1 Data
EXT6–2	CODEC Interface Channel 1 Data
EXT7–1	CODEC Interface Configuration Register
EXT7–2	Wait-State Generator and CODEC Interface Configuration Register

Note: The loading and reading of the three pairs of CODEC Interface registers (EXT5–1,2 EXT6–1,2 and EXT7–1,2) are described in the CODEC Interface section.

X and **Y** are two 16-bit input registers for the multiplier. These registers can be utilized as temporary registers when the multiplier is not being used.

P holds the result of multiplications and is read-only.

A is a 24-bit Accumulator. The output of the ALU is sent to this register. When 16-bit data is transferred into this register, it is placed into the 16 MSBs, and the least significant eight bits are set to zero. Only the upper 16 bits are transferred to the destination register when the Accumulator is selected as a source register in transfer instructions.

Pn:b are the pointer registers for accessing data RAM where n = 0, 1, or 2, and b = 0 or 1. These registers can perform either a direct read or write function, and each can point to locations in data RAM.

PC is the Program Counter. Any instruction which may modify this register requires two clock cycles.

SR is the status register. It contains the ALU status and processor control bits (Table 7).

Table 7. Status Register Bit Functions

SR Bit	Function	Read/Write
S15 (N)	ALU Negative	RO
S14 (OV)	ALU Overflow	RO
S13 (Z)	ALU Zero	RO
S12 (L)	Carry	RO
S11 (UI1)	User Input 1	RO
S10 (UI0)	User Input 0	RO
S9 (SH3)	MPY Output Arithmetically Shifted Right by Three Bits	R/W
S8 (OP)	Overflow Protection	R/W
S7 (IE)	Interrupt Enable	R/W
S6 (UO1)	User Output 1	R/W
S5 (UO0)	User Output 0	R/W
S4–S3	"Short Form Direct" bits	R/W
S2–S0 (RPL)	RAM Pointer Loop Size	R/W

Note: RO = read only, RW = read/write. The status register can always be read in its entirety.

S15–S12 are set/reset by the ALU after an operation.

S11–S10 are set/reset by the user inputs.

If S9 is set, and a multiply/shift option is used, the shifter shifts the result three bits right. This feature allows the data to be scaled and prevents overflows.

If S8 is set, the hardware clamps at maximum positive or negative values instead of overflowing.

S7 enables interrupts.

S6–S0 are control bits.

REGISTERS (Continued)

Table 8. RPL Description

S2	S1	S0	Loop Size
0	0	0	256
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The following are not actually registers; however, they have a read/write function that acts primarily the same way as the hardware registers do on the chip:

Register	Register Definition
BUS	DDATA Bus
Dn:b	Program Memory Pointers
EXTn	External Registers

BUS is a read-only register which, when accessed, returns the contents of the D-Bus. BUS is used for emulation only.

Dn:b refers to locations in RAM that can be used as a pointer to locations in program memory. These locations make the Z89321/371 capable for coefficient addressing. The programmer decides which location to choose from based on two bits in the status register and two bits in the operand; only the lower 16 possible locations in RAM can be specified. At any one time, there are eight usable pointers, four per bank, and the four pointer are in consecutive locations in RAM. For example, if S3/S4=1 in the status register, then D0:0/D1:0/D2:0/D3:0 refer to register locations 4/5/6/7 in RAM Bank 0.

Note: When the data pointers are being written to, a number is actually being loaded to Data RAM. In effect, these data pointers can be used as a limited method for writing to RAM.

EXT0–EXT3 are used to map external peripherals into the address space of the processor.

Note: The actual register RAM does not exist on the chip, but would exist as part of the external device (such as an A/D result latch). The External Address Bus, EA2–EA0, the External Data Bus, $\overline{ED15}$–ED0 and the control signals $\overline{DS}$, WAIT and RD/$\overline{WR}$, are used to access external peripherals.

EXT4 is used by the 13-bit Timer. If the Timer is disabled, then this address can be used to access an external peripheral on the External Data Bus.

EXT5 and **EXT6** are used by the CODEC Interface channels 0 and 1 respectively. If a CODEC channel is disabled, the corresponding address can be used to access an external peripheral.

EXT7 is used to program wait states for EXT0–EXT6, and is not available for accessing an external peripheral.

If both the Timer and CODEC Interface are disabled, there are 7 addresses available to access external peripherals.

If both the Timer and CODEC Interface are enabled, there are 4 addresses available to access external peripherals.

Figure 17. Status Register

EXT4

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Count Value (down-counter)

Clock Source
0 = CLK/2 (default)
1 = CODEC Counter Output

Count Operation
0 = Stop (default)
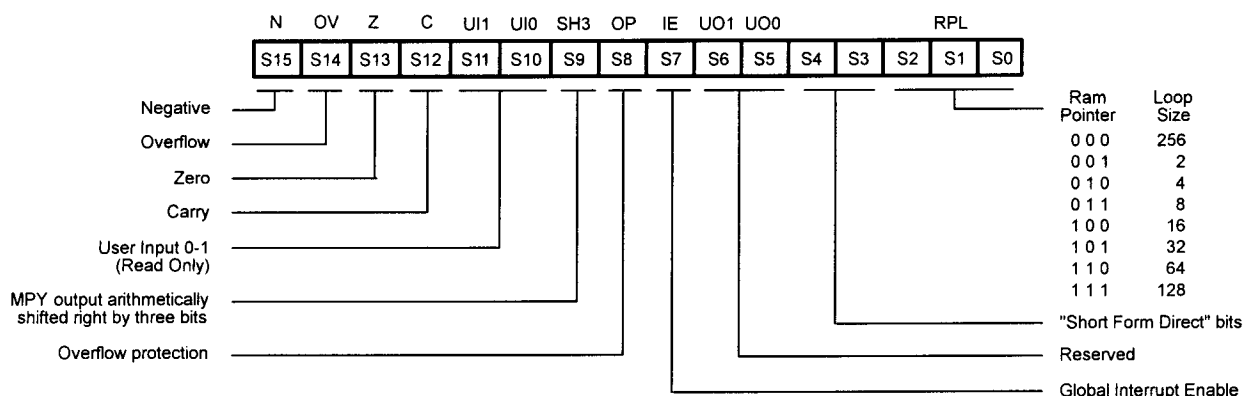1 = Run

Counter
0 = Disable
1 = Enable (default)

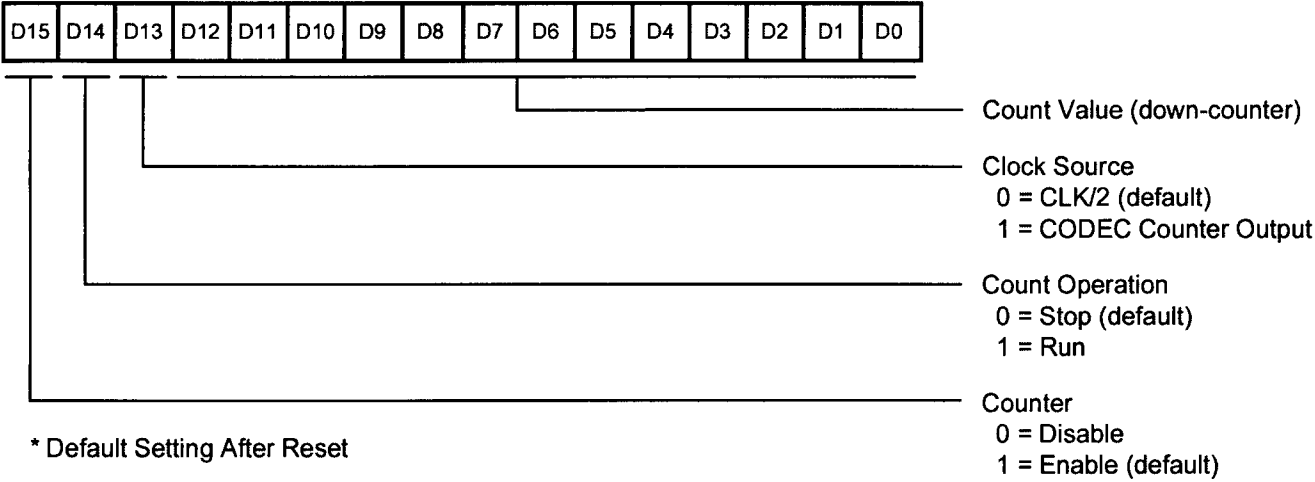* Default Setting After Reset

Figure 18. Timer Register EXT4

FS0, FS1. Frame Sync 0 and Frame Sync 1 (output). These pins are used to mark data transfer/receive frames. The rising and falling edge of the Frame Sync signals indicate the beginning and the end of each serial data transmission.

CODEC Interface Interrupt Behavior

When the transmission of serial data is completed, the CODEC Interface generates an internal interrupt which vectors to the INT1 service routine address. This interrupt is coincident with the falling edge of FS1. The following clarifies the behavior of the CODEC Interface interrupt:

- While the CODEC Interface is enabled, it utilizes the INT1 service routine address.

- The CODEC Interface will be disabled after $\overline{RESET}$.

- The INT1 pin has an internal pull-down.

- If INT1 is tied High, the CODEC Interface generates an interrupt at the end of each frame transfer.

- If INT1 is not connected, or tied Low, the CODEC Interface not only generates an interrupt when first enabled, but generates an interrupt at the end of each frame transfer.

- When the CODEC Interface is disabled, INT1 can be controlled by an external peripheral.

Note: In single channel applications, use Channel 1 because INT1 coincides with FS1, not FS0.

Registers

The CODEC Interface registers (EXT5, EXT6 and EXT7) each act as a 2-deep FIFO. See the CODEC Interface Block Diagram for more information, Figure 19. Two operations may be required for some data transfers.

EXT5 and **EXT6.** The CODEC Interface constantly transfers and receives data during normal operation. The reading of receive data, and the writing of transmit data, are interleaved.

An example of Channel 1 operation in 8 or 16-bit mode, where one can wait for the input data, is as follows:

LD<dest>, EXT6	; Read previous input data from EXT6–1
LD EXT6, <xmit data>	; Push current data from EXT6–2 to EXT6–1 ; Load EXT6–2 with data to be transmitted

To obtain the input data as soon as it arrives, and extra instruction is required:

LD EXT6,<anything>	; Push current input data from EXT6–2 to EXT6–1
LD<test>, EXT6	; Read current input data from EXT6–1
LD EXT6, <xmit data>	; Load EXT6–2 with data to be transmitted

For 64-bit mode, one can use the following code sequence:

LD <Ch. 0 MSW input dest>, EXT5	; Get MSW of Ch. 0 input
LD <Ch. 1 MSW input dest>, EXT6	; Get MSW of Ch 1 input
LD EXT5, <Ch. 0 MSW output data>	; Move LSB of Ch. 0 input and Load MSW of output
LD EXT6, <Ch. 1 MSW output data>	; Move LSB of Ch. 1 input and Load MSW of output
LD<Ch. 0 LSW input test>, EXT5	; Get LSW of Ch. 0 input
LD<Ch. 1 LSW input test>, EXT6	; Get LSW of Ch. 1 input
LD EXT5, <Ch. 0 LSW output data>	; Load LSW of Ch. 0 output
LD EXT6, <Ch. 1 LSW output data>	; Load LSW of Ch. 1 output

Note: EXT# denotes EXT5 or EXT6.

In the 8 and 16-bit modes, EXT5–2 and EXT6–2 are the shift registers for Channel 0 and Channel 1, respectively. In 8-bit mode, the 8-bits reside in the least significant byte for both transmit and receive. In 64-bit mode, the output/input order is EXT 5–1 first, followed by EXT5–2, EXT6–1, and finally by EXT6–2. In all modes, the MSB is shifted out/in first.

Channel 0 uses FS0, EXT5–1, and EXT5–2. Channel 1 uses FS1, EXT6–1, and EXT6–2.

EXT7. This register contains the configuration information for the CODEC Interface and the Wait-State Generator. In normal operation, the user writes configuration data for EXT7–1 followed by configuration data for EXT7–2.

Write EXT7	LD EXT7, <config data1>	; Move data to 7–2
	LD EXT7, <config data2>	; Move data to 7–1

CODEC INTERFACE (Continued)
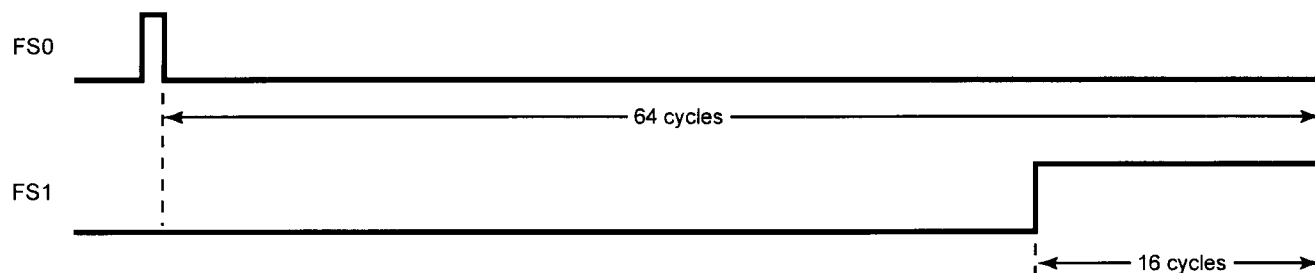
Figure 20. 64-Bit CODEC Frame Synchronization
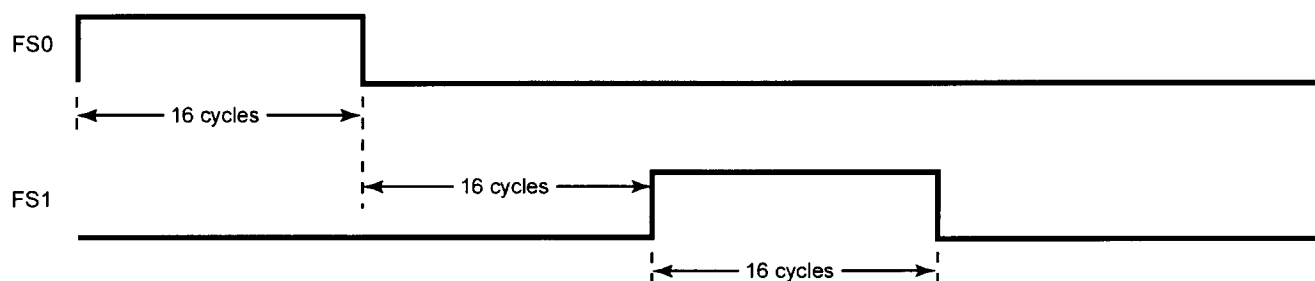
Figure 21. 16-Bit CODEC Frame Synchronization
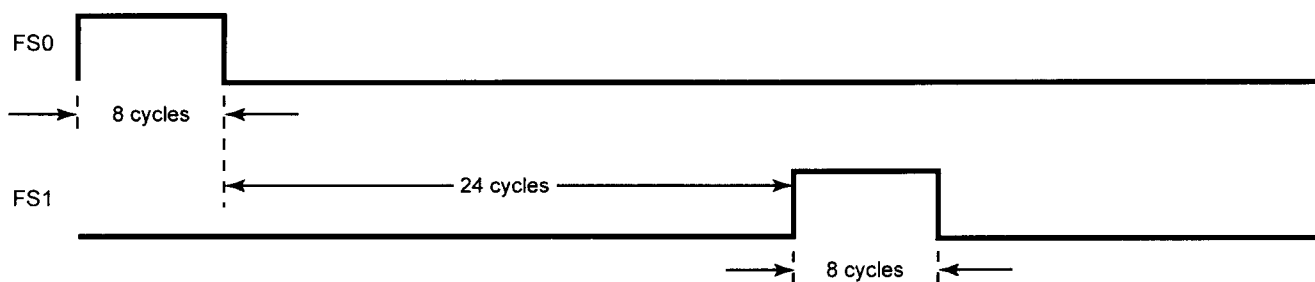
Figure 22. 8-Bit CODEC Frame Synchronization

CODEC INTERFACE (Continued)

EXT7-1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SCLK Prescaler Value (up-counter)

SCLK/FSYNC Ratio Prescaler Value (up-counter)

CODEC Mode
00 = 8-bit with Hardware μ-Law
01 = 8-bit without Hardware μ-Law
10 = 16-bit Linear
11 = 64-bit Stereo

FSYNC
0 = Disable (default)
1 = Enable

CODEC Channel 0
0 = Disable (default)
1 = Enable

Example:EXT7-1 = #%x00DCLK = 12.288 MHz, SCLK = 2.048 MHz, FSYNC = 8 kHz
EXT7-1 = #%x00DCLK = 12.288 MHz, SCLK = 2.048 MHz, FSYNC = 8 kHz
EXT7-1 = #%xFFxNo interrupt
EXT7-1 = #%x000Max interrupt period (667 μs for CLK = 12.288 MHz)

Figure 23. CODEC Interface Control Register

EXT7-2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Wait State EXT0

Wait State EXT1

Wait State EXT2

Wait State EXT3

Wait State EXT4

Wait State EXT5

Wait State EXT6

SCLK
0 = Disable (default)
1 = CLK/2

CODEC Channel 1
0 = Disable (default)
1 = Enable

00 read (nws), write (nws)
01 read (nws), write (ws)
10 read (ws), write (nws)
11 read (ws), write (ws)

nws = no wait states
ws = one wait state

Figure 24. Wait-State Generator and CODEC Interface Control Register

INSTRUCTION SET

The addressing modes are:

<pregs>, <hwregs> These modes are used for loads to and from registers within the chip, such as loading to the accumulator, or loading from a pointer register. The names of the registers are specified in the operand field (destination first, then source).

<dregs> This mode is used for access to the lower 16 addresses in each bank of RAM. The 4-bit address comes from 2 bits of the status register and 2 bits of the operand field of the data pointer. Data registers can be used to access data in RAM, but typically these registers are used as pointers to access data from the program memory.

<accind> Similar to the previous mode, the address for the program memory read is stored in the Accumulator. Hence, @A in the second operand field loads the number in memory specified by the address in A.

<direct> The direct mode allows read or write to data RAM from the Accumulator by specifying the absolute address of the RAM in the operand of the instruction. A number between 0 and 255 indicates a location in RAM bank 0, and a number between 256 and 511 indicates a location in RAM bank 1.
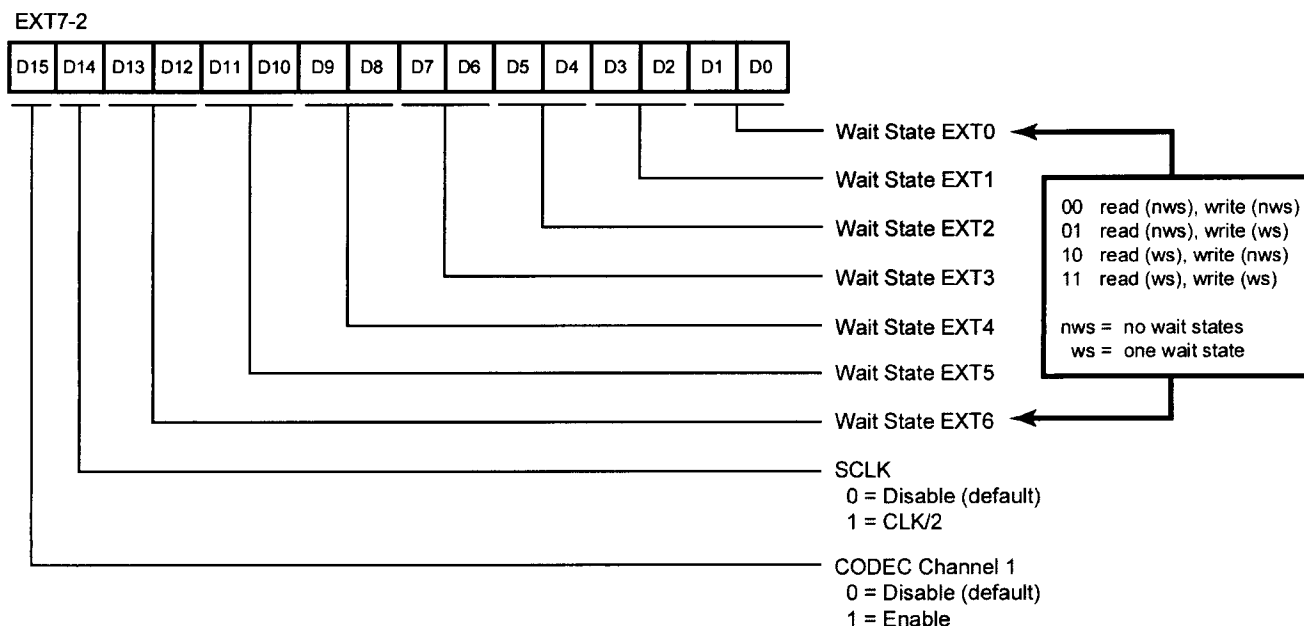
<limm> This address mode indicates a long immediate operand. A 16-bit word can be loaded directly from the operand into the specified register or memory location.

<simm> This address mode indicates a short immediate operand. It is used to load 8-bit data into the specified RAM pointer.

<regind> This mode is used for indirect access to the data RAM. The address of the RAM location is stored in the pointer. The "@" symbol indicates "indirect" and precedes the pointer. For example, @P1:1 refers to the location in RAM bank 1 specified by the value in the pointer.

<memind> This mode is used for indirect access to the program memory. The address of the memory is located in a RAM location, which is specified by the value in a pointer. Therefore, @@P1:1 instructs the processor to read from a location in memory. This instruction specifies a value in RAM, and the location of the RAM is, in turn, specified by the value in the pointer.

Note: The data pointer can also be used for a memory access in this manner, but only one "@" precedes the pointer. In both cases, each time the addressing mode is used, the memory address stored in RAM is incremented by one to allow easy transfer of sequential data from program memory.

Table 9. Instruction Set Addressing Modes

Symbolic Name	Syntax	Description
<pregs>	Pn:b	Pointer Registers
<dregs> (points to RAM)	Dn:b	Data Registers
<hwregs>	X, Y, PC, SR, P, EDn, A, BUS	Hardware Registers
<accind> (points to Program Memory)	@A	Accumulator Memory Indirect
<direct>	<expression>	Direct Address Expression
<limm>	#<const exp>	Long (16-bit) Immediate Value
<simm>	#<const exp>	Short (8-bit) Immediate Value
<regind> (points to RAM)	@Pn:b	Pointer Register Indirect
	@Pn:b+	Pointer Register Indirect with Increment
	@Pn:b–LOOP	Pointer Register Indirect with Loop Decrement
	@Pn:b+LOOP	Pointer register Indirect with Loop Increment
<memind> (points to Program Memory)	@@Pn:b	Pointer Register Memory Indirect
	@Dn:b	Data Register Memory Indirect
	@@Pn:b–LOOP	Pointer Register Memory Indirect with Loop Decrement
	@@Pn:b+LOOP	Pointer Register Memory Indirect with Loop Increment
	@@Pn:b+	Pointer Register Memory Indirect with Increment

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the < cc > (condition code) symbol in one of its addressing modes, the instruction will only execute if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	No Interrupts Enabled
NOV	No Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

INSTRUCTION DESCRIPTIONS

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
ABS	Absolute Value	ABS[<cc>,]<src>	<cc>,A	1	1	ABS NC, A
			A	1	1	ABS A
ADD	Addition	ADD<dest>,<src>	A,<pregs>	1	1	ADD A,P0:0
			A,<dregs>	1	1	ADD A,D0:0
			A,<limm>	2	2	ADD A,#%1234
			A,<memind>	1	3	ADD A,@@P0:0
			A,<direct>	1	1	ADD A,%F2
			A,<regind>	1	1	ADD A,@P1:1
			A,<hwregs>	1	1	ADD A,X
			A,<simm>	1	1	ADD A, #%12
AND	Bitwise AND	AND<dest>,<src>	A,<pregs>	1	1	AND A,P2:0
			A,<dregs>	1	1	AND A,D0:1
			A,<limm>	2	2	AND A,#%1234
			A,<memind>	1	3	AND A,@@P1:0
			A,<direct>	1	1	AND A,%2C
			A,<regind>	1	1	AND A,@P1:2+LOOP
			A,<hwregs>	1	1	AND A,EXT3
			A,<simm>	1	1	AND A, #%12
CALL	Subroutine call	CALL [<cc>,]<address>	<cc>,<direct>	2	2	CALL Z,sub2
			<direct>	2	2	CALL sub1
CCF	Clear C flag	CCF	None	1	1	CCF
CIEF	Clear IE Flag	CIEF	None	1	1	CIEF
COPF	Clear OP flag	COPF	None	1	1	COPF
CP	Comparison	CP<src1>,<src2>	A,<pregs>	1	1	CP A,P0:0
			A,<dregs>	1	1	CP A,D3:1
			A,<memind>	1	3	CP A,@@P0:1
			A,<direct>	1	1	CP A,%FF
			A,<regind>	1	1	CP A,@P2:1+
			A,<hwregs>	1	1	CP A,STACK
			A,<limm>	2	2	CP A,#%FFCF
			A,<simm>	1	1	CP A, #%12
DEC	Decrement	DEC [<cc>,]<dest>	<cc>,A	1	1	DEC NZ,A
			A	1	1	DEC A
INC	Increment	INC [<cc>,] <dest>	<cc>,A	1	1	INC PL,A
			A	1	1	INC A
JP	Jump	JP [<cc>,]<address>	<cc>,<direct>	2	2	JP C,Label
			<direct>	2	2	JP Label
LD	Load destination with source	LD<dest>,<src>	A,<hwregs>	1	1	LD A,X
			A,<dregs>	1	1	LD A,D0:0
			A,<pregs>	1	1	LD A,P0:1
			A,<regind>	1	1	LD A,@P1:1
			A,<memind>	1	3	LD A,@D0:0
			A,<direct>	1	1	LD A,124
			<direct>,A	1	1	LD 124,A
			<dregs>,<hwregs>	1	1	LD D0:0,EXT7
			<pregs>,<simm>	1	1	LD P1:1,#%FA
			<pregs>,<hwregs>	1	1	LD P1:1,EXT1
			<regind>,<limm>	1	1	LD@P1:1,#1234
			<regind>,<hwregs>	1	1	LD @P1:1+,X
			<hwregs>,<pregs>	1	1	LD Y,P0:0
			<hwregs>,<dregs>	1	1	LD SR,D0:0
			<hwregs>,<limm>	2	2	LD PC,#%1234
			<hwregs>,<accind>	1	3	LD X,@A
			<hwregs>,<memind>	1	3	LD Y,@D0:0
			<hwregs>,<regind>	1	1	LD A,@P0:0–LOOP
			<hwregs>,<hwregs>	1	1	LD X,EXT6

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples

Notes:
1. When <dest> is <hwregs>, <dest> cannot be P.
2. When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR.
3. When <src> is <accind> <dest> cannot be A.

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MLD	Multiply	MLD <src1>,<src2> [,<bank switch>]	<hwregs>,<regind>	1	1	MLD A,@P0:0+LOOP
			<hwregs>,<regind>,<bank switch>	1	1	MLD A,@P1:0,OFF
			<regind>,<regind>	1	1	MLD @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MLD @P0:1,@P1:0,ON

Notes:
1. If src1 is <regind> it must be a bank 1 register. Src2's <regind must be a bank 0 register.
2. <hwregs> for src1 cannot be X.
3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MPYA	Multiply and add	MPYA <src1>,<src2> [,<bank switch>]	<hwregs>,<regind>	1	1	MPYA A,@P0:0
			<hwregs>,<regind>,<bank switch>	1	1	MPYA A,@P1:0,OFF
			<regind>,<regind>	1	1	MPYA @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MPYA@P0:1,@P1:0,ON

Notes:
1. If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.
2. <hwregs> for src1 cannot be X.
3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MPYS	Multiply and subtract	MPYS <src1>,<src2> [,<bank switch>]	<hwregs>,<regind>	1	1	MPYS A,@P0:0
			<hwregs>,<regind>,<bank switch>	1	1	MPYS A,@P1:0,OFF
			<regind>,<regind>	1	1	MPYS @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MPYS @P0:1,@P1:0,ON

Notes:
1. If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.
2. <hwregs> for src1 cannot be X.
3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON.

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
NEG	Negate	NEG <cc>,A	<cc>, A	1	1	NEG MI,A
			A	1	1	NEG A
NOP	No operation	NOP	None	1	1	NOP
OR	Bitwise OR	OR <dest>,<src>	A,<pregs>	1	1	OR A,P0:1
			A,<dregs>	1	1	OR A, D0:1
			A,<limm>	2	2	OR A,#%2C21
			A,<memind>	1	3	OR A,@@P2:1+
			A,<direct>	1	1	OR A, %2C
			A,<regind>	1	1	OR A,@P1:0–LOOP
			A,<hwregs>	1	1	OR A,EXT6
			A,<simm>	1	1	OR A,#%12
POP	Pop value from stack	POP <dest>	<pregs>	1	1	POP P0:0
			<dregs>	1	1	POP D0:1
			<regind>	1	1	POP @P0:0
			<hwregs>	1	1	POP A

PACKAGE INFORMATION

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
⌀	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH
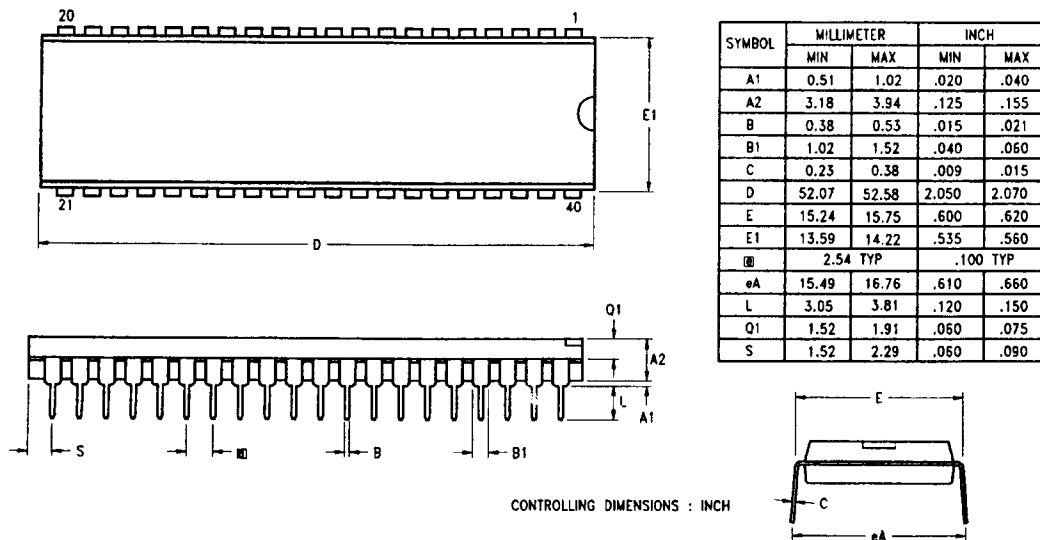
Figure 25. 40-Pin Package Diagram

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
⌀	1.27 TYP		.050 TYP	
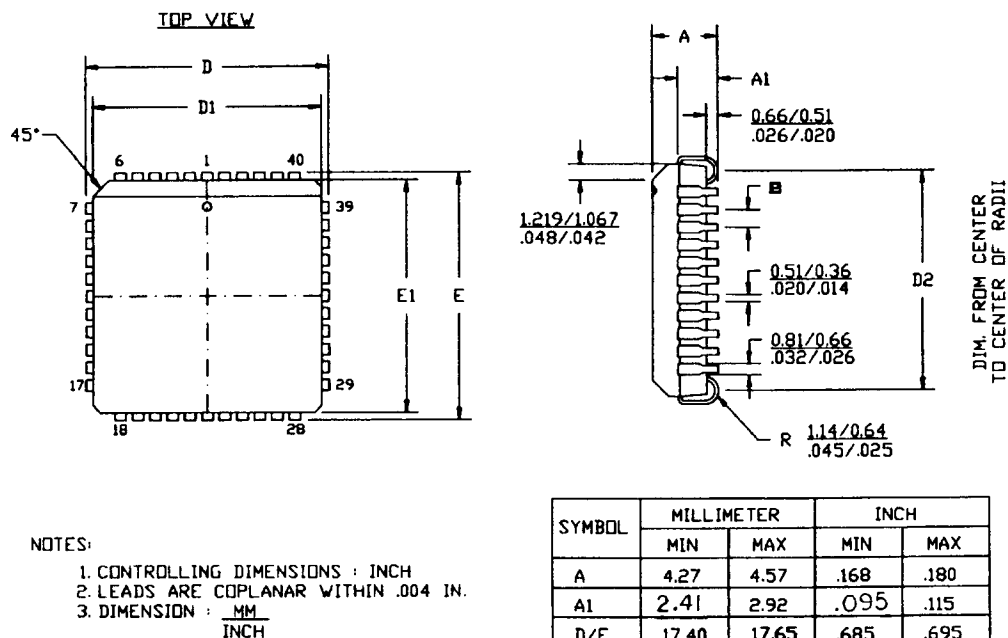
Figure 26. 44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
⊡	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10
                                .004"

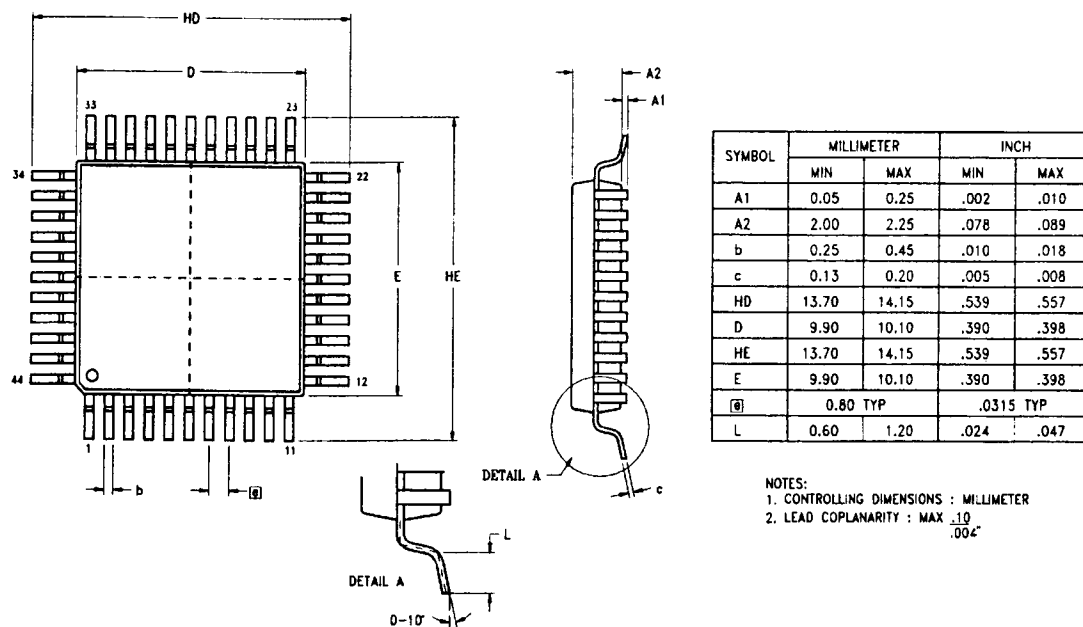**Figure 27.** 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z89321

Z8932120PSC
Z8932120VSC
Z8932120VEC
Z8932120FSC
Z8932120FEC

Z89371

Z8937120PSC
Z8937120VSC
Z8937120FSC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

Package	P = Plastic DIP
	V = Plastic PLCC
	F = Plastic LQFP
Temperature	S = 0°C to +70°C
	E = –40°C to 85°C
Speed	20 = 20 MHz
Environmental	C = Plastic Standard

Example:
Z 89321 20 V S C   is a Z89321, 20 MHz, PLCC, 0° to +70°C, Plastic Standard Flow

- Environmental Flow
- Temperature
- Package
- Speed
- Product Number
- ZiLOG Prefix