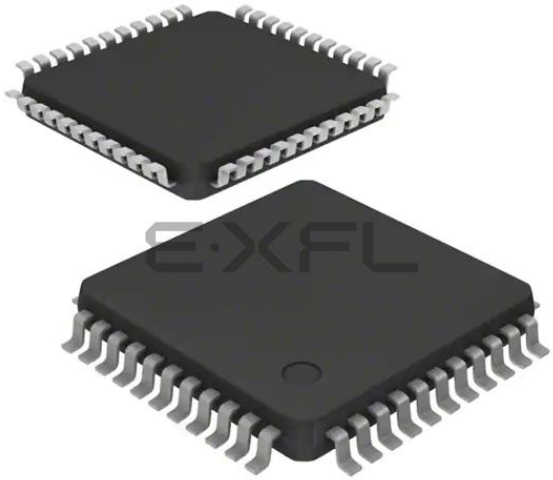

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	External Peripheral Interface
Clock Rate	20MHz
Non-Volatile Memory	OTP (8kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937120fsg

PIN FUNCTIONS

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are *"external"* to the DSP core, and are used to access internal and external peripherals.

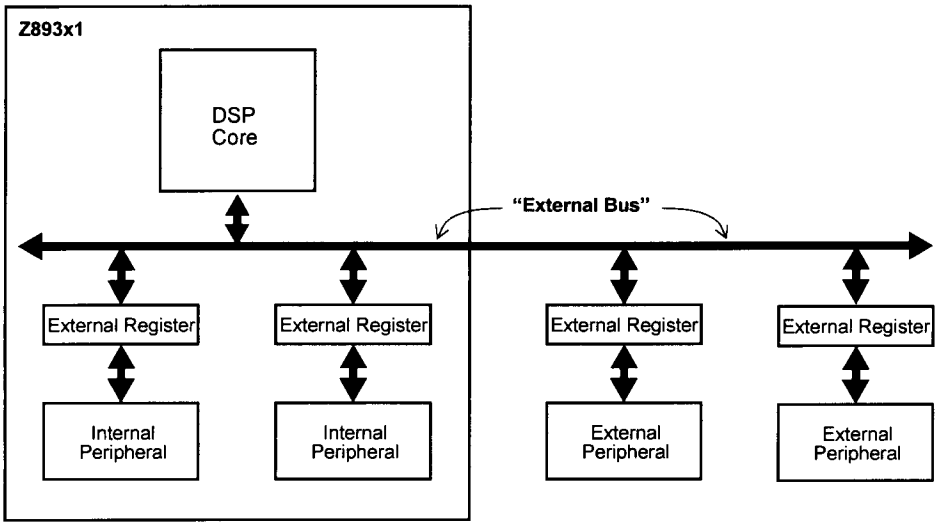


Figure 2. "External" Bus

EA2–EA0. External Address Bus (output).These pins control the user-defined register address output (latched). This bus is driven during both internal and external accesses. One of seven user-defined external registers is selected by the processor for reads or writes. External registers EXT0–EXT3 are always available to the user. External registers EXT4–EXT6 are used internally by the processor, or optionally by the user, if the pertinent internal peripherals are disabled. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers. The pins are normally tri-stated, except when these registers are specified as destination registers in a write instruction to an external peripheral. This bus uses the control signals RD/$\overline{WR}$, $\overline{DS}$, WAIT and the address pins EA2–EA0.

Note: The ED Bus was known as the EXT Bus in earlier versions of this document, and may be referred to as the EXT Bus, pins EXT15–EXT0, in other older related documents.

$\overline{DS}$. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. DS is active for transfers to/from external peripherals only.

RD/$\overline{WR}$. Read/$\overline{Write}$ Select (output). This pin controls the data direction signal for the ED Bus. Data is available from the processor on ED15–ED0 when this signal and $\overline{DS}$ are both Low.

WAIT. WAIT State (input). The wait signal is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin has an internal pull-down.

HALT. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains at the same value when this pin is held High. This pin has an internal pull-down.

INT0–INT2. Interrupts (input, positive edge triggered). These pins control interrupt requests 0–2. Interrupts are generated on the rising edge of the input signal. The DSP

PIN FUNCTIONS (Continued)

fetches the interrupt service routine starting addresses from the following program memory locations:

Device	INT0	INT1	INT2
Z89321/371	0FFFH	0FFEH	0FFDH
Z89391	FFFFH	FFFEH	FFFDH

The interrupt priority is INT0 = highest, INT2 = lowest. These pins have internal pull-downs.

Note: INT1 and INT2 pins are not available on the 40-pin DIP package.

CLK Clock (input). This pin is the clock circuit input.

$\overline{\text{RESET}}$. Reset (input, active Low). This pin resets the processor. It pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH (or FFFCH for the Z89391) after the RESET signal is released. The Status register is set to all zeros. At power-up, RAM and other registers are undefined; however, they are left unchanged with subsequent resets. RESET can be asserted asynchronously. If the rising edge of RESET meets prescribed setup conditions relative to the falling edge of the clock, the processor commences execution with a fixed number of clock cycles later. See the Timing Diagrams definitions for details.

UI0, UI1. User Input (input). These general-purpose input pins are directly tested by the conditional branch instructions. The pins can also be read as bits in the status register. These are asynchronous input signals that have no special clock synchronization requirements.

UO0, UO1. User Output (output). These general-purpose output pins reflect the value of two bits in the status register. These bits may be used to output data by writing to the status register.

Note: The value at the output pin is inverted from the value in the register.

The pins **SCLK, FS0, FS1, RXD** and **TXD** are described in the CODEC Interface section.

PIN DESCRIPTION (Continued)

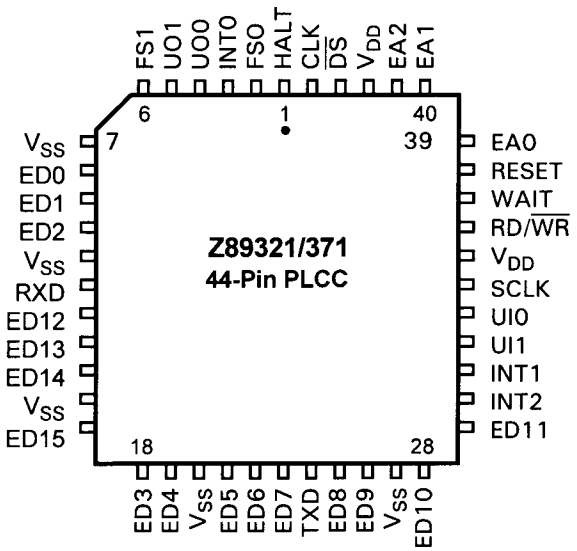


Figure 4. Z89321/371 44-Pin PLCC Pin Assignments

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
1	HALT	Stop execution	Input
2	FS0	Frame Sync–CODEC Ch. 0	Output
3	INT0	Interrupt	Input
4	UO0	User Output	Output
5	UO1	User Output	Output
6	FS1	Frame Sync–CODEC Ch. 1	Output
7	V_{SS}	Ground	
8	ED0	External Data Bus	In/Out
9	ED1	External Data Bus	In/Out
10	ED2	External Data Bus	In/Out
11	V_{SS}	Ground	
12	RXD	Serial Input Data	Input
13	ED12	External Data Bus	In/Out
14	ED13	External Data Bus	In/Out
15	ED14	External Data Bus	In/Out
16	V_{SS}	Ground	
17	ED15	External Data Bus	In/Out
18	ED3	External Data Bus	In/Out
19	ED4	External Data Bus	In/Out
20	V_{SS}	Ground	
21	ED5	External Data Bus	In/Out
22	ED6	External Data Bus	In/Out

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
23	ED7	External Data Bus	In/Out
24	TXD	Serial Output Data	Output
25	ED8	External Data Bus	In/Out
26	ED9	External Data Bus	In/Out
27	V_{SS}	Ground	
28	ED10	External Data Bus	In/Out
29	ED11	External Data Bus	In/Out
30	INT2	Interrupt	Input
31	INT1	Interrupt	Input
32	UI1	User Input	Input
33	UI0	User Input	Input
34	SCLK	CODEC Serial Clock	Output
35	V_{DD}	Power Supply	Input
36	RD/$\overline{WR}$	Read/$\overline{Write}$ select for ED bus	Output
37	WAIT	Wait state	Input
38	RESET	Reset	Input
39	EA0	External Address bus	Output
40	EA1	External Address bus	Output
41	EA2	External Address bus	Output
42	V_{DD}	Power Supply	Input
43	$\overline{DS}$	Data Strobe for ED Bus	Output
44	CLK	Clock	Input

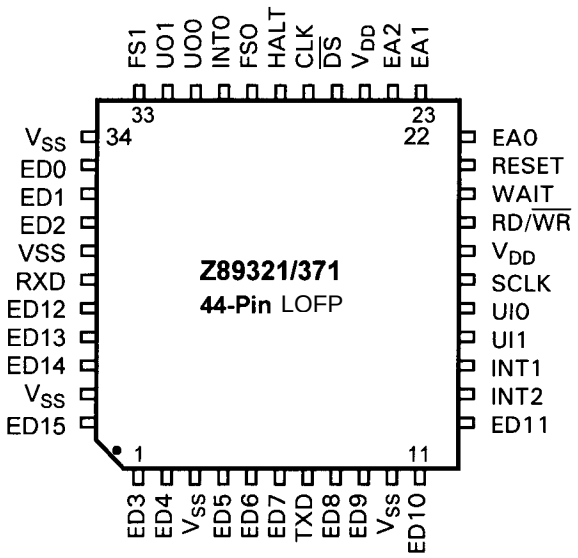


Figure 5. Z89321/371 44-Pin LOFP Pin Assignments

Table 3. Z89321/371 44-Pin LOFP Pin Identification

No.	Symbol	Function	Direction
1	ED3	External Data Bus	In/Out
2	ED4	External Data Bus	In/Out
3	V_{SS}	Ground	
4	ED5	External Data Bus	In/Out
5	ED6	External Data Bus	In/Out
6	ED7	External Data Bus	In/Out
7	TXD	Serial Output Data	Output
8	ED8	External Data Bus	In/Out
9	ED9	External Data Bus	In/Out
10	V_{SS}	Ground	
11	ED10	External Data Bus	In/Out
12	ED11	External Data Bus	In/Out
13	INT2	Interrupt	Input
14	INT1	Interrupt	Input
15	UI1	User Input	Input
16	UI0	User Input	Input
17	SCLK	CODEC Serial Clock	Output
18	V_{DD}	Power Supply	Input
19	RD/$\overline{WR}$	Read/$\overline{Write}$ select for ED bus	Output
20	WAIT	Wait state	Input
21	RESET	Reset	Input
22	EA0	External Address bus	Output

Table 3. Z89321/371 44-Pin LOFP Pin Identification

No.	Symbol	Function	Direction
23	EA1	External Address bus	Output
24	EA2	External Address bus	Output
25	V_{DD}	Power Supply	Input
26	$\overline{DS}$	Data Strobe for ED Bus	Output
27	CLK	Clock	Input
28	HALT	Stop execution	Input
29	FS0	Frame Sync–CODEC Ch. 0	Output
30	INT0	Interrupt	Input
31	UO0	User Output	Output
32	UO1	User Output	Output
33	FS1	Frame Sync–CODEC Ch. 1	Output
34	V_{SS}	Ground	
35	ED0	External Data Bus	In/Out
36	ED1	External Data Bus	In/Out
37	ED2	External Data Bus	In/Out
38	V_{SS}	Ground	
39	RXD	Serial Input Data	Input
40	ED12	External Data Bus	In/Out
41	ED13	External Data Bus	In/Out
42	ED14	External Data Bus	In/Out
43	V_{SS}	Ground	
44	ED15	External Data Bus	In/Out

AC ELECTRICAL CHARACTERISTICS

Table 5. V_{DD} = 5V ±10%, T_A = 0°C to +70°C for "S" Temperature Range (T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted)

Symbol	Parameter	Min [ns]	Max [ns]
Clock			
TCY	CLK Cycle Time	50	31250
CPWH	CLK Pulse Width High	21	
CPWL	CLK Pulse Width Low	21	
Tr	CLK Rise Time		2
Tf	CLK Fall Time		2
External Peripheral Bus			
DSVALID	$\overline{DS}$ Valid Time from CLK Fall	0	15
DSHOLD	$\overline{DS}$ Hold Time from CLK Rise	0	15
EASET	EA Setup Time to $\overline{DS}$ Fall	10	
EAHOLD	EA Hold Time from $\overline{DS}$ Rise	4	
RWSET	Read/Write Setup Time to $\overline{DS}$ Fall	10	
RWHOLD	Read/Write Hold Time from $\overline{DS}$ Rise	0	
RDSET	Data Read Setup Time to $\overline{DS}$ Rise	15	
RDHOLD	Data Read Hold Time from $\overline{DS}$ Rise	0	
WRVALID	Data Write Valid Time from $\overline{DS}$ Fall		5
WRHOLD	Data Write Hold Time from $\overline{DS}$ Rise	2	
Reset			
RSET	Reset Setup Time to CLK Fall for synchronous operation	15	
RWIDTH	Reset Low Pulse Width	2 TCY	
RRISE	Reset Rise Time		50
Interrupt			
INTSET	Interrupt Setup Time to CLK Fall	7	
INTWIDTH	Interrupt Low Pulse Width	1 TCY	
Halt			
HSET	Halt Setup Time to CLK Rise	4	
HHOLD	Halt Hold Time from CLK Rise	12	
Wait State			
WSET	Wait Setup Time to CLK Rise	20	
WHOLD	Wait Hold Time from CLK Rise	10	
CODEC Interface			
SSET	SCLK Setup Time from CLK Rise		15
FSSET	FSYNC Setup Time from SCLK Rise		7
TXSET	TXD Setup Time from SCLK Rise		7
RXSET	RXD Setup Time to SCLK Fall	7	
RXHOLD	RXD Hold Time from SCLK Fall	0	

TIMING DIAGRAMS (Continued)

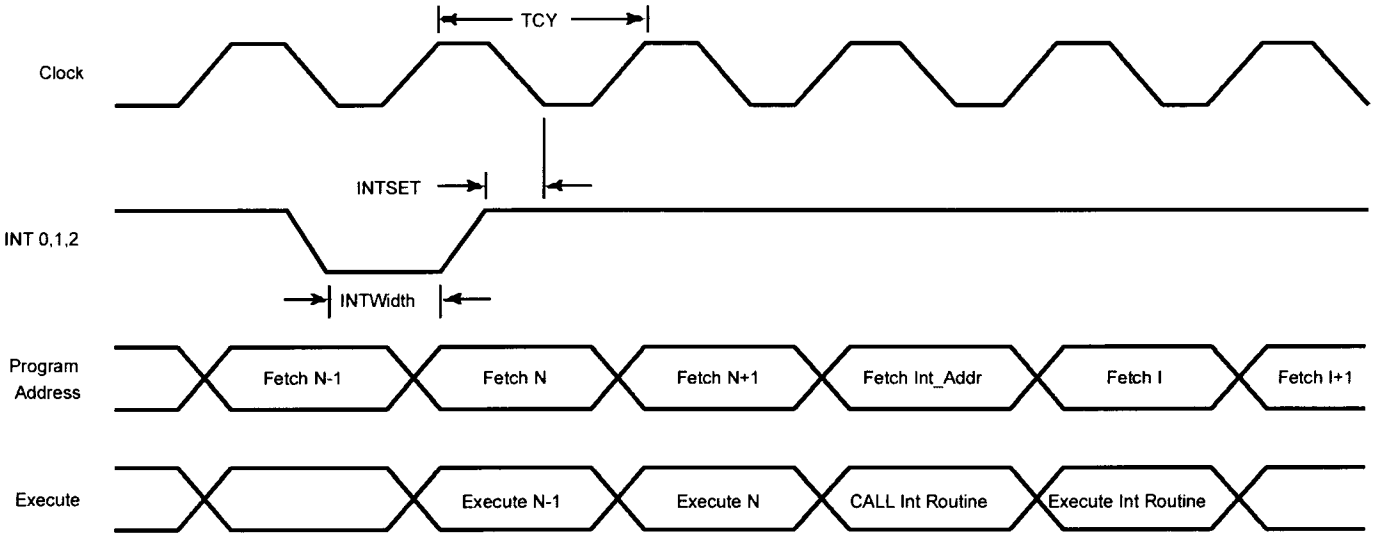


Figure 11. Interrupt Timing

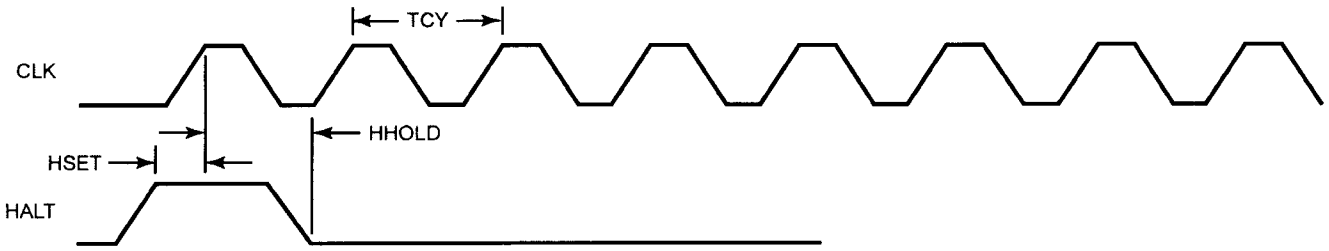


Figure 12. HALT Timing

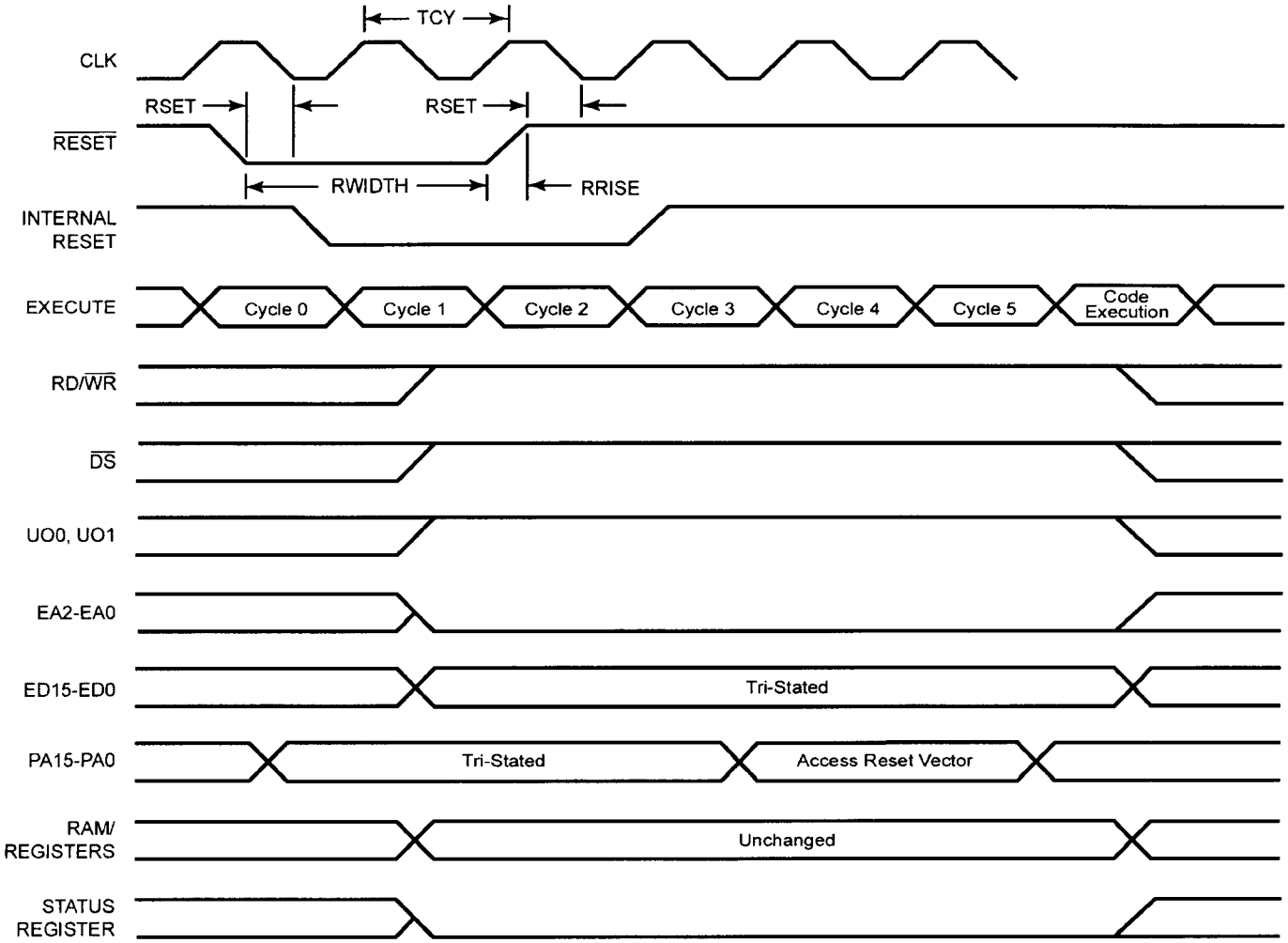


Figure 13. Synchronous Reset Timing

13-BIT GENERAL PURPOSE TIMER

The General-Purpose Timer can be enabled or disabled. At power-on or $\overline{\text{RESET}}$, the counter is enabled. When the Timer is disabled, it can only be re-enabled by another $\overline{\text{RESET}}$. The Timer operates in a continuous or one-shot mode, and can be stopped. The Timer utilizes a 13-bit down-counter.

Continuous Mode With a load instruction, the user sets the Timer to run the mode, selects the clock source, and loads a non-zero count value:

1. When the down-counter reaches zero, an interrupt is generated on INT2,
2. The non-zero count value is automatically reloaded into the down-counter,
3. The process continues at step #1.

One-Shot Mode With a load instruction, the user sets the Timer to run the mode, selects the clock source, and loads a non-zero count value:

4. When the down-counter reaches zero, an interrupt is generated on INT2,
5. The user interrupt service routine must load a zero value into the Count Operation bit (D14 of EXT4),
6. The process stops.

Timing Intervals If the Timer clock source is CLK/2:

Time Interval = (count value) x (2/CLK)

Timer Frequency = (CLK/2) / (count value)

where CLK denotes the system clock frequency.

Extended Timing Intervals The Timer interval can be extended beyond 13-bits by using the Timer in conjunction with the CODEC Interface Counter/Timer. The count is thus extended to a maximum of 25 bits:

- 12-bits from the CODEC counter/timer
- 13-bits from the Timer

If the Timer clock source is the CODEC counter output:

Time Interval =(Timer count value) x (CODEC counter/timer period)

Timer Freq. = (CODEC counter/timer freq.) ÷ (Timer count value)

Timer Interrupt Behavior The following clarifies the behavior of the Timer interrupt:

- While the Timer is enabled, it utilizes theINT2 service routine address.
- The Timer is enabled after $\overline{\text{RESET}}$; however, the Timer is in stop mode.
- The INT2 pin has an internal pull-down.
- When the Timer is in run mode, it generates an interrupt each time it counts down to zero.
- When the Timer is disabled, INT2 can be controlled by an external peripheral.

Note: If the Timer is to be disabled, and an external peripheral is driving INT2, it should hold INT2 High while the Timer is being disabled.

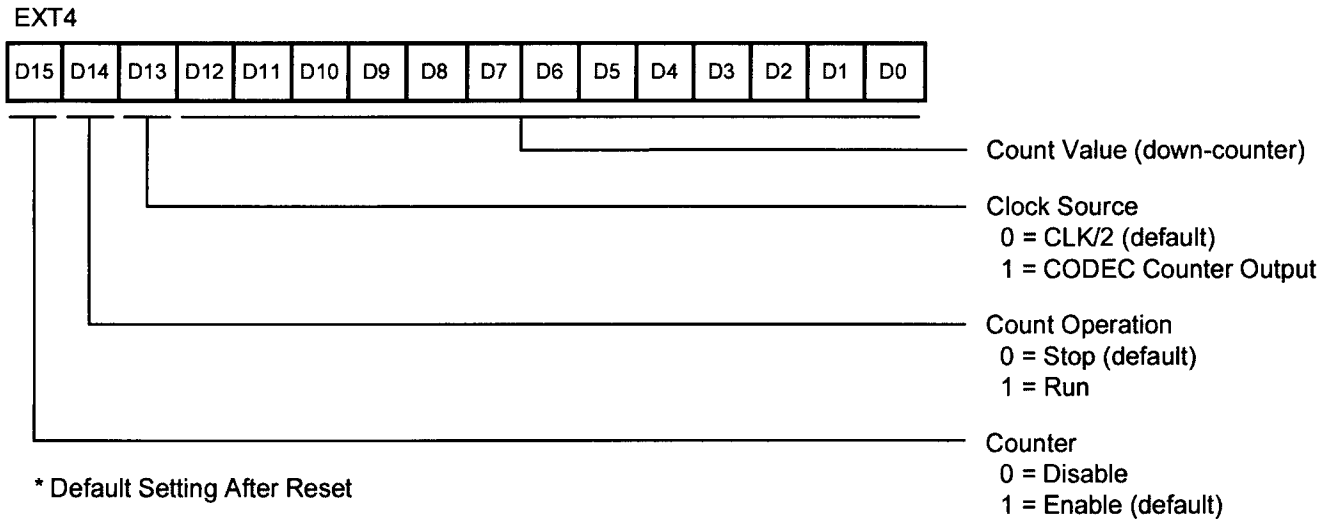


Figure 18. Timer Register EXT4

CODEC INTERFACE

Overview

The CODEC Interface not only supports a variety of external 8-bit, 16-bit linear, 64-bit sigma-delta stereo CODECs, and external A/D and D/A Converters, but the interface can also be used as a general purpose high-speed serial port. The CODEC Interface includes optional hardware μ-Law compression. The CODEC Interface is designed to support both Half-Duplex and Full-Duplex operation. The CODEC Interface is designed to operate in master mode only. The CODEC Interface generates a serial clock and two Frame Sync signals, which allows for two channels of data.

Hardware

The CODEC Interface hardware uses six 16-bit registers, μ-Law compression logic, and general-purpose control logic to control transfers to/from the appropriate registers.

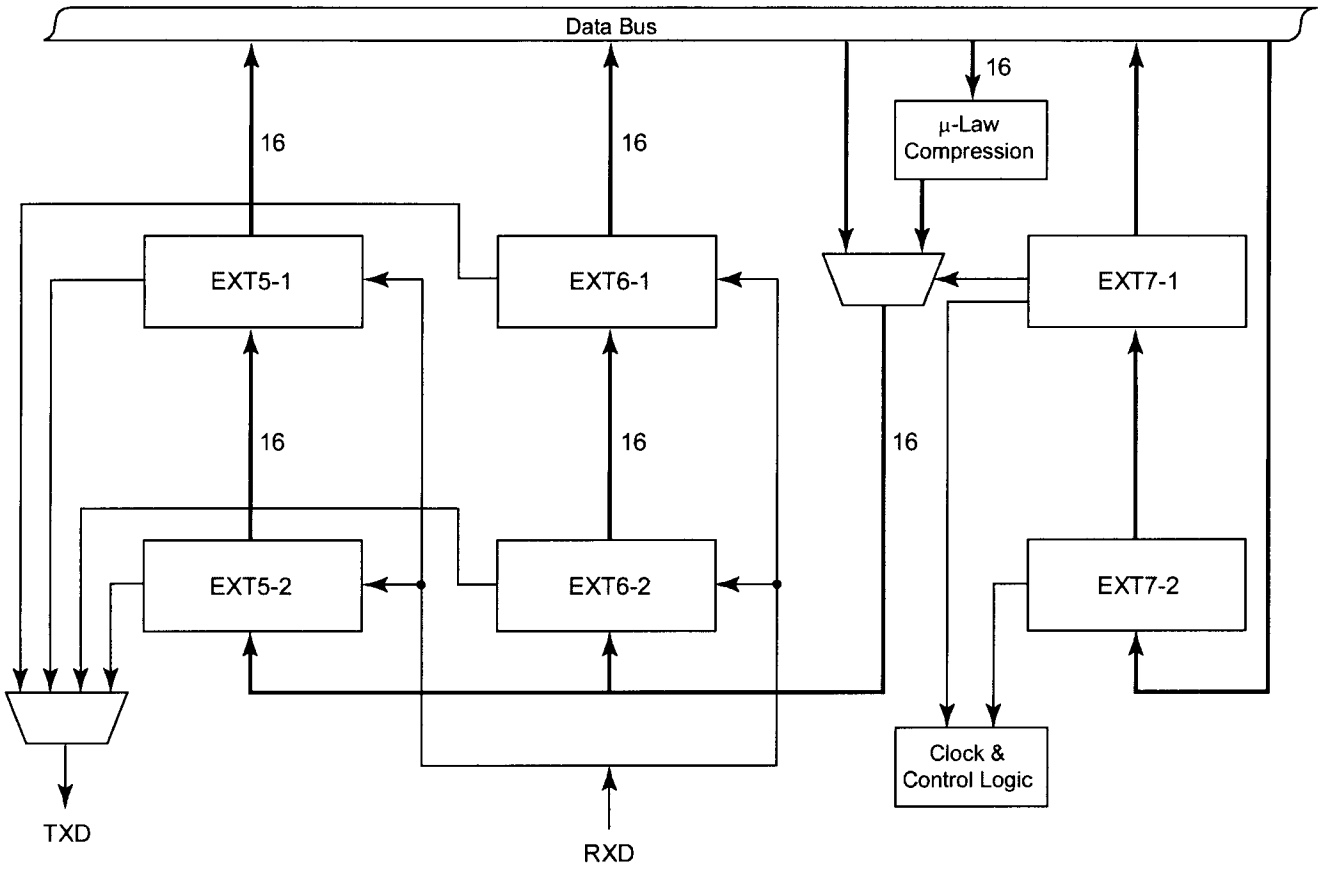


Figure 19. CODEC Interface Block Diagram

CODEC Interface Control Signals

SCLK. Serial Clock (output). This pin provides the clock signal for operating the external CODEC. A 4-bit prescaler is used to divide down the system clock (CLK) to produce the desired output frequency of SCLK. An internal divide-by-two is performed on CLK before passing it to the SCLK prescaler:

$$SCLK = (CLK/2) \div PS$$

where PS = 2's complement of the 4-bit Pre-Scaler value (PS is an up-counter).

TXD. Serial Output Data (output). This pin provides 8, 16, and 64-bit data transfers. Each bit is clocked out of the processor by the rising edge of SCLK, with the MSB transmitted first.

RXD. Serial Input Data (input). This pin provides 8, 16, and 64-bit data transfers. Each bit is clocked into the processor by the falling edge of SCLK, with the MSB received first.

FS0, FS1. Frame Sync 0 and Frame Sync 1 (output). These pins are used to mark data transfer/receive frames. The rising and falling edge of the Frame Sync signals indicate the beginning and the end of each serial data transmission.

CODEC Interface Interrupt Behavior

When the transmission of serial data is completed, the CODEC Interface generates an internal interrupt which vectors to the INT1 service routine address. This interrupt is coincident with the falling edge of FS1. The following clarifies the behavior of the CODEC Interface interrupt:

- While the CODEC Interface is enabled, it utilizes the INT1 service routine address.
- The CODEC Interface will be disabled after $\overline{\text{RESET}}$.
- The INT1 pin has an internal pull-down.
- If INT1 is tied High, the CODEC Interface generates an interrupt at the end of each frame transfer.
- If INT1 is not connected, or tied Low, the CODEC Interface not only generates an interrupt when first enabled, but generates an interrupt at the end of each frame transfer.
- When the CODEC Interface is disabled, INT1 can be controlled by an external peripheral.

Note: In single channel applications, use Channel 1 because INT1 coincides with FS1, not FS0.

Registers

The CODEC Interface registers (EXT5, EXT6 and EXT7) each act as a 2-deep FIFO. See the CODEC Interface Block Diagram for more information, Figure 19. Two operations may be required for some data transfers.

EXT5 and **EXT6.** The CODEC Interface constantly transfers and receives data during normal operation. The reading of receive data, and the writing of transmit data, are interleaved.

An example of Channel 1 operation in 8 or 16-bit mode, where one can wait for the input data, is as follows:

```
LD<dest>, EXT6          ; Read previous input data from
                          EXT6–1
LD EXT6, <xmit data>    ; Push current data from EXT6–2
                          to EXT6–1
                        ; Load EXT6–2 with data to be
                          transmitted
```

To obtain the input data as soon as it arrives, and extra instruction is required:

```
LD EXT6,<anything>      ; Push current input data from
                          EXT6–2 to EXT6–1
LD<test>, EXT6          ; Read current input data from
                          EXT6–1
LD EXT6, <xmit data>    ; Load EXT6–2 with data to be
                          transmitted
```

For 64-bit mode, one can use the following code sequence:

```
LD <Ch. 0 MSW input dest>, ; Get MSW of Ch. 0 input
EXT5
LD <Ch. 1 MSW input dest>, ; Get MSW of Ch 1 input
EXT6
LD EXT5,                ; Move LSB of Ch. 0 input
<Ch. 0 MSW output data>   and Load MSW of output
LD EXT6,                ; Move LSB of Ch. 1 input
<Ch. 1 MSW output data>   and Load MSW of output
LD<Ch. 0 LSW input test>, ; Get LSW of Ch. 0 input
EXT5
LD<Ch. 1 LSW input test>, ; Get LSW of Ch. 1 input
EXT6
LD EXT5,                ; Load LSW of Ch. 0 output
<Ch. 0 LSW output data>
LD EXT6,                ; Load LSW of Ch. 1 output
<Ch. 1 LSW output data>
```

Note: EXT# denotes EXT5 or EXT6.

In the 8 and 16-bit modes, EXT5–2 and EXT6–2 are the shift registers for Channel 0 and Channel 1, respectively. In 8-bit mode, the 8-bits reside in the least significant byte for both transmit and receive. In 64-bit mode, the output/input order is EXT 5–1 first, followed by EXT5–2, EXT6–1, and finally by EXT6–2. In all modes, the MSB is shifted out/in first.

Channel 0 uses FS0, EXT5–1, and EXT5–2. Channel 1 uses FS1, EXT6–1, and EXT6–2.

EXT7. This register contains the configuration information for the CODEC Interface and the Wait-State Generator. In normal operation, the user writes configuration data for EXT7–1 followed by configuration data for EXT7–2.

```
Write EXT7 LD EXT7, <config data1>  ; Move data to 7–2
           LD EXT7, <config data2>  ; Move data to 7–1
```

CODEC INTERFACE (Continued)

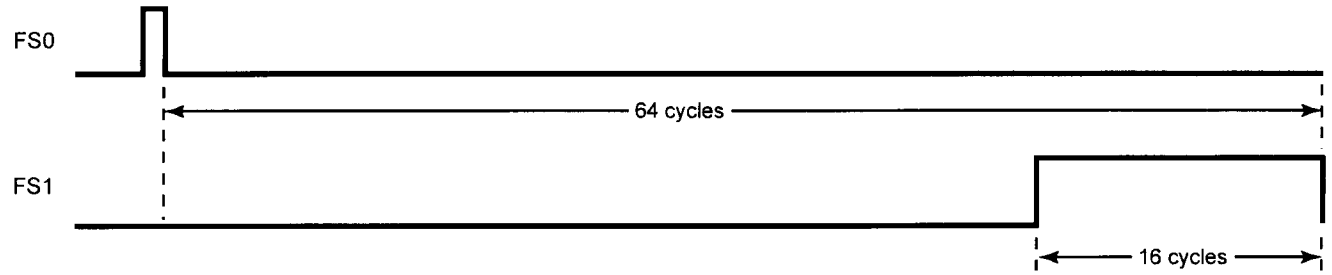


Figure 20. 64-Bit CODEC Frame Synchronization

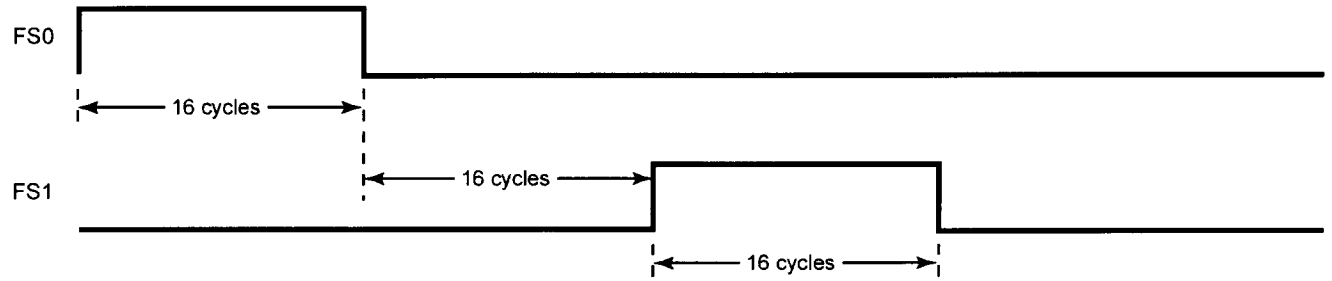


Figure 21. 16-Bit CODEC Frame Synchronization

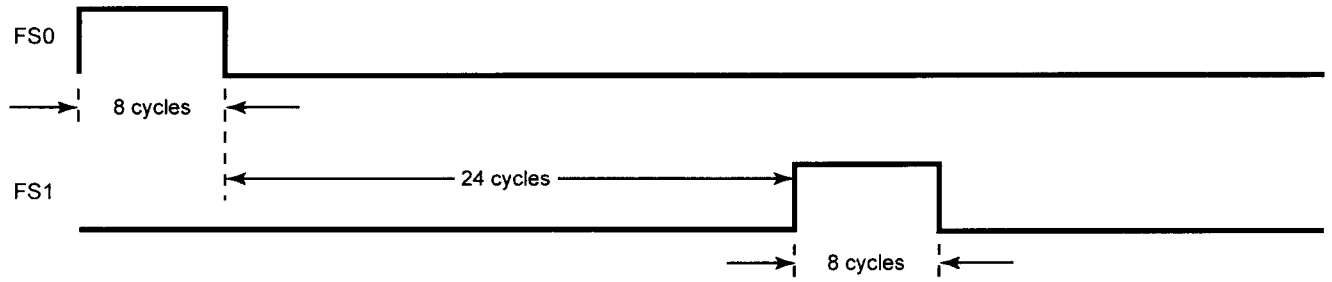


Figure 22. 8-Bit CODEC Frame Synchronization

CODEC INTERFACE (Continued)

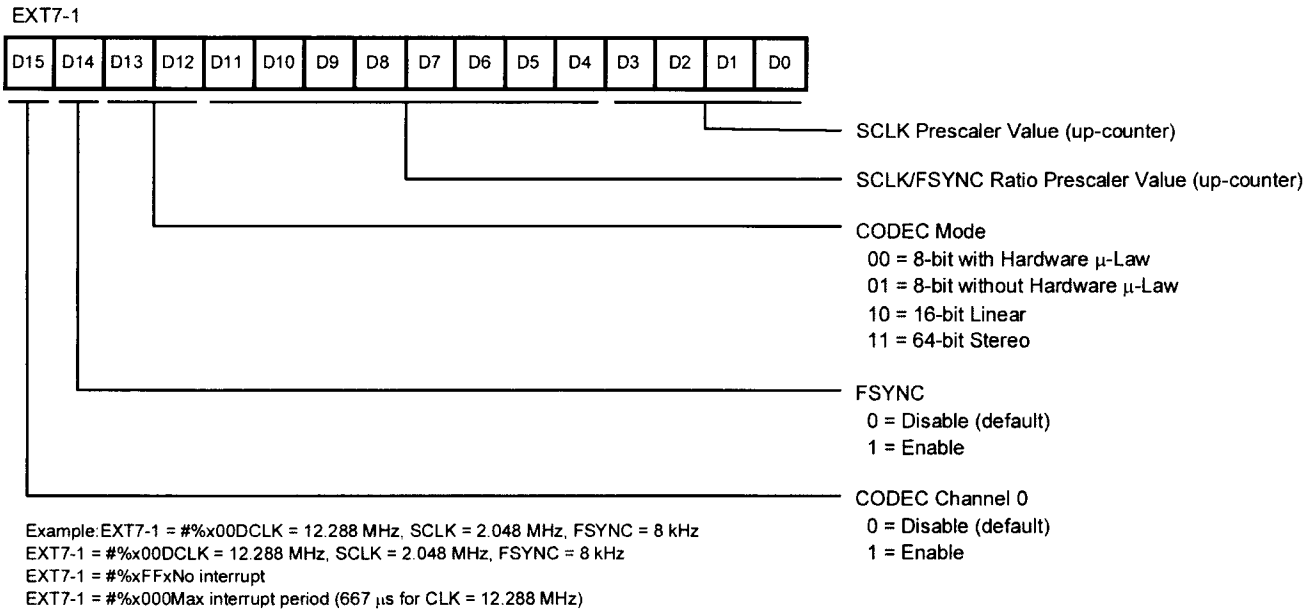


Figure 23. CODEC Interface Control Register

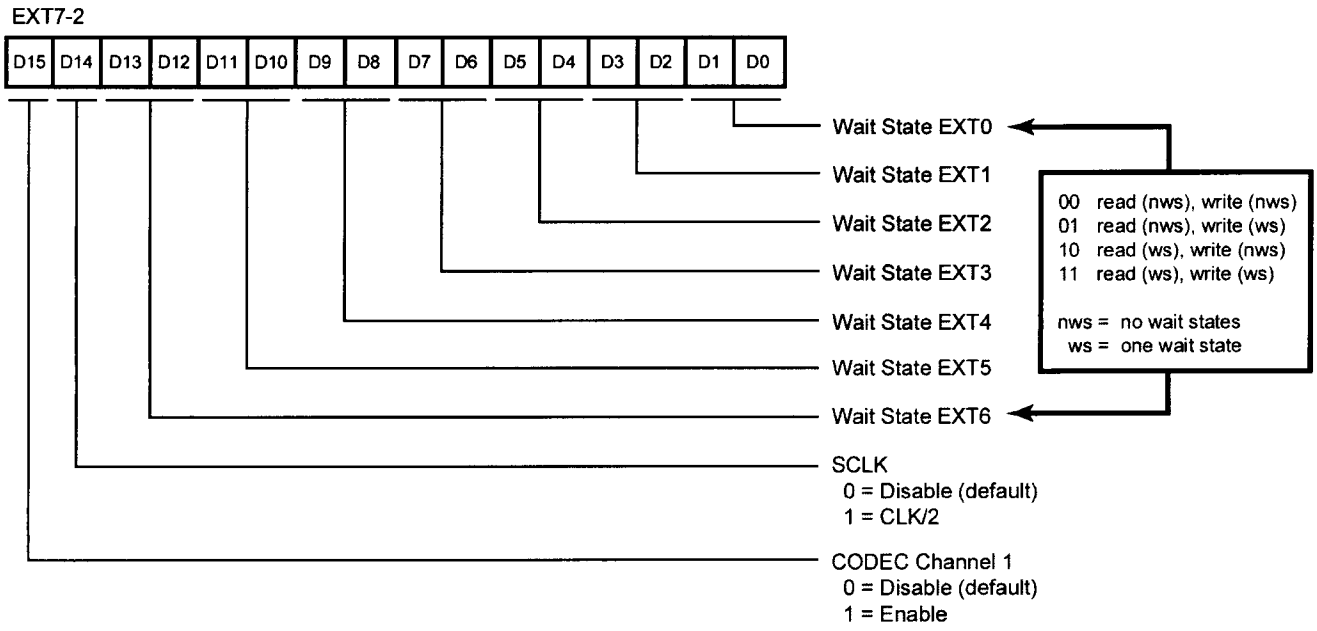


Figure 24. Wait-State Generator and CODEC Interface Control Register

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the < cc > (condition code) symbol in one of its addressing modes, the instruction will only execute if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	No Interrupts Enabled
NOV	No Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

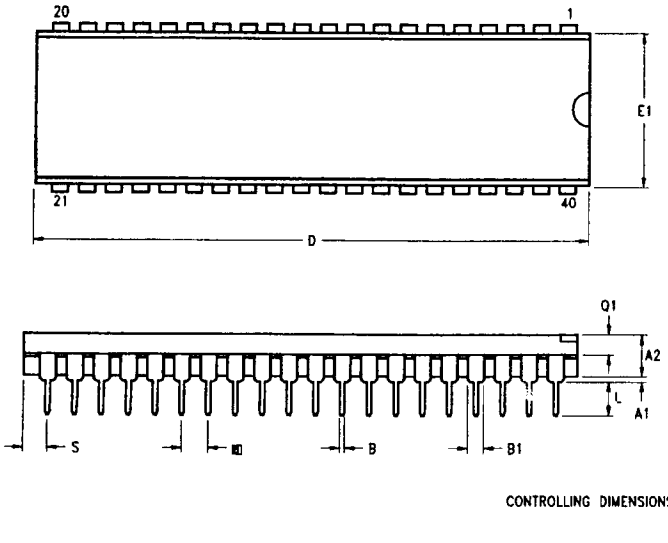
Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
Notes: 1. When <dest> is <hwregs>, <dest> cannot be P. 2. When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR. 3. When <src> is <accind> <dest> cannot be A.						
MLD	Multiply	MLD <src1>,<src2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MLD A,@P0:0+LOOP MLD A,@P1:0,OFF MLD @P1:1,@P2:0 MLD @P0:1,@P1:0,ON
Notes: 1. If src1 is <regind> it must be a bank 1 register. Src2's <regind must be a bank 0 register. 2. <hwregs> for src1 cannot be X. 3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.						
MPYA	Multiply and add	MPYA <src1>,<src2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MPYA A,@P0:0 MPYA A,@P1:0,OFF MPYA @P1:1,@P2:0 MPYA@P0:1,@P1:0,ON
Notes: 1. If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register. 2. <hwregs> for src1 cannot be X. 3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.						
MPYS	Multiply and subtract	MPYS <src1>,<src2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MPYS A,@P0:0 MPYS A,@P1:0,OFF MPYS @P1:1,@P2:0 MPYS @P0:1,@P1:0,ON
Notes: 1. If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register. 2. <hwregs> for src1 cannot be X. 3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON.						
NEG	Negate	NEG <cc>,A	<cc>, A A	1 1	1 1	NEG MI,A NEG A
NOP	No operation	NOP	None	1	1	NOP
OR	Bitwise OR	OR <dest>,<src>	A,<pregs> A,<dregs> A,<limm> A,<memind> A,<direct> A,<regind> A,<hwregs> A,<simm>	1 1 2 1 1 1 1 1	1 1 2 3 1 1 1 1	OR A,P0:1 OR A, D0:1 OR A,#%2C21 OR A,@@P2:1+ OR A, %2C OR A,@P1:0–LOOP OR A,EXT6 OR A,#%12
POP	Pop value from stack	POP <dest>	<pregs> <dregs> <regind> <hwregs>	1 1 1 1	1 1 1 1	POP P0:0 POP D0:1 POP @P0:0 POP A

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
PUSH	Push value onto stack	PUSH <src>	<pregs>	1	1	PUSH P0:0
			<dregs>	1	1	PUSH D0:1
			<regind>	1	1	PUSH @P0:0
			<hwregs>	1	1	PUSH BUS
			<limm>	2	2	PUSH #12345
			<accind>	1	3	PUSH @A
			<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine	RET	None	1	2	RET
RL	Rotate Left	RL <cc>,A	<cc>,A	1	1	RL NZ,A
			A	1	1	RL A
RR	Rotate Right	RR <cc>,A	<cc>,A	1	1	RR C,A
			A	1	1	RR A
SCF	Set C flag	SCF	None	1	1	SCF
SIEF	Set IE flag	SIEF	None	1	1	SIEF
SLL	Shift left logical	SLL	[<cc>,]A	1	1	SLL NZ,A
			A	1	1	SLL A
SOPF	Set OP flag	SOPF	None	1	1	SOPF
SRA	Shift right arithmetic	SRA<cc>,A	<cc>,A	1	1	SRA NZ,A
			A	1	1	SRA A
SUB	Subtract	SUB<dest>,<src>	A,<pregs>	1	1	SUB A,P1:1
			A,<dregs>	1	1	SUB A,D0:1
			A,<limm>	2	2	SUB A,#%2C2C
			A,<memind>	1	3	SUB A,@D0:1
			A,<direct>	1	1	SUB A,%15
			A,<regind>	1	1	SUB A,@P2:0–LOOP
			A,<hwregs>	1	1	SUB A,STACK
			A,<simm>	1	1	SUB A, #%12
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A,<pregs>	1	1	XOR A,P2:0
			A,<dregs>	1	1	XOR A,D0:1
			A,<limm>	2	2	XOR A,#13933
			A,<memind>	1	3	XOR A,@@P2:1+
			A,<direct>	1	1	XOR A,%2F
			A,<regind>	1	1	XOR A,@P2:0
			A,<hwregs>	1	1	XOR A,BUS
			A,<simm>	1	1	XOR A, #%12

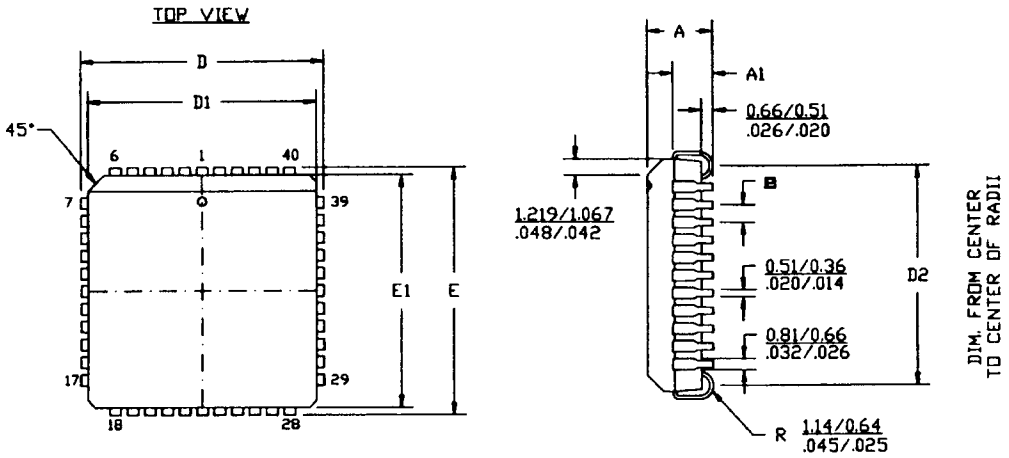
Bank Switch Operand. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether the bank switch is set ON or OFF. To more clearly represent this capacity, the keywords ON and OFF are used to state the status of the switch. These keywords are referenced in the instruction descriptions through the <bank switch> symbol. The most notable capability this item provides is that a source operand can be multiplied by itself (squared).

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 25. 40-Pin Package Diagram

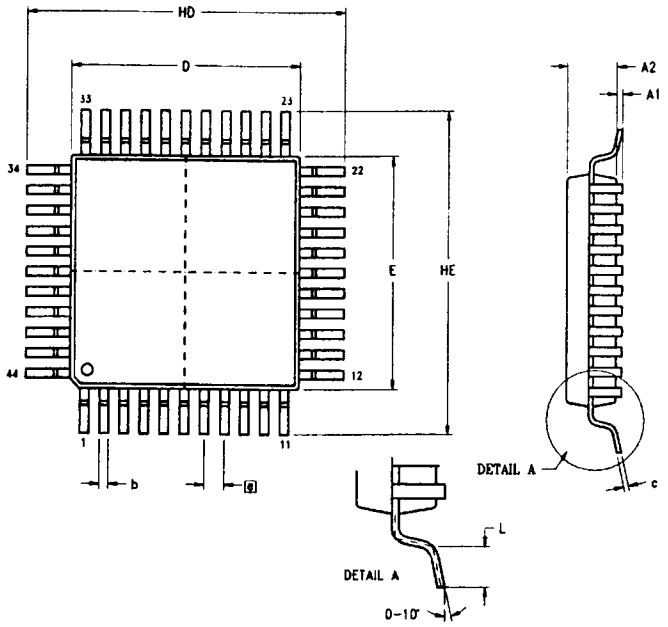


NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 26. 44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

Figure 27. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z89321
Z8932120PSC
Z8932120VSC
Z8932120VEC
Z8932120FSC
Z8932120FEC
Z89371
Z8937120PSC
Z8937120VSC
Z8937120FSC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

Package	P = Plastic DIP
	V = Plastic PLCC
	F = Plastic LOFP
Temperature	S = 0°C to +70°C
	E = –40°C to 85°C
Speed	20 = 20 MHz
Environmental	C = Plastic Standard

Example:

Z 89321 20 V S C is a Z89321, 20 MHz, PLCC, 0° to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- V — Package
- 20 — Speed
- 89321 — Product Number
- Z — ZiLOG Prefix

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The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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