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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Fixed Point
Interface	External Peripheral Interface
Clock Rate	20MHz
Non-Volatile Memory	OTP (8kB)
On-Chip RAM	1kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8937120vsg

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline are active Low. For example in RD/ $\overline{\text{WR}}$, RD is active High and $\overline{\text{WR}}$ is active Low.

The power connections follow the convention described below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

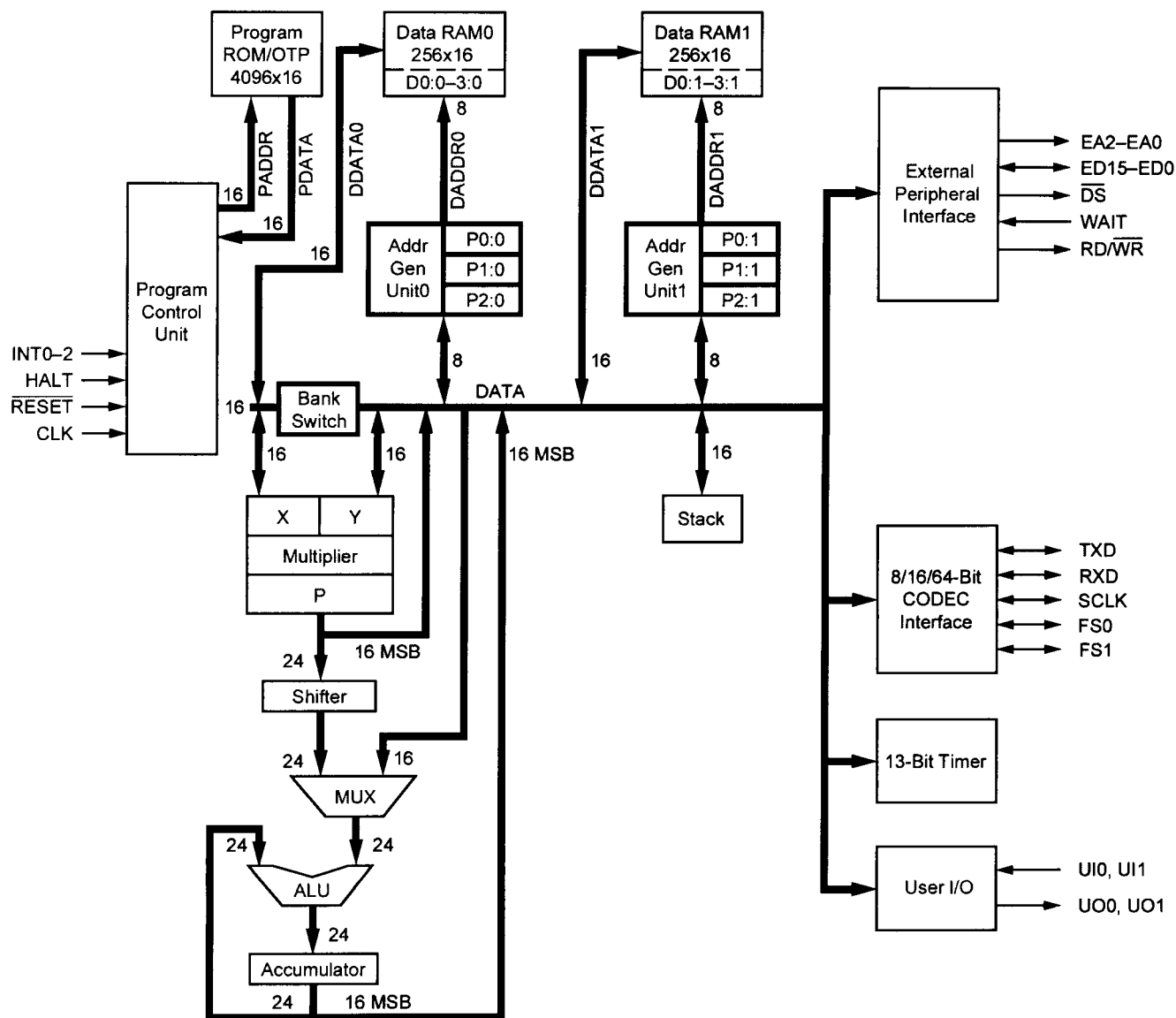


Figure 1. Z893x1 Functional Block Diagram

PIN FUNCTIONS

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are “external”

to the DSP core, and are used to access internal and external peripherals.

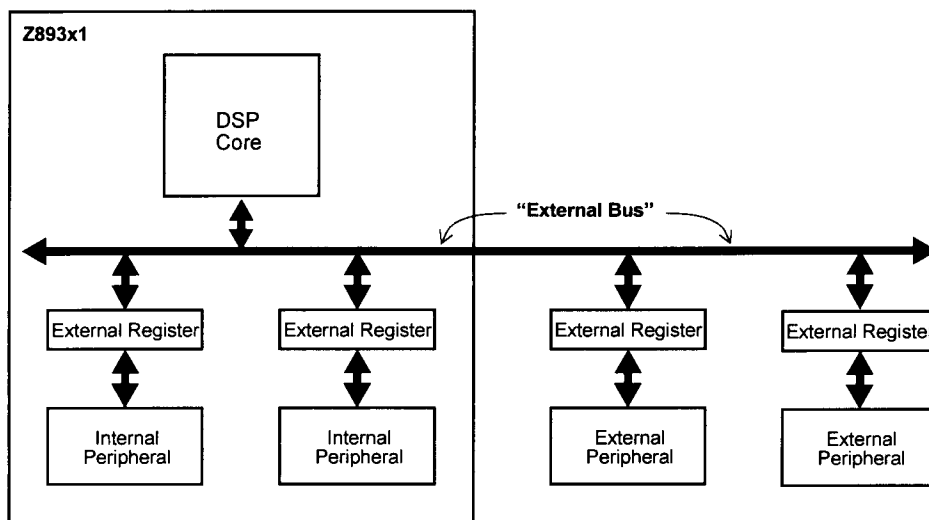


Figure 2. “External” Bus

EA2–EA0. External Address Bus (output). These pins control the user-defined register address output (latched). This bus is driven during both internal and external accesses. One of seven user-defined external registers is selected by the processor for reads or writes. External registers EXT0–EXT3 are always available to the user. External registers EXT4–EXT6 are used internally by the processor, or optionally by the user, if the pertinent internal peripherals are disabled. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers. The pins are normally tri-stated, except when these registers are specified as destination registers in a write instruction to an external peripheral. This bus uses the control signals RD/WR, DS, WAIT and the address pins EA2–EA0.

Note: The ED Bus was known as the EXT Bus in earlier versions of this document, and may be referred to as the EXT Bus, pins EXT15–EXT0, in other older related documents.

DS. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. DS is active for transfers to/from external peripherals only.

RD/WR. Read/Write Select (output). This pin controls the data direction signal for the ED Bus. Data is available from the processor on ED15–ED0 when this signal and DS are both Low.

WAIT. WAIT State (input). The wait signal is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin has an internal pull-down.

HALT. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains at the same value when this pin is held High. This pin has an internal pull-down.

INT0–INT2. Interrupts (input, positive edge triggered). These pins control interrupt requests 0–2. Interrupts are generated on the rising edge of the input signal. The DSP

PIN DESCRIPTION

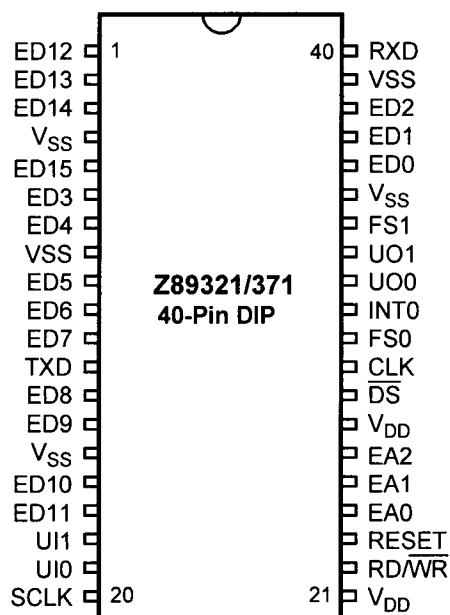


Figure 3. Z89321/371 40-Pin DIP Pin Assignments

Table 1. Z89321/371 40-Pin DIP Pin Identification

No.	Symbol	Function	Direction	No.	Symbol	Function	Direction
1	ED12	External Data Bus	In/Out	21	V _{DD}	Power Supply	Input
2	ED13	External Data Bus	In/Out	22	RD/WR	Read/Write select for ED bus	Output
3	ED14	External Data Bus	In/Out	23	RESET	Reset	Input
4	V _{SS}	Ground		24	EA0	External Address Bus	Output
5	ED15	External Data Bus	In/Out	25	EA1	External Address Bus	Output
6	ED3	External Data Bus	In/Out	26	EA2	External Address Bus	Output
7	ED4	External Data Bus	In/Out	27	V _{DD}	Power Supply	Input
8	V _{SS}	Ground		28	DS	Data Strobe for ED Bus	Output
9	ED5	External Data Bus	In/Out	29	CLK	Clock	Input
10	ED6	External Data Bus	In/Out	30	FS0	Frame Sync–CODEC Ch. 0	Output
11	ED7	External Data Bus	In/Out	31	INT0	Interrupt	Input
12	TXD	Serial Output Data	Output	32	UO0	User Output	Output
13	ED8	External Data Bus	In/Out	33	UO1	User Output	Output
14	ED9	External Data Bus	In/Out	34	FS1	Frame Sync–CODEC Ch. 1	Output
15	V _{SS}	Ground		35	V _{SS}	Ground	
16	ED10	External Data Bus	In/Out	36	ED0	External Data Bus	In/Out
17	ED11	External Data Bus	In/Out	37	ED1	External Data Bus	In/Out
18	UI1	User Input	Input	38	ED2	External Data Bus	In/Out
19	UI0	User Input	Input	39	V _{SS}	Ground	
20	SCLK	CODEC Serial Clock	Output	40	RXD	Serial Input Data	Input

Note: HALT, WAIT, INT1 and INT2 are not available in the 40-pin DIP package.

PIN DESCRIPTION (Continued)

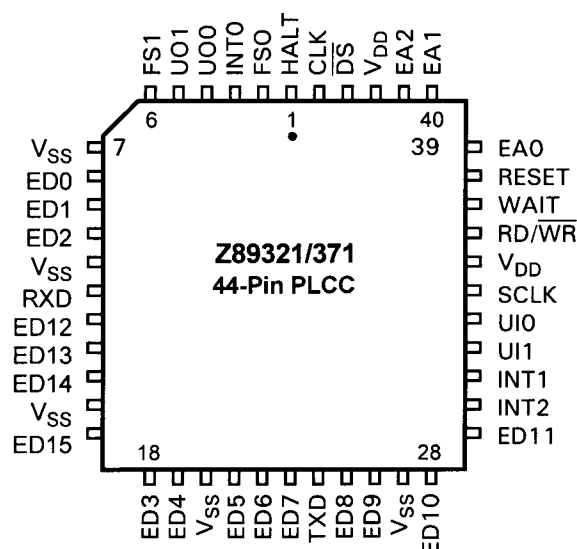


Figure 4. Z89321/371 44-Pin PLCC Pin Assignments

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
1	HALT	Stop execution	Input
2	FS0	Frame Sync-CODEC Ch. 0	Output
3	INT0	Interrupt	Input
4	UO0	User Output	Output
5	UO1	User Output	Output
6	FS1	Frame Sync-CODEC Ch. 1	Output
7	V _{SS}	Ground	
8	ED0	External Data Bus	In/Out
9	ED1	External Data Bus	In/Out
10	ED2	External Data Bus	In/Out
11	V _{SS}	Ground	
12	RXD	Serial Input Data	Input
13	ED12	External Data Bus	In/Out
14	ED13	External Data Bus	In/Out
15	ED14	External Data Bus	In/Out
16	V _{SS}	Ground	
17	ED15	External Data Bus	In/Out
18	ED3	External Data Bus	In/Out
19	ED4	External Data Bus	In/Out
20	V _{SS}	Ground	
21	ED5	External Data Bus	In/Out
22	ED6	External Data Bus	In/Out

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
23	ED7	External Data Bus	In/Out
24	TXD	Serial Output Data	Output
25	ED8	External Data Bus	In/Out
26	ED9	External Data Bus	In/Out
27	V _{SS}	Ground	
28	ED10	External Data Bus	In/Out
29	ED11	External Data Bus	In/Out
30	INT2	Interrupt	Input
31	INT1	Interrupt	Input
32	UI1	User Input	Input
33	UI0	User Input	Input
34	SCLK	CODEC Serial Clock	Output
35	V _{DD}	Power Supply	Input
36	RD/WR	Read/Write select for ED bus	Output
37	WAIT	Wait state	Input
38	RESET	Reset	Input
39	EA0	External Address bus	Output
40	EA1	External Address bus	Output
41	EA2	External Address bus	Output
42	V _{DD}	Power Supply	Input
43	DS	Data Strobe for ED Bus	Output
44	CLK	Clock	Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{DD}	Supply voltage with respect to V_{SS}	-0.3	7.0	V
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient Operating Temperature			
	"S" device	0	70	°C
	"E" device	-40	85	°C

Stresses greater than those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground.

Positive current $I_{(+)}$ flows into the referenced pin.

Negative current $I_{(-)}$ flows out of the referenced pin.

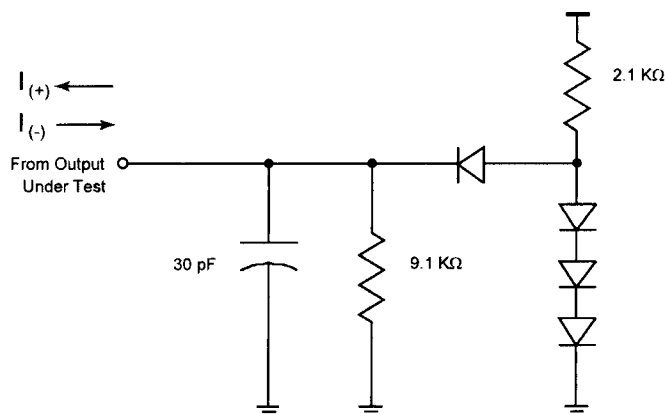


Figure 6. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Table 4. $V_{DD} = 5V \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for "S" Temperature Range
($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for "E" temperature range, unless otherwise noted)

Sym	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Supply Current	$V_{DD} = 5.5V$		70.0	TBD	mA
I_{DC}	DC Power Consumption	$V_{DD} = 5.0V$ and CLK stopped High		5.0	TBD	mA
V_{IH}	Input High Level		2.7			V
V_{IL}	Input Low Level				0.8	V
I_L	Input Leakage				10	μA
V_{OH}	Output High Voltage	$I_{OH} = -100 \mu A$	$V_{DD}-0.2$			V
		$I_{OH} = -160 \mu A$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6 \text{ mA}$			0.4	V
		$I_{OL} = 2.0 \text{ mA}$			0.5	V
I_{FL}	Output Floating Leakage Current				10	μA

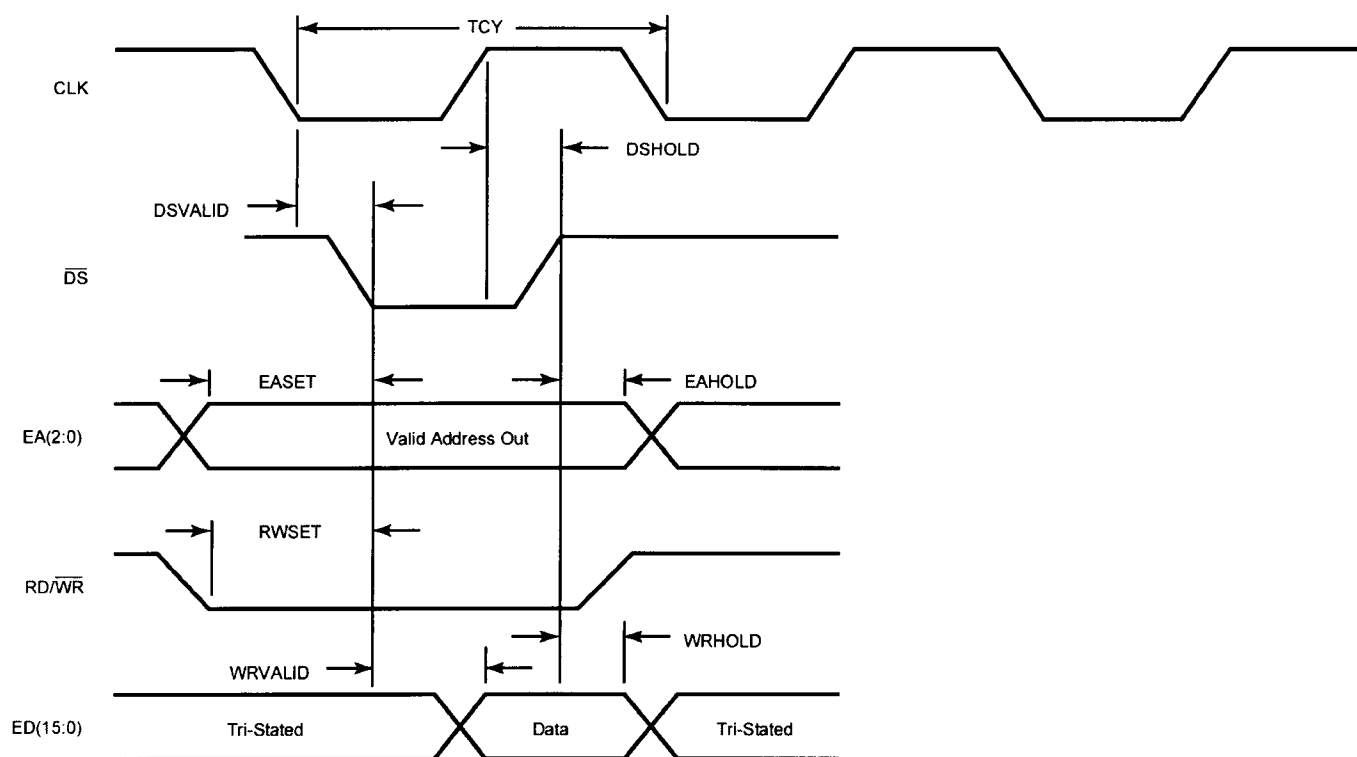


Figure 9. Write Timing

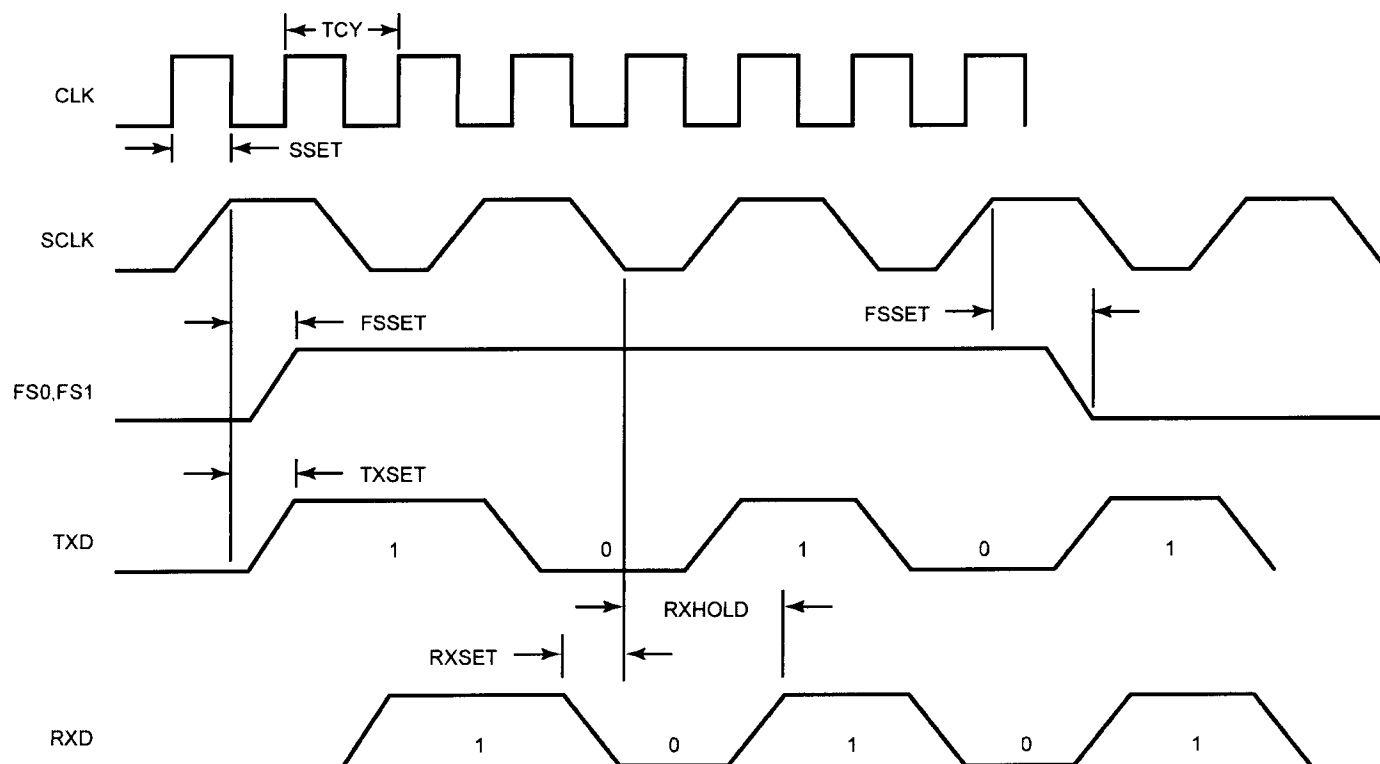


Figure 10. CODEC Interface Timing

TIMING DIAGRAMS (Continued)

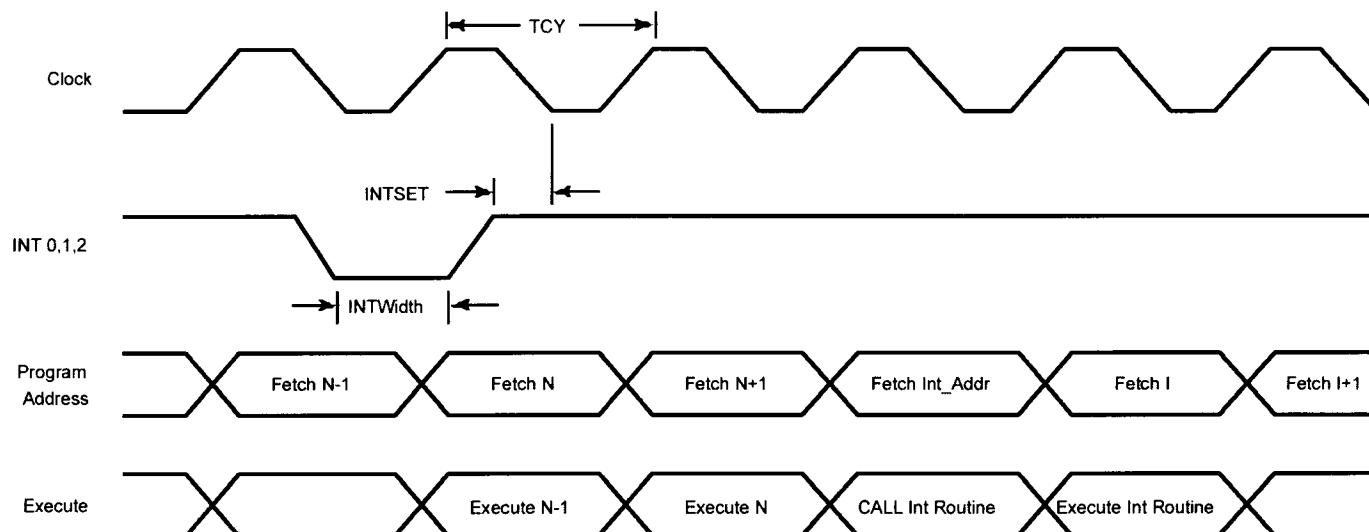


Figure 11. Interrupt Timing

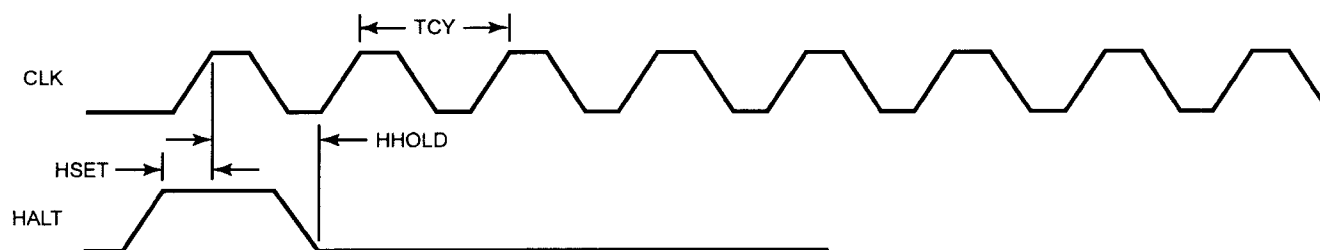


Figure 12. HALT Timing

Interrupts. The Z893x1 has three positive edge-triggered interrupt inputs. An interrupt is serviced at the end of an instruction execution. Two machine cycles are required to enter an interrupt instruction sequence. The PC is pushed onto the stack. At the end of the interrupt service routine, a RET instruction is used to pop the stack into the PC. The priority of the interrupts is INT0 = highest, INT2 = lowest. When those peripherals are enabled, INT1 is dedicated to the CODEC Interface and INT2 is dedicated to the 13-bit timer.

The Set-Interrupt-Enable-Flag (SIEF) instruction enables the interrupts. Interrupts are automatically disabled when entering an interrupt service routine. Before exiting an interrupt service routine, the SIEF instruction can be used to re-enable interrupts.

Registers. The Z893x1 has 19 internal registers and up to seven user-defined 16-bit external registers (EXT0–EXT6). The external register address space for EXT4–EXT6 is used by the Z893x1 internal peripherals. Disabling a peripheral allows access to these addresses for general-purpose use.

External Register Usage. The external registers EXT0–EXT6 are accessed using the External Address Bus EA2–EA0, the External Data Bus (ED Bus) ED15–ED0, and control signals \overline{DS} , WAIT, and RD/ \overline{WR} . These registers provide a convenient data transfer capability with external peripherals. Data transfers can be performed in a single-cycle. An internal Wait-State generator is provided to accommodate slower external peripherals. A single wait state can be implemented through control register EXT7–2. For ad-

ditional wait states, the WAIT pin can be used. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals on the ED bus.

Wait-State Generator. An internal Wait-State generator is provided to accommodate slow external peripherals. A single Wait-State can be implemented through a control register. For additional states, a dedicated pin (WAIT) can be held Low. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals (ED bus).

CODEC Interface. The CODEC Interface provides the necessary control signals for transmission of CODEC information to/from the processor. The CODEC Interface accommodates external 8-bit PCM or 16/64-bit linear CODECs. The CODEC Interface can also be used with external A/D and D/A converters. The interface can also be used as a high-speed serial port.

μ -Law Compression. The CODEC Interface provides optional hardware μ -Law compression from 13-bit format to 8-bit format. Decompression is performed in software using a 128-word lookup table.

Timers. Two programmable timers, a general purpose 13-bit Timer, and a dedicated 12-bit Counter/Timer are provided to support the CODEC Interface. The 13-bit Timer can be operated in either continuous or one-shot mode. If the CODEC Interface is not enabled, its 12-bit Counter/Timer is also available for general-purpose use.

REGISTERS

The internal registers are defined in Table 6 below:

Table 6. Register Definitions

Register	Definition
X	Multiplier X Input, 16-bits
Y	Multiplier Y Input, 16-bits
P	Multiplier Output, 24-bits
A	Accumulator, 24-bits
Pn:b	Six Data RAM Pointers, 8-bits each
PC	Program Counter, 16-bits
SR	Status Register, 16-bits
EXT4	13-bit Timer Configuration Register
EXT5-1	CODEC Interface Channel 0 Data
EXT5-2	CODEC Interface Channel 0 Data
EXT6-1	CODEC Interface Channel 1 Data
EXT6-2	CODEC Interface Channel 1 Data
EXT7-1	CODEC Interface Configuration Register
EXT7-2	Wait-State Generator and CODEC Interface Configuration Register

Note: The loading and reading of the three pairs of CODEC Interface registers (EXT5-1,2 EXT6-1,2 and EXT7-1,2) are described in the CODEC Interface section.

X and **Y** are two 16-bit input registers for the multiplier. These registers can be utilized as temporary registers when the multiplier is not being used.

P holds the result of multiplications and is read-only.

A is a 24-bit Accumulator. The output of the ALU is sent to this register. When 16-bit data is transferred into this register, it is placed into the 16 MSBs, and the least significant eight bits are set to zero. Only the upper 16 bits are transferred to the destination register when the Accumulator is selected as a source register in transfer instructions.

Pn:b are the pointer registers for accessing data RAM where $n = 0, 1, \text{ or } 2$, and $b = 0 \text{ or } 1$. These registers can perform either a direct read or write function, and each can point to locations in data RAM.

PC is the Program Counter. Any instruction which may modify this register requires two clock cycles.

SR is the status register. It contains the ALU status and processor control bits (Table 7).

Table 7. Status Register Bit Functions

SR Bit	Function	Read/Write
S15 (N)	ALU Negative	RO
S14 (OV)	ALU Overflow	RO
S13 (Z)	ALU Zero	RO
S12 (L)	Carry	RO
S11 (UI1)	User Input 1	RO
S10 (UI0)	User Input 0	RO
S9 (SH3)	MPY Output Arithmetically Shifted Right by Three Bits	R/W
S8 (OP)	Overflow Protection	R/W
S7 (IE)	Interrupt Enable	R/W
S6 (UO1)	User Output 1	R/W
S5 (UO0)	User Output 0	R/W
S4-S3	"Short Form Direct" bits	R/W
S2-S0 (RPL)	RAM Pointer Loop Size	R/W

Note: RO = read only, RW = read/write. The status register can always be read in its entirety.

S15-S12 are set/reset by the ALU after an operation.

S11-S10 are set/reset by the user inputs.

If S9 is set, and a multiply/shift option is used, the shifter shifts the result three bits right. This feature allows the data to be scaled and prevents overflows.

If S8 is set, the hardware clamps at maximum positive or negative values instead of overflowing.

S7 enables interrupts.

S6-S0 are control bits.

REGISTERS (Continued)

Table 8. RPL Description

S2	S1	S0	Loop Size
0	0	0	256
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The following are not actually registers; however, they have a read/write function that acts primarily the same way as the hardware registers do on the chip:

Register	Register Definition
BUS	DDATA Bus
Dn:b	Program Memory Pointers
EXTn	External Registers

BUS is a read-only register which, when accessed, returns the contents of the D-Bus. BUS is used for emulation only.

Dn:b refers to locations in RAM that can be used as a pointer to locations in program memory. These locations make the Z89321/371 capable for coefficient addressing. The programmer decides which location to choose from based on two bits in the status register and two bits in the operand; only the lower 16 possible locations in RAM can be specified. At any one time, there are eight usable pointers, four per bank, and the four pointers are in consecutive locations in RAM. For example, if S3/S4=1 in the status register, then D0:0/D1:0/D2:0/D3:0 refer to register locations 4/5/6/7 in RAM Bank 0.

Note: When the data pointers are being written to, a number is actually being loaded to Data RAM. In effect, these data pointers can be used as a limited method for writing to RAM.

EXT0–EXT3 are used to map external peripherals into the address space of the processor.

Note: The actual register RAM does not exist on the chip, but would exist as part of the external device (such as an A/D result latch). The External Address Bus, EA2–EA0, the External Data Bus, ED15–ED0 and the control signals \overline{DS} , WAIT and RD/ \overline{WR} , are used to access external peripherals.

EXT4 is used by the 13-bit Timer. If the Timer is disabled, then this address can be used to access an external peripheral on the External Data Bus.

EXT5 and **EXT6** are used by the CODEC Interface channels 0 and 1 respectively. If a CODEC channel is disabled, the corresponding address can be used to access an external peripheral.

EXT7 is used to program wait states for EXT0–EXT6, and is not available for accessing an external peripheral.

If both the Timer and CODEC Interface are disabled, there are 7 addresses available to access external peripherals.

If both the Timer and CODEC Interface are enabled, there are 4 addresses available to access external peripherals.

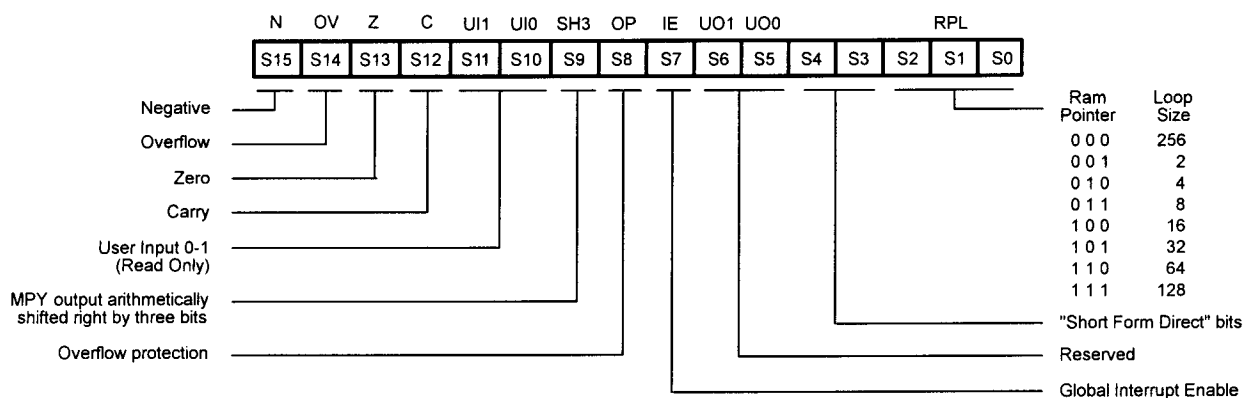


Figure 17. Status Register

13-BIT GENERAL PURPOSE TIMER

The General-Purpose Timer can be enabled or disabled. At power-on or $\overline{\text{RESET}}$, the counter is enabled. When the Timer is disabled, it can only be re-enabled by another $\overline{\text{RESET}}$. The Timer operates in a continuous or one-shot mode, and can be stopped. The Timer utilizes a 13-bit down-counter.

Continuous Mode With a load instruction, the user sets the Timer to run the mode, selects the clock source, and loads a non-zero count value:

1. When the down-counter reaches zero, an interrupt is generated on INT2,
2. The non-zero count value is automatically reloaded into the down-counter,
3. The process continues at step #1.

One-Shot Mode With a load instruction, the user sets the Timer to run the mode, selects the clock source, and loads a non-zero count value:

4. When the down-counter reaches zero, an interrupt is generated on INT2,
5. The user interrupt service routine must load a zero value into the Count Operation bit (D14 of EXT4),
6. The process stops.

Timing Intervals If the Timer clock source is CLK/2:

$$\text{Time Interval} = (\text{count value}) \times (2/\text{CLK})$$

$$\text{Timer Frequency} = (\text{CLK}/2) / (\text{count value})$$

where CLK denotes the system clock frequency.

Extended Timing Intervals The Timer interval can be extended beyond 13-bits by using the Timer in conjunction with the CODEC Interface Counter/Timer. The count is thus extended to a maximum of 25 bits:

- 12-bits from the CODEC counter/timer
- 13-bits from the Timer

If the Timer clock source is the CODEC counter output:

$$\text{Time Interval} = (\text{Timer count value}) \times (\text{CODEC counter/timer period})$$

$$\text{Timer Freq.} = (\text{CODEC counter/timer freq.}) \div (\text{Timer count value})$$

Timer Interrupt Behavior The following clarifies the behavior of the Timer interrupt:

- While the Timer is enabled, it utilizes the INT2 service routine address.
- The Timer is enabled after $\overline{\text{RESET}}$; however, the Timer is in stop mode.
- The INT2 pin has an internal pull-down.
- When the Timer is in run mode, it generates an interrupt each time it counts down to zero.
- When the Timer is disabled, INT2 can be controlled by an external peripheral.

Note: If the Timer is to be disabled, and an external peripheral is driving INT2, it should hold INT2 High while the Timer is being disabled.

EXT4

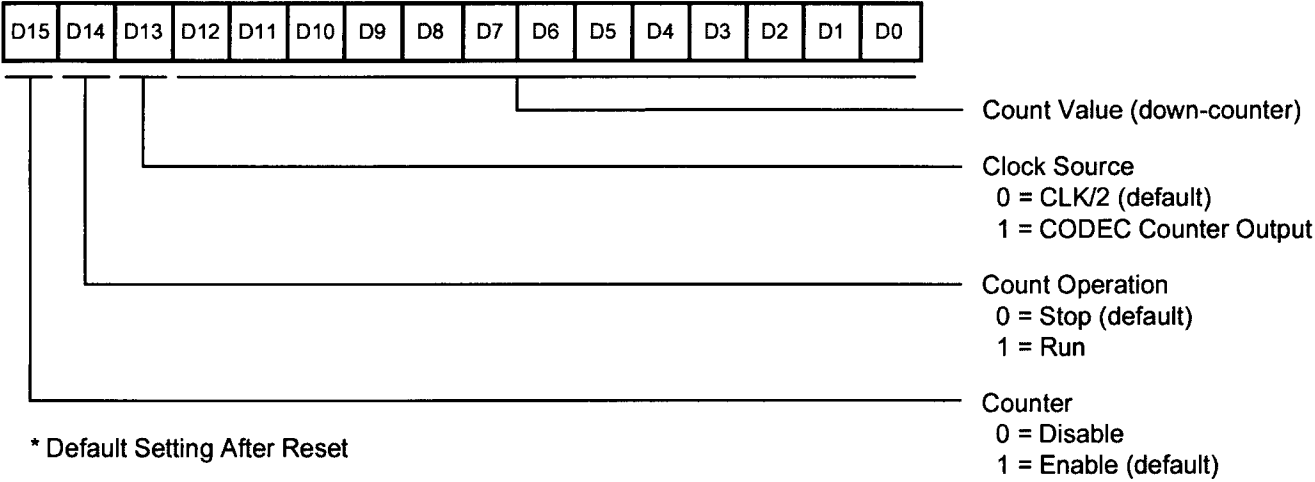


Figure 18. Timer Register EXT4

CODEC INTERFACE

Overview

The CODEC Interface not only supports a variety of external 8-bit, 16-bit linear, 64-bit sigma-delta stereo CODECs, and external A/D and D/A Converters, but the interface can also be used as a general purpose high-speed serial port. The CODEC Interface includes optional hardware μ -Law compression. The CODEC Interface is designed to support both Half-Duplex and Full-Duplex operation. The CODEC In-

terface is designed to operate in master mode only. The CODEC Interface generates a serial clock and two Frame Sync signals, which allows for two channels of data.

Hardware

The CODEC Interface hardware uses six 16-bit registers, μ -Law compression logic, and general-purpose control logic to control transfers to/from the appropriate registers.

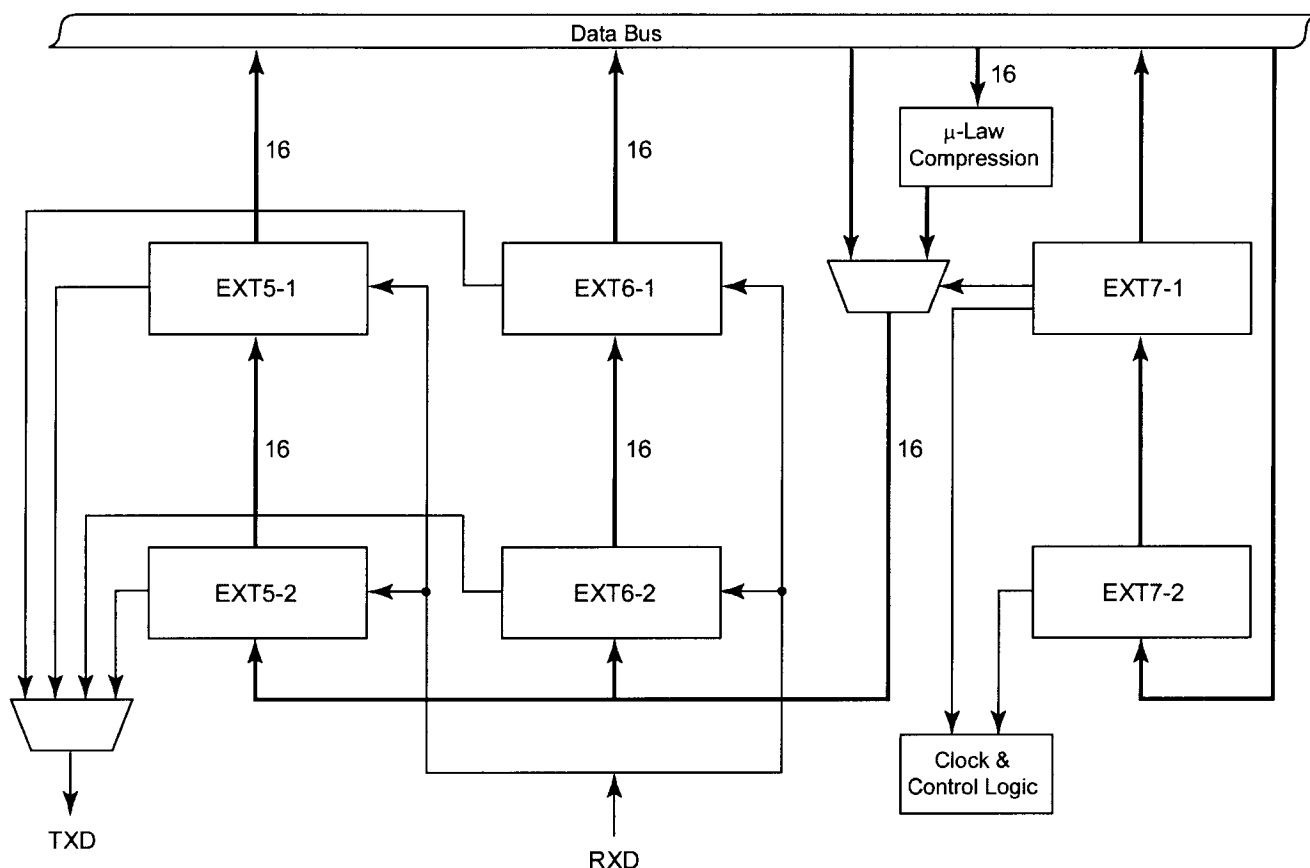


Figure 19. CODEC Interface Block Diagram

CODEC Interface Control Signals

SCLK. Serial Clock (output). This pin provides the clock signal for operating the external CODEC. A 4-bit prescaler is used to divide down the system clock (CLK) to produce the desired output frequency of SCLK. An internal divide-by-two is performed on CLK before passing it to the SCLK prescaler:

$$\text{SCLK} = (\text{CLK}/2) \div \text{PS}$$

where PS = 2's complement of the 4-bit Pre-Scaler value (PS is an up-counter).

TXD. Serial Output Data (output). This pin provides 8, 16, and 64-bit data transfers. Each bit is clocked out of the processor by the rising edge of SCLK, with the MSB transmitted first.

RXD. Serial Input Data (input). This pin provides 8, 16, and 64-bit data transfers. Each bit is clocked into the processor by the falling edge of SCLK, with the MSB received first.

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one

of its addressing modes, the instruction will only execute if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	No Interrupts Enabled
NOV	No Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
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Notes:

- When <dest> is <hwregs>, <dest> cannot be P.
- When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR.
- When <src> is <accind> <dest> cannot be A.

MLD	Multiply	MLD <src1>, <src2> [, <bank switch>]	<hwregs>, <regind>	1	1	MLD A, @P0:0+LOOP
			<hwregs>, <regind>, <	1	1	MLD A, @P1:0, OFF
			bank switch>	1	1	MLD @P1:1, @P2:0
			<regind>, <regind>	1	1	MLD @P0:1, @P1:0, ON
			<regind>, <regind>, <bank switch>			

Notes:

- If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.
- <hwregs> for src1 cannot be X.
- For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

MPYA	Multiply and add	MPYA <src1>, <src2> [, <bank switch>]	<hwregs>, <regind>	1	1	MPYA A, @P0:0
			<hwregs>, <regind>, <	1	1	MPYA A, @P1:0, OFF
			bank switch>	1	1	MPYA @P1:1, @P2:0
			<regind>, <regind>	1	1	MPYA @P0:1, @P1:0, ON
			<regind>, <regind>, <bank switch>			

Notes:

- If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.
- <hwregs> for src1 cannot be X.
- For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.

MPYS	Multiply and subtract	MPYS <src1>, <src2> [, <bank switch>]	<hwregs>, <regind>	1	1	MPYS A, @P0:0
			<hwregs>, <regind>, <	1	1	MPYS A, @P1:0, OFF
			bank switch>	1	1	MPYS @P1:1, @P2:0
			<regind>, <regind>	1	1	MPYS
			<regind>, <regind>, <bank switch>			@P0:1, @P1:0, ON

Notes:

- If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.
- <hwregs> for src1 cannot be X.
- For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON.

NEG	Negate	NEG <cc>, A	<cc>, A	1	1	NEG MI, A
			A	1	1	NEG A
NOP	No operation	NOP	None	1	1	NOP
OR	Bitwise OR	OR <dest>, <src>	A, <pregs>	1	1	OR A, P0:1
			A, <dregs>	1	1	OR A, D0:1
			A, <limm>	2	2	OR A, #2C21
			A, <memind>	1	3	OR A, @P2:1+
			A, <direct>	1	1	OR A, %2C
			A, <regind>	1	1	OR A, @P1:0-LOOP
			A, <hwregs>	1	1	OR A, EXT6
			A, <simmm>	1	1	OR A, #12
POP	Pop value from stack	POP <dest>	<pregs>	1	1	POP P0:0
			<dregs>	1	1	POP D0:1
			<regind>	1	1	POP @P0:0
			<hwregs>	1	1	POP A

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
PUSH	Push value onto stack	PUSH <src>	<pregs>	1	1	PUSH P0:0
			<dregs>	1	1	PUSH D0:1
			<regind>	1	1	PUSH @P0:0
			<hwregs>	1	1	PUSH BUS
			<limm>	2	2	PUSH #12345
			<accind>	1	3	PUSH @A
			<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine	RET	None	1	2	RET
RL	Rotate Left	RL <cc>,A	<cc>,A	1	1	RL NZ,A
			A	1	1	RL A
RR	Rotate Right	RR <cc>,A	<cc>,A	1	1	RR C,A
			A	1	1	RR A
SCF	Set C flag	SCF	None	1	1	SCF
SIEF	Set IE flag	SIEF	None	1	1	SIEF
SLL	Shift left logical	SLL	[<cc>],A	1	1	SLL NZ,A
			A	1	1	SLL A
SOPF	Set OP flag	SOPF	None	1	1	SOPF
SRA	Shift right arithmetic	SRA<cc>,A	<cc>,A	1	1	SRA NZ,A
			A	1	1	SRA A
SUB	Subtract	SUB<dest>,<src>	A,<pregs>	1	1	SUB A,P1:1
			A,<dregs>	1	1	SUB A,D0:1
			A,<limm>	2	2	SUB A,##%2C2C
			A,<memind>	1	3	SUB A,@D0:1
			A,<direct>	1	1	SUB A,%15
			A,<regind>	1	1	SUB A,@P2:0-LOOP
			A,<hwregs>	1	1	SUB A,STACK
			A,<siml>	1	1	SUB A,##%12
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A,<pregs>	1	1	XOR A,P2:0
			A,<dregs>	1	1	XOR A,D0:1
			A,<limm>	2	2	XOR A,#13933
			A,<memind>	1	3	XOR A,@@P2:1+
			A,<direct>	1	1	XOR A,%2F
			A,<regind>	1	1	XOR A,@P2:0
			A,<hwregs>	1	1	XOR A,BUS
			A,<siml>	1	1	XOR A,##%12

Bank Switch Operand. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether the bank switch is set ON or OFF. To more clearly represent this capacity, the keywords ON and OFF are used to state

the status of the switch. These keywords are referenced in the instruction descriptions through the <bank switch> symbol. The most notable capability this item provides is that a source operand can be multiplied by itself (squared).

PACKAGE INFORMATION

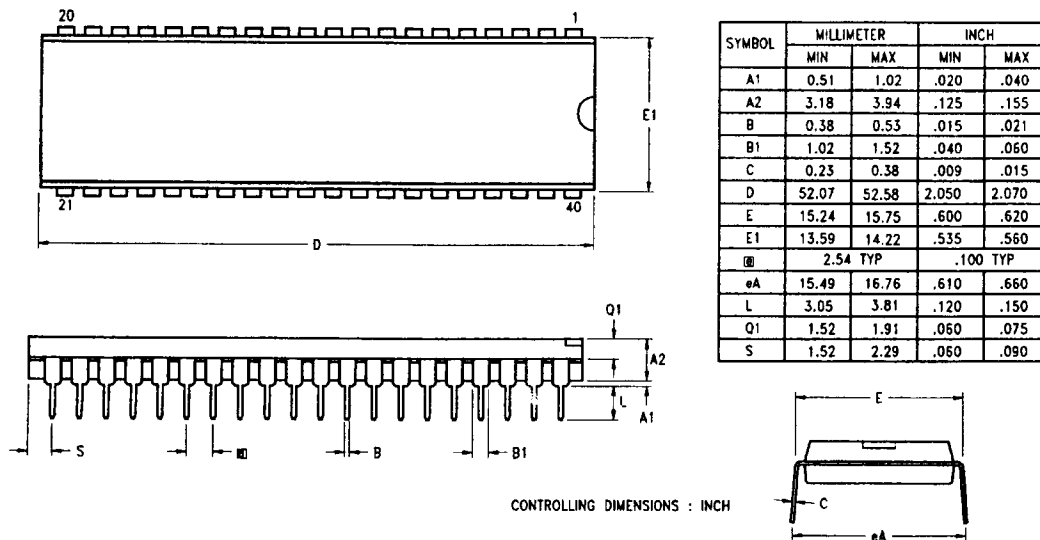


Figure 25. 40-Pin Package Diagram

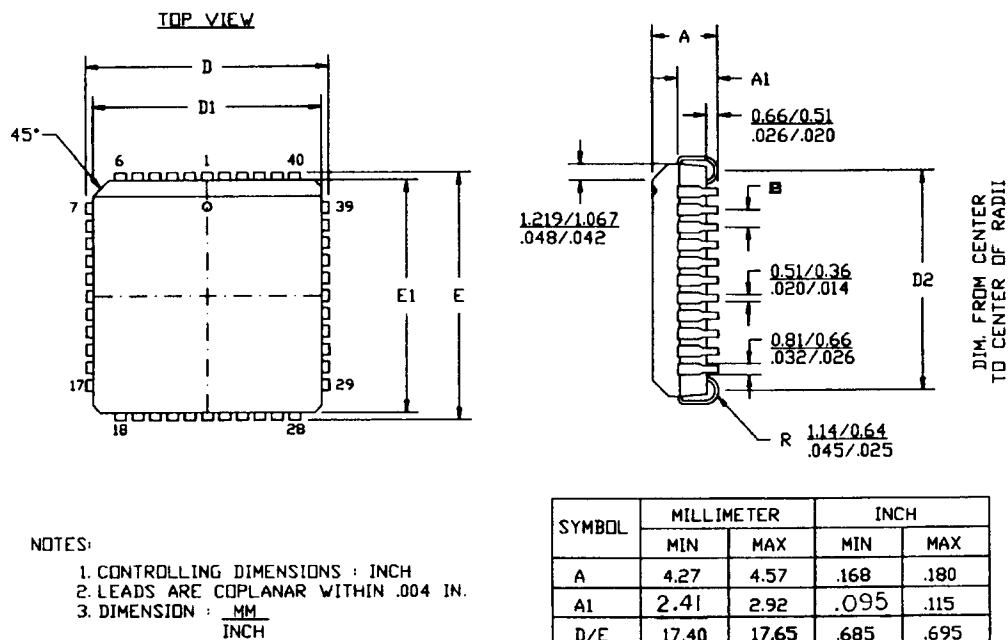


Figure 26. 44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)

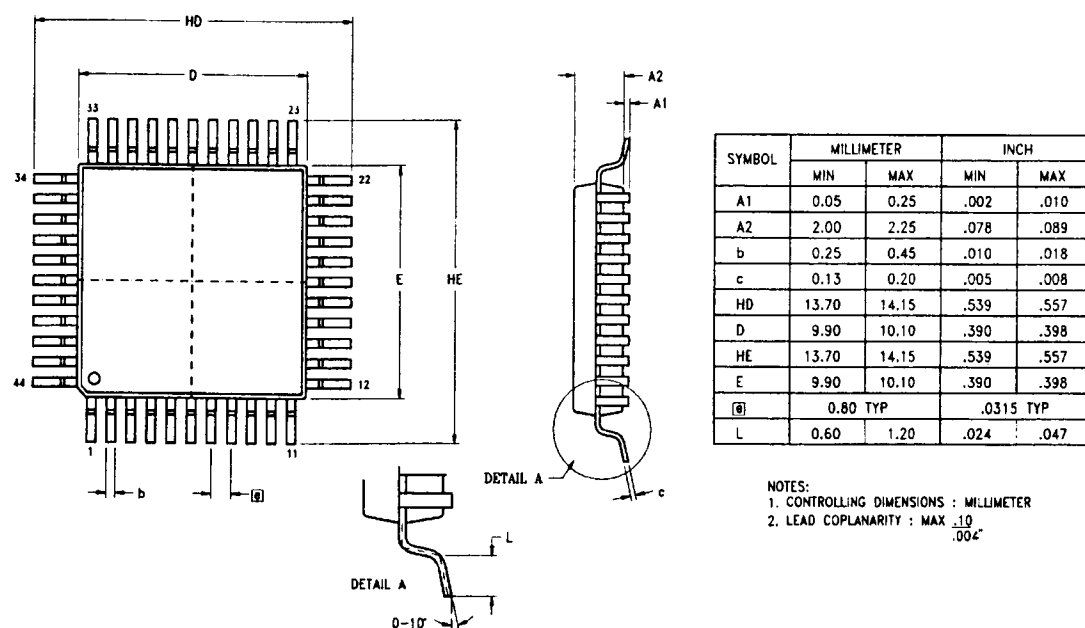


Figure 27. 44-Pin LQFP Package Diagram

ORDERING INFORMATION**Z89321**

Z8932120PSC
 Z8932120VSC
 Z8932120VEC
 Z8932120FSC
 Z8932120FEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Z89371

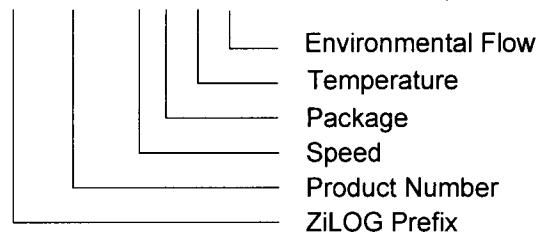
Z8937120PSC
 Z8937120VSC
 Z8937120FSC

Codes

Package	P = Plastic DIP
	V = Plastic PLCC
	F = Plastic LQFP
Temperature	S = 0°C to +70°C
	E = -40°C to 85°C
Speed	20 = 20 MHz
Environmental	C = Plastic Standard

Example:

Z 89321 20 V S C is a Z89321, 20 MHz, PLCC, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product:

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance

with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at <http://www.zilog.com/kb>.

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