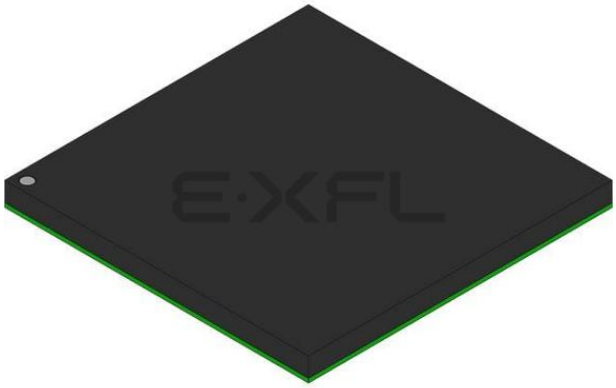

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	140MHz
Connectivity	CANbus, EBI/EMI, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 1.32V
Data Converters	A/D 6x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	225-LFBGA
Supplier Device Package	225-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5253cvm140

For additional information regarding software drivers and applications, refer to http://www.freescale.com/coldfire.

1.1 Orderable Part Numbers

Table 1 lists the orderable part numbers for the MCF5253 processor.

Table 1. Orderable Part Numbers

Orderable Part Number	Maximum Clock Frequency	Package Type	Operating Temperature Range	Part Status
MCF5253VM140	140 MHz	225 MAPBGA	-20 to +70°C	Lead free
MCF5253CVM140			-40 to +85°C	

1.2 Block Diagram

Figure 1 illustrates the functional block diagram of the MCF5253 processor.

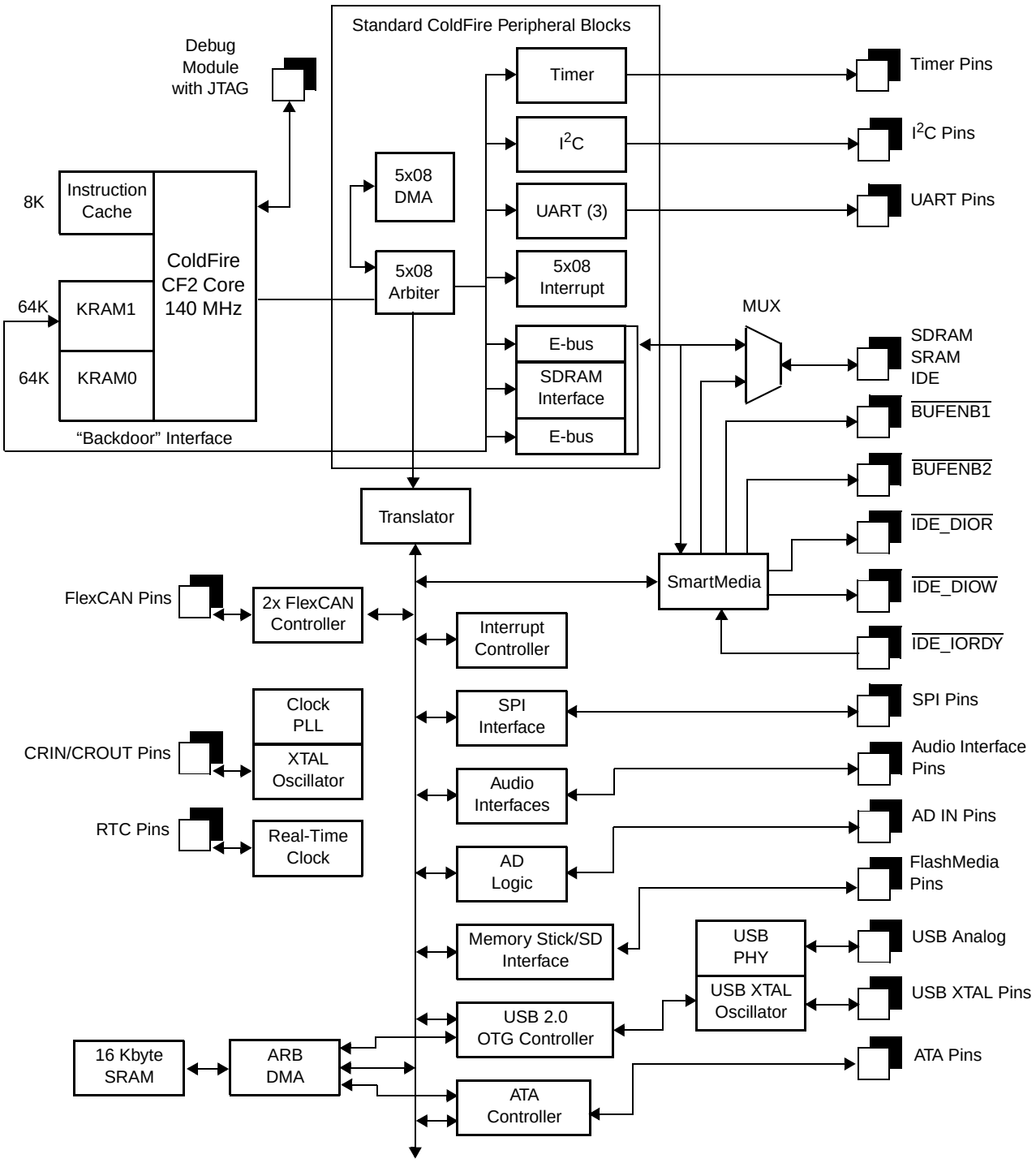


Figure 1. MCF5253 Block Diagram

Table 2. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description
UART	Universal Asynchronous Receiver /Transmitter Module	Connectivity Peripheral	Three UARTs handle asynchronous serial communication.
USBOTG	USB 2.0 High-Speed On-The-Go	Connectivity Peripheral	The USB module is used for communication to a PC or communication to slave devices; for example, to download data from a hard disc player to a flash player, and to other devices.

3 Signal Description

This chapter describes the MCF5253 input and output signals. The signal descriptions as shown in Table 3 are grouped according to relevant functionality. For additional signal information, see “Chapter 2, Signal Description” in the MCF5253 reference manual.

Table 3. MCF5253 Signal Index

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Address	A[24:1] A[23]/GPO54	24 address lines—address 23 is multiplexed with GPO54 and address 24 is multiplexed with A20 (SDRAM access only).	Out	X
Read-write control	RW	Bus write enable—indicates if read or write cycle in progress.	Out	H
Output enable	$\overline{\text{OE}}$	Output enable for asynchronous memories connected to chip selects	Out	negated
Data	D[31:16]	Data bus used to transfer word data	In/Out	Hi-Z
Synchronous row address strobe	$\overline{\text{SDRAS}}$/GPIO59	Row address strobe for external SDRAM	Out	negated
Synchronous column address strobe	$\overline{\text{SDCAS}}$/GPIO39	Column address strobe for external SDRAM	Out	negated
SDRAM write enable	$\overline{\text{SDWE}}$/GPIO38	Write enable for external SDRAM	Out	negated
SDRAM upper byte enable	$\overline{\text{SDUDQM}}$/GPO53	Upper byte enable—indicates during write cycle if high byte is written.	Out	–
SDRAM lower byte enable	$\overline{\text{SDLDQM}}$/GPO52	Lower byte enable—indicates during write cycle if low byte is written.	Out	–
SDRAM chip selects	$\overline{\text{SD\_CS0}}$/GPIO60	SDRAM chip select	In/Out	negated
SDRAM clock enable	BCLKE/GPIO63	SDRAM clock enable	Out	–
System clock	BCLK/GPIO40	SDRAM clock output	In/Out	–

Table 3. MCF5253 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
ISA bus read strobe	IDE_DIOR/GPIO31 (CS2)	1 ISA bus read strobe and 1 ISA bus write strobe—allow connection of an independent ISA bus peripheral, such as an IDE slave device.	In/Out	–
ISA bus write strobe	IDE_DIOW/GPIO32 (CS2)		In/Out	–
ISA bus wait signal	IDE_IORDY/GPIO33	ISA bus wait line available for both busses	In/Out	–
Chip Selects[2:0]	CS0/CS4 CS1/QSPICS3/GPIO28	Chip selects bits 2 through 0—enable peripherals at programmed addresses. CS0 provides boot ROM selection.	Out In/Out	negated
Buffer enable 1	BUFENB1/GPIO29	Two programmable buffer enables—allow seamless steering of external buffers to split data and address bus in sections.	In/Out	–
Buffer enable 2	BUFENB2/GPIO30		In/Out	–
Transfer acknowledge	TA/GPIO12	Transfer Acknowledge signal.	In/Out	–
Wake Up	WAKEUP/GPIO21	Wake-up signal input	In	–
Serial Clock Line	SCL0/SDATA1_BS1/GPIO41 SCL1/TXD1/GPIO10	Clock signal for Dual I^2C module operation	In/Out	–
Serial Data Line	SDA0/SDATA3/GPIO42 SDA1/RXD1/GPIO44	Serial data port for second I^2C module operation	In/Out	–
Receive Data	SDA1/RXD1/GPIO44 RXD0/GPIO46 EF/RXD2/GPIO6	Receive serial data input for UART	In	–
Transmit Data	SCL1/TXD1/GPIO10 TXD0/GPIO45 XTRIM/TXD2/GPIO0	Transmit serial data output for UART	Out	–
Request-To-Send	DDATA3/RTS0/GPIO4 DDATA1/RTS1/SDATA2_BS2/GPIO2	Signals sent from UART0/1 that it is ready to receive data	Out	–
Clear-To-Send	DDATA2/CTS0/GPIO3 DDATA0/CTS1/SDATA0_SDIO1/GPIO1	Signals sent to UART0/1 that data can be transmitted to peripheral	In	–
Timer Output	SDATAO1/TOUT0/GPIO18	Capability of output waveform or pulse generation	Out	–
IEC958 inputs	EBUIN1/GPIO36 EBUIN2/SCLKOUT/GPIO13 EBUIN3/CMD_SDIO2/GPIO14 QSPICS0/EBUIN4/GPIO15	Audio interfaces to IEC958 inputs	In	–
IEC958 outputs	EBUOUT1/GPIO37 QSPICS1/EBUOUT2/GPIO16	Audio interfaces to IEC958 outputs	Out	–
Serial data in	SDATAI1/GPIO17 SDATAI3/GPIO8	Audio interfaces to serial data inputs	In	–

Table 3. MCF5253 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Serial data out	SDATAO1/TOUT0/GPIO18 SDATAO2/GPIO34	Audio interfaces to serial data outputs	In/Out Out	–
Word clock	LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/AUDIOCLOCK/GPIO43	Audio interfaces to serial word clocks	In/Out	–
Bit clock	SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35	Audio interfaces to serial bit clocks	In/Out	–
Serial input	EF/RXD2/GPIO6	Error flag serial in	In/Out	–
Serial input	CFLG/GPIO5	C-flag serial in	In/Out	–
Subcode clock	RCK/QSPIDIN/QSPIDOUT/ GPIO26	Audio interfaces to subcode clock	In/Out	–
Subcode sync	QSPIDOUT/SFSY/GPIO27	Audio interfaces to subcode sync	In/Out	–
Subcode data	QSPICLK/SUBR/GPIO25	Audio interfaces to subcode data	In/Out	–
Clock frequency trim	XTRIM/TXD2/GPIO0	Clock trim control	Out	–
Audio clocks out	MCLK1/GPIO11 QSPICS2/MCLK2/GPIO24	DAC output clocks	Out	–
Audio clock in	LRCK3/AUDIOCLOCK/GPIO43	Optional audio clock input		–
MemoryStick/ SecureDigital interface	EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command lane—MemoryStick interface 2 data I/O	In/Out	–
	EBUIN2/SCLKOUT/GPIO13	Clock out for both MemoryStick interfaces and for Secure Digital	In/Out	–
	DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	SecureDigital serial data bit 0—MemoryStick interface 1 data I/O	In/Out	–
	SCL0/SDATA1_BS1/GPIO41	SecureDigital serial data bit 1—MemoryStick interface 1 strobe	In/Out	–
	DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	SecureDigital serial data bit 2—MemoryStick interface 2 strobe Reset output signal	In/Out	–
	SDA0/SDATA3/GPIO42	SecureDigital serial data bit 3	In/Out	–

Table 3. MCF5253 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
AT attachment interface (IDE interface)	ATA_DIOW	ATA write strobe signal	Out	–
	ATA_DIOR	ATA read strobe signal	Out	–
	ATA_IORDY	ATA I/O ready input	In	–
	ATA_DMARQ	ATA DMA request	In	–
	ATA_DMACK	ATA DMA acknowledge	Out	–
	ATA_INTRQ	ATA interrupt request	In	–
	ATA_CS0	ATA chip select 0	Out	–
	ATA_CS1	ATA chip select 1	Out	–
	ATA_A[2:0]	3-bit ATA address bus	Out	–
	ATA_D[15:0]	16-bit ATA data bus	In/Out	–
CAN interface	CAN0_TX	CAN 0 transmit	Out	–
	CAN0_RX	CAN 0 receive	In	–
	CAN1_TX	CAN 1 transmit	Out	–
	CAN1_RX	CAN 1 receive	In	–
USB PHY interface	USBVBUS	USB Vbus input	In	–
	USBID	USB ID input	In	–
	USBRES	USB current programming resistor pin	Analog	–
	USBDN	USB DM signalling line	In/Out	–
	USBDP	USB DP signalling line	In/Out	–
USB oscillator	USB_CRIN USB_CROUT	Connections for USB oscillator crystal (24 MHz)	In Out	–
RTC oscillator	RTC_CRIN RTCCROUT	Connections for real-time clock crystal (32.768 kHz)	In Out	–
AD IN	ADIN0/GPI52 ADIN1/GPI53 ADIN2/GPI54 ADIN3/GPI55 ADIN4/GPI56 ADIN5/GPI57	Analog-to-Digital Converter input signals	In	–
AD OUT	ADREF ADOUT/SCLK4/GPIO58	Analog-to-Digital Converter output signal—connects to ADREF via integrator network.	In/Out	–
QSPI clock	QSPICLK/SUBR/GPIO25	QSPI clock signal	In/Out	–
QSPI data in	RCK/QSPIDIN/QSPIDOUT/GPIO26	QSPI data input	In/Out	–

Table 3. MCF5253 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
QSPI data out	RCK/QSPIDIN/QSPIDOUT/GPIO26 QSPIDOUT/SFSY/GPIO27	QSPI data out	In/Out	–
QSPI chip selects	QSPICS0/EBUIN4/GPIO15 QSPICS1/EBUOUT2/GPIO16 QSPICS2/MCLK2/GPIO24 $\overline{\text{CS1}}$/QSPICS3/GPIO28	QSPI chip selects	In/Out	–
System oscillator in	CRIN	System input	In	–
System oscillator out	CROUT	System output	Out	–
Reset In	$\overline{\text{RSTI}}$	Processor reset input	In	–
Freescale Test Mode	TEST[2:0]	TEST pins.	In	–
Linear regulator output	LINOUT	Output of 1.2 V to supply core	Out	–
Linear regulator input	LININ	Input, typically I/O supply (3.3V)	In	–
Linear regulator ground	LINGND			–
High Impedance	$\overline{\text{HI\_Z}}$	Assertion tri-states output signal pins	In	
Debug Data	DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1 DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2 DDATA2/$\overline{\text{CTS0}}$/GPIO3 DDATA3/$\overline{\text{RTS0}}$/GPIO4	Display of captured processor data and break-point statuses	In/Out	Hi-Z
Processor Status	PST0/GPIO50 PST1/GPIO49 PST2/INTMON2/GPIO48 PST3/INTMON1/GPIO47	Indication of internal processor status.	In/Out	Hi-Z
Processor clock	PSTCLK/GPIO51	Processor clock output	Out	–
Test Clock	TCK	Clock signal for IEEE 1149.1A JTAG	In	–
Test Reset/ Development Serial Clock	DSCLK/$\overline{\text{TRST}}$	Multiplexed signal that is asynchronous reset for JTAG controller. Also, clock input for debug module.	In	–
Test Mode Select/Break Point	TMS/$\overline{\text{BKPT}}$	Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode	In	–
Test Data Input/ Development Serial Input	TDI/DSI	Multiplexed serial input for the JTAG or background debug module.	In	–
Test Data Output/Development Serial Output	TDO/DSO	Multiplexed serial output for the JTAG or background debug module	Out	–

Table 6. Recommended Operating Supply Voltages (continued)

Pin Name	Min	Typ	Max	Unit
USBGND	–	GND	–	V
RTCVDDA	3.0	–	4.2	V
RTCVSSA	–	GND	–	V
PLLCOREVDD	1.08	1.2	1.32	V
PLLCOREGND	–	GND	–	V
LININ	3.0	3.3	3.6	V
GND	–	GND	–	V

Table 7 provides the operating parameters for the linear regulator.

Table 7. Linear Regulator Operating Parameters

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage (LININ)	Vin	3.0	3.3	3.6	V
Output Voltage (LINOUT)	Vout	1.08	1.2	1.32	V
Output Current	Iout	–	100	150	mA
Power Dissipation	Pd	–	–	500	mW
Load Regulation 10% Iout ≥ 90% Iout	–	–	50	60	mV
Power Supply Rejection	PSRR	–	40	–	dB

NOTE

A pmos regulator is used as a current source in this linear regulator, so a 10 µF capacitor (ESR 0... 5 Ohm) is needed on the output pin (LINOUT) to integrate the current. Typically, this requires the use of a tantalum type capacitor.

Table 8 provides the measured parameters related to temperature for the linear regulator.

Table 8. Linear Regulator—Measured Parameters Related to Temperature

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage (LININ)	Vin	2.97	3.3	3.63	V
Output Voltage (LINOUT) 100 mA load	Vout	125 ^{o}C: 1.16:	25 ^{o}C: 1.19	-40 ^{o}C: 1.22	V
Current Consumption	Icc	-40 ^{o}C: 44	25 ^{o}C: 56	125 ^{o}C: 68	mA
Power Dissipation	Pd	-40 ^{o}C: 131	25 ^{o}C: 185	125 ^{o}C: 247	mW
Load Regulation 10% Iout ≥ 90% Iout	–	-40 ^{o}C: 46	25 ^{o}C: 57	125 ^{o}C: 70	mV

Table 10. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc) (continued)

Characteristic	Symbol	Min	Max	Units
Input Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{in}	–	±1	µA
Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{TSI}	–	±1	µA
Output High Voltage I_{OH} = 11.9 mA[1], 6.3 mA[2],3.1 mA[3]	V_{OH}	2.4	–	V
Output Low Voltage I_{OL} = 7.1m A[1], 3.5 mA[2], 1.8 mA[3]	V_{OL}	–	0.4	V
Schmitt Trigger Low to High Threshold Point[4]	V_{T+}	1.67	1.79	V
Schmitt Trigger High to Low Threshold Point[4]	V_{T-}	1.01	1.15	V
Load Capacitance: D[31:16], SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[3:1], SDATAO[2:1], CFLG, EF, IDE_DIOR, IDE_DIOW, IDE_IORDY, MCLK1, MCLK2	C_L	–	50	pF
Load Capacitance: A[24:9], ATA_CS0, ATA_CS1, ATA_A[2:0], ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_D[15:0], SDATAI[3,1]	C_L	15	40	pF
Load Capacitance: A[8:1], ADOUT, ATA_RST BCLK, BCLKE, SDCAS, SDRAS, SDLDQM, SDCS0, SDUDQM, SDWE, BUFENB[2:1], CAN0_TX, CAN1_TX, EBUIN1, RXD[2:0]	C_L	–	30	pF
Load Capacitance: SDA0, SDA1, SCL0, SCL1, CMD_SDIO2, SDATA2_BS2, SDATA1_BS1, SDATA0_SDIO1, CS0/CS4, CS1, OE, RW, TA, TXD[2:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT0, QSPID_OUT, QSPICS[3:0], QSPICLK, GPIO[6:5]	C_L	–	20	pF
Load Capacitance: DDATA[3:0], PST[3:0], PSTCLK	C_L	–	15	pF
Capacitance[5], V_{in} = 0 V, f = 1 MHz	C_{IN}	–	6	pF

1 **8.0 mA:** SCL0, SDA0, SCL1, SDA1, PST[3:0], DDATA[3:0], TDSO, RW, ATA_RST, MCLK1, QSPICS2_MCLK2

2 **4.0 mA:** BUFENB1, BUFENB2, EBUOUT1, SCLKOUT, CMDSDIO, IDE_DIOR, IDE_DIOW, TOUT0, RTS[1:0], TXD[1:0], SCLK[4:1], LRCK[4:1], SDATAO1, SDATAO2, QSPICLK, QSPICS0, QSPICS1_EBUOUT2, QSPICS3, QSPIDOUT, RCK, XTRIM, A[8:1], ATA_CS0, ATA_CS1, ATA_A[2:0]

3 **2.0 mA:** TMS/BKPT, DSI/TDI, TRST/DSCLK

4 SCLK[4:1], SCL0, SCL1, SDA0, SDA1, ATA_DMARQ, ATA_INTRQ, ATA_IORDY

5 Capacitance C_{IN} is periodically sampled rather than 100% tested.

Table 12 shows the CRIN Crystal suggested parameters.

Table 12. CRIN Crystal Suggested Parameters

Parameter	Min	Typ	Max	Unit
Frequency	5	–	16.94	MHz
Frequency Tolerance	–	–	±50	ppm
Frequency Stability Over Operating Temperature Range	–	–	±50	ppm
ESR	–	40	–	Ω
Shunt Capacitance	–	7	–	pF
Load Capacitance	–	18	–	pF

4.1 SDRAM Bus Timing

The SDRAM bus is a synchronous bus. Propagation delays, set-up times and hold times with respect to the SDRAM clock BCLK are shown in Figure 4 and the parameters provided in Table 13. When BCLK clock is not active, SDRAM interface is not valid and the external bus cannot be used.

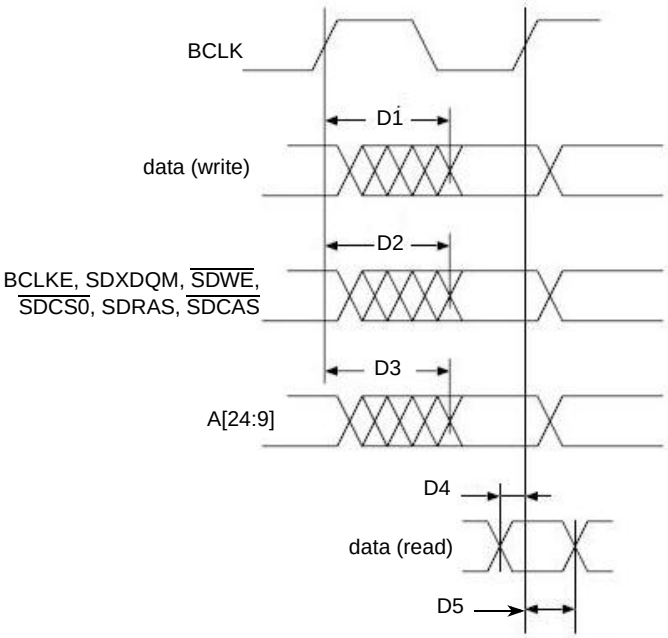


Figure 4. SDRAM Bus Timing Diagram

Table 17. JTAG Timing Parameters

ID	Characteristic	Min	Max	Units
–	TCK Frequency of Operation	0	10	MHz
J1	TCK Cycle Time	100	—	ns
J2A	TCK Clock Pulse High Width	25	—	ns
J2B	TCK Clock Pulse Low Width	25	—	ns
J3A	TCK Fall Time (V_{IH}=2.4 V to V_{IL}=0.5 V)	—	5	ns
J3B	TCK Rise Time (V_{IL}=0.5 v to V_{IH}=2.4 V)	—	5	ns
J4	TDI, TMS to TCK rising (Input Setup)	8	—	ns
J5	TCK rising to TDI, TMS Invalid (Hold)	10	—	ns
J6	Boundary Scan Data Valid to TCK (Setup)	1	—	ns
J7	TCK to Boundary Scan Data Invalid to rising edge (Hold)	10	—	ns
J8	$\overline{\text{TRST}}$ Pulse Width (asynchronous to clock edges)	12	—	ns
J9	TCK falling to TDO Valid (signal from driven or three-state)	—	15	ns
J10	TCK falling to TDO High Impedance	2	15	ns
J11	TCK falling to Boundary Scan Data Valid (signal from driven or three-state)	—	15	ns
J12	TCK falling to Boundary Scan. Data High Impedance	1	15	ns

5 Power Consumption

Table 18 shows maximum power consumption for the MCF5253 device. Typicals will be supplied at a later time.

Table 18. Maximum Power Consumption

Supply	Maximum Current
1.2 V Core	150 mA
3.3 V I/O (with core supplied separately)	150 mA[1]
3.3 V I/O (with core supplied via internal 1.2 V regulator which is fed from the 3.3 V supply)	400 mA

1 This does not include the current required for any externally connected 3.3V device (e.g., flash, SDRAM, and other I/O devices).

6 Package Information and Pinout

This section includes the pin assignment information, contact connection diagram, and the mechanical package drawing.

Table 19. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
D27	IO / 8 mA	40	–	–	–	–	HI_Z	–
D28	IO / 8 mA	40	–	–	–	–	HI_Z	–
D29	IO / 8 mA	40	–	–	–	–	HI_Z	–
D30	IO / 8 mA	40	–	–	–	–	HI_Z	–
D31	IO / 8 mA	40	–	–	–	–	HI_Z	–
Bus Control								
$\overline{OE}$	O / 4 mA	30	–	–	–	–	Negated	–
RW	O / 4 mA	30	–	–	–	–	H	–
$\overline{TA}$/GPIO12	IO / 2 mA	30	$\overline{TA}$	–	–	IO12	–	–
$\overline{BUFENB1}$/GPIO29	IO / 2 mA	30	$\overline{BUFENB1}$	–	–	IO29	–	–
$\overline{BUFENB2}$/GPIO30	IO / 2 mA	30	$\overline{BUFENB2}$	–	–	IO30	–	–
$\overline{IDE\_DIOR}$/GPIO31	IO / 2 mA	30	$\overline{IDE\_DIOR}$	–	–	IO31	–	Controlled by $\overline{CS2}$ registers
$\overline{IDE\_DIOW}$/GPIO32	IO / 2 mA	30	$\overline{IDE\_DIOW}$	–	–	IO32	–	Controlled by $\overline{CS2}$ registers
$\overline{IDE\_IORDY}$/GPIO33	IO / 2 mA	30	$\overline{IDE\_IORDY}$	–	–	IO33	–	–
Chip Selects								
$\overline{CS0}$/$\overline{CS4}$	O / 4 mA	30	$\overline{CS0}$	$\overline{CS4}$	–	–	Negated	Boot Mode Select:1-$\overline{CS0}$; 0-$\overline{CS4}$
$\overline{CS1}$/QSPICS3/ GPIO28	IO / 2 mA	30	$\overline{CS1}$	QSPICS3	25	IO28	Negated	–
SDRAM Controller								
BCLK/GPIO40	IO / 8 mA	15	BCLK	–	–	IO40	–	–
BCLKE/GPIO63	IO / 8 mA	20	BCLKE	–	–	IO63	–	–
$\overline{SDLDQM}$/GPO52	O / 8 mA	20	$\overline{SDLDQM}$	–	–	O52	–	–
$\overline{SDUDQM}$/GPO53	O / 8 mA	20	$\overline{SDUDQM}$	–	–	O53	–	–
$\overline{SDWE}$/GPIO38	IO / 8 mA	20	$\overline{SDWE}$	–	–	IO38	Negated	–
$\overline{SDCS0}$/GPIO60	IO / 8 mA	20	$\overline{SDCS0}$	–	–	IO60	Negated	–
$\overline{SDRAS}$/GPIO59	IO / 8 mA	20	$\overline{SDRAS}$	–	–	IO59	Negated	–
$\overline{SDCAS}$/GPIO39	IO / 8 mA	20	$\overline{SDCAS}$	–	–	IO39	Negated	–
ATA Interface								
ATA_A0	O / 2 mA	40	–	–	–	–	–	–
ATA_A1	O / 2 mA	40	–	–	–	–	–	–
ATA_A2	O / 2 mA	40	–	–	–	–	–	–
ATA_D0	IO / 8 mA	40	–	–	–	–	–	–
ATA_D1	IO / 8 mA	40	–	–	–	–	–	–
ATA_D2	IO / 8 mA	40	–	–	–	–	–	–
ATA_D3	IO / 8 mA	40	–	–	–	–	–	–
ATA_D4	IO / 8 mA	40	–	–	–	–	–	–
ATA_D5	IO / 8 mA	40	–	–	–	–	–	–
ATA_D6	IO / 8 mA	40	–	–	–	–	–	–
ATA_D7	IO / 8 mA	40	–	–	–	–	–	–
ATA_D8	IO / 8 mA	40	–	–	–	–	–	–
ATA_D9	IO / 8 mA	40	–	–	–	–	–	–
ATA_D10	IO / 8 mA	40	–	–	–	–	–	–
ATA_D11	IO / 8 mA	40	–	–	–	–	–	–
ATA_D12	IO / 8 mA	40	–	–	–	–	–	–
ATA_D13	IO / 8 mA	40	–	–	–	–	–	–
ATA_D14	IO / 8 mA	40	–	–	–	–	–	–

Table 19. 225 MAPBGA Pin Assignment (continued)

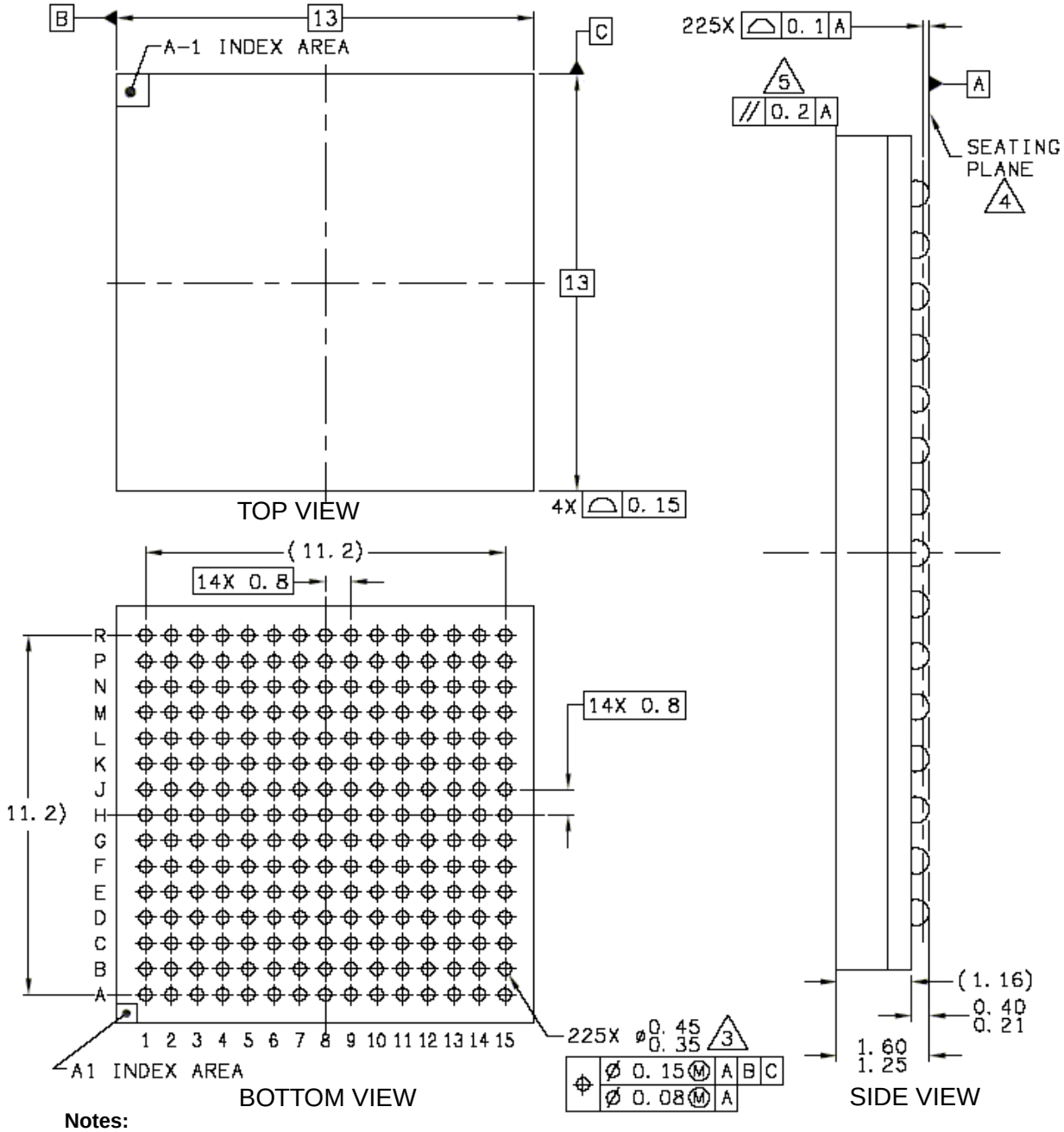
Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
ATA_D15	IO / 8 mA	40	–	–	–	–	–	–
ATA_CS0	O / 2 mA	40	–	–	–	–	–	–
ATA_CS1	O / 2 mA	40	–	–	–	–	–	–
ATA_DIOR	O / 8 mA	40	–	–	–	–	–	–
ATA_DIOW	O / 8 mA	40	–	–	–	–	–	–
ATA_IORDY	I	–	–	–	–	–	–	–
ATA_INTRQ	I	–	–	–	–	–	–	–
ATA_DMARQ	I	–	–	–	–	–	–	–
ATA_DMACK	O / 8 mA	40	–	–	–	–	–	–
$\overline{\text{ATA\_RST}}$	O / 2 mA	40	–	–	–	–	–	–
Clock Generation								
CRIN	–	–	–	–	–	–	–	Main Processor Clock Input
CROUT	–	–	–	–	–	–	–	Main Processor Clock Output
RTC_CRIN	A	–	–	–	–	–	–	Real Time Clock (32.768 kHz) Input
RTCCROUT	A	–	–	–	–	–	–	Real Time Clock (32.768 kHz) Output
USB_CRIN	A	–	–	–	–	–	–	USB Clock (24 MHz) Input
USB_CROUT	A	–	–	–	–	–	–	USB Clock (24 MHz) Output
XTRIM/TXD2/GPIO0	IO / 2 mA	30	XTRIM	TXD2	0	IO0	–	Interrupt Capable Input
JTAG/BDM/Test								
TDO/DSO	O / 4 mA	30	–	–	–	–	–	See TEST0 Description
TDI/DSI	I	–	–	–	–	–	–	See TEST0 Description
TMS/$\overline{\text{BKPT}}$	I	–	–	–	–	–	–	See TEST0 Description
TCK	I	–	–	–	–	–	–	–
$\overline{\text{TRST}}$/DSCLK	I	–	–	–	–	–	–	See TEST0 Description
$\overline{\text{HI\_Z}}$	I	–	–	–	–	–	–	For Normal Operation Tie This Pin High
PSTCLK/GPIO51	IO / 8 mA	30	PSTCLK	–	–	IO51	–	–
PST0/GPIO50	IO / 4 mA	30	PST0	–	–	IO50	HI_Z	–
PST1/GPIO49	IO / 4 mA	30	PST1	–	–	IO49	HI_Z	–
PST2/INTMON2/ GPIO48	IO / 4 mA	30	PST2	INTMON2	17	IO48	HI_Z	–
PST3/INTMON1/ GPIO47	IO / 4 mA	30	PST3	INTMON1	18	IO47	HI_Z	–
DDATA0/$\overline{\text{CTS1}}$/ SDATA0_SDIO1/GPIO1	IO / 4 mA	30	DDATA0	$\overline{\text{CTS1}}$/SDATA 0_SDIO1	14,13	IO1	HI_Z	Interrupt Capable Input
DDATA1/$\overline{\text{RTS1}}$/ SDATA2_BS2/GPIO2	IO / 4 mA	30	DDATA1	$\overline{\text{RTS1}}$/SDATA 2_BS2	24,23	IO2	HI_Z	Interrupt Capable Input
DDATA2/$\overline{\text{CTS0}}$/GPIO3	IO / 4 mA	30	DDATA2	$\overline{\text{CTS0}}$	22	IO3	HI_Z	Interrupt Capable Input
DDATA3/$\overline{\text{RTS0}}$/GPIO4	IO / 4 mA	30	DDATA3	$\overline{\text{RTS0}}$	21	IO4	HI_Z	Interrupt Capable Input
TEST0	I	–	–	–	–	–	–	BDM/JTAG Select: 1-BDM; 0-JTAG
TEST1	I	–	–	–	–	–	–	For normal operation, tie this pin low.
TEST2	I	–	–	–	–	–	–	For normal operation, tie this pin low.
Reset/Wake-up								
RSTI	I	–	–	–	–	–	–	–

Table 19. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
FlexCAN								
CAN0_TX	O / 8 mA	30	–	–	–	–	–	–
CAN0_RX	I	–	–	–	–	–	–	–
CAN1_TX	O / 8 mA	30	–	–	–	–	–	–
CAN1_RX	I	–	–	–	–	–	–	–
QSPI								
QSPICLK/SUBR/ GPIO25	IO / 2 mA	30	QSPICLK	SUBR	27	IO25	–	–
RCK/QSPIDIN/ QSPIDOUT/GPIO26	IO / 2 mA	30	RCK	QSPIDIN/ QSPIDOUT	26	IO26	–	–
QSPIDOUT/SFSY/ GPIO27	IO / 2 mA	30	QSPIDOUT	SFSY	10	IO27	–	–
I^2C								
SDA0/SDATA3/ GPIO42	IO / 4 mA	30	SDA0	SDATA3	11	IO42	–	–
SCL0/SDATA1_BS1/ GPIO41	IO / 4 mA	30	SCL0	SDATA1_BS1	12	IO41	–	–
SDA1/RXD1/GPIO44	IO / 4 mA	30	SDA1	RXD1	19	IO44	–	–
SCL1/TXD1/GPIO10	IO / 4 mA	30	SCL1	TXD1	20	IO10	–	–
UART								
TXD0/GPIO45	IO / 2 mA	30	TXD0	–	–	IO45	–	–
RXD0/GPIO46	IO / 2 mA	30	RXD0	–	–	IO46	–	–
Power/Ground Pins								
LININ	–	–	–	–	–	–	–	3.3 Volt Supply Required
LINOUT	–	–	–	–	–	–	–	1.2 Volt Output (Approx 50% Efficient)
LINGND	–	–	–	–	–	–	–	–
PLLCOREVDD (3 Balls)	–	–	–	–	–	–	–	1.2 Volt Supply Required (M4, N3, P2)
PLLCOREGND (3 Balls)	–	–	–	–	–	–	–	N4,P3,R2
USBVDD (2 Balls)	–	–	–	–	–	–	–	3.3 Volt Supply Required (L13, M13)
USBVDDP	–	–	–	–	–	–	–	1.2 Volt Supply Required
USBGND (3 Balls)	–	–	–	–	–	–	–	K11, L11, M12
OSCPADVDD	–	–	–	–	–	–	–	3.3 Volt Supply Required
OSCPADGND	–	–	–	–	–	–	–	–
RTC_VDDA	–	–	–	–	–	–	–	3.3 Volt Supply Required
RTCVSSA	–	–	–	–	–	–	–	–
ADVDD	–	–	–	–	–	–	–	3.3 Volt Supply Required
ADGND	–	–	–	–	–	–	–	–
PADVDD (10 Balls)	–	–	–	–	–	–	–	3.3 Volt Supply Required (E7, E9, F10, H8, H11, K5, L6, L8, L10, R13)

6.2 Package Drawing

Figure 6 shows the package outline diagram for the MCF5253 processor.



Notes:

1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M–1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crown of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Figure 6. MCF5253 Package Drawing

Table 20 shows the signal color and signal name legend.

Table 20. Signal Color/Name Legend

Color	Name
None	Signal name as listed
	GND
	PADVDD
	COREVDD
	USBGND

Table 21 shows the device pin list, sorted by signal identification.

Table 21. MCF5253 13 x 13 BGA (225 Signal ID by Pad Grid Location)

Signal ID	Pad Location
A1	H03
A10	F02
A11	G05
A12	F03
A13	F01
A14	E01
A15	G04
A16	E02
A17	F04
A18	E03
A19	F05
A2	H02
A20/A24	F06
A21	D03
A22	D01
A23/GPO54	D02
A3	H01
A4	H05
A5	G01
A6	G03
A7	G02
A8	H04
A9	H06
ADGND	L04
ADIN0/GPI52	K03
ADIN1/GPI53	L01
ADIN2/GPI54	L02
ADIN3/GPI55	L03
ADIN4/GPI56	M01
ADIN5/GPI57	J06
ADOUT/SCLK4/GPIO58	J05
ADREF	M02
ADVDD	K04

Table 21. MCF5253 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
D17	E04
D18	E05
D19	B01
D20	C02
D21	D04
D22	C03
D23	B02
D24	A02
D25	B03
D26	A03
D27	C04
D28	B04
D29	D05
D30	A04
D31	C05
DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	K10
DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	R11
DDATA2/$\overline{\text{CTS0}}$/GPIO3	J14
DDATA3/$\overline{\text{RTS0}}$/GPIO4	J12
EBUIN1/GPIO36	N06
EBUIN2/SCLKOUT/GPIO13	M06
EBUIN3/CMD_SDIO2/GPIO14	K07
EBUOUT1/GPIO37	P06
EF/RXD2/GPIO6	R09
GND	A01
GND	A15
GND	E08
GND	E10
GND	F07
GND	G06
GND	G07
GND	G09
GND	G11
GND	J07
GND	J09
GND	J10
GND	J11
GND	L05
GND	L07
GND	L09
GND	R01
GND	R15
$\overline{\text{HI\_Z}}$	B13
$\overline{\text{IDE\_DIOR}}$/GPIO31	M05
$\overline{\text{IDE\_DIOW}}$/GPIO32	P04
$\overline{\text{IDE\_IORDY}}$/GPIO33	R04

Table 21. MCF5253 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
LINGND	C13
LININ	A14
LINOUT	B14
LRCK1/GPIO19	P08
LRCK2/GPIO23	E14
LRCK3/AUDIOCLK/GPIO43	M10
MCLK1/GPIO11	D14
NC	R14
$\overline{OE}$	R03
OSCPADGND	P01
OSCPADVDD	N01
PADVDD	E07
PADVDD	E09
PADVDD	F10
PADVDD	H08
PADVDD	H11
PADVDD	K05
PADVDD	L06
PADVDD	L08
PADVDD	L10
PADVDD	R13
PLLAVDD	M04
PLLCOREGND	N04
PLLCOREGND	P03
PLLCOREGND	R02
PLLCOREVDD	N03
PLLCOREVDD	P02
PST0/GPIO50	G15
PST1/GPIO49	G12
PST2/INTMON2/GPIO48	H14
PST3/INTMON1/GPIO47	H13
PSTCLK/GPIO51	G14
QSPICLK/SUBR/GPIO25	P07
QSPICS0/EBUIN4/GPIO15	R07
QSPICS1/EBUOUT2/GPIO16	N08
QSPICS2/MCLK2/GPIO24	P09
QSPIDOUT/SFSY/GPIO27	M08
RCK/QSPIDIN/QSPIDOUT/GPIO26	N07
RSTI	E15
RTC_CRIN	J01
RTC_VDDA	J02
RTCCROUT	K02
RTCVSSA	K01
RW	J04
RXD0/GPIO46	H15
SCL0/SDATA1_BS1/GPIO41	P10

7 Product Documentation

This section includes the related product documentation and references to information posted on Freescale's external web page.

This document is labeled as the type: Data Sheet: Technical Data. Definitions for all Freescale document types are available at: http://www.freescale.com.

You can also obtain information on the mechanical characteristics of the MCF5253 integrated microprocessor at http://www.freescale.com/coldfire.

The following documents are required for a complete description of the device and are necessary for proper design:

MCF5253 Reference Manual (order number: MCF5253RM)

MCF5253 Product Brief (order number: MCF5253PB)

7.1 Revision History

Table 22 summarizes revisions to this document.

Table 22. MCF5253DS Revision History

Rev. No.	Substantive Change(s)
2	First public version.
3	Added industrial temperature part number, MCF5253CVM140.
4	Added Section 5, "Power Consumption"

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