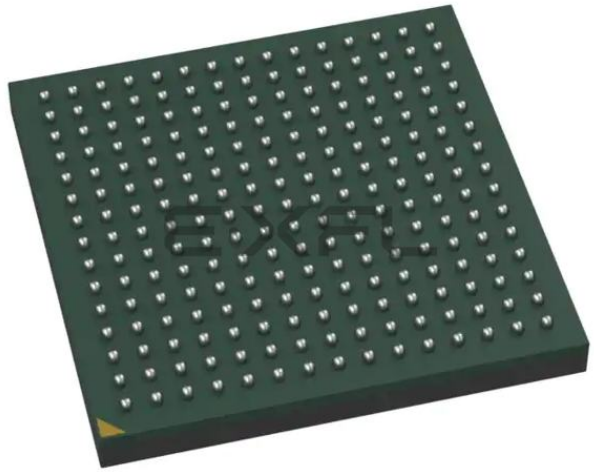

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	140MHz
Connectivity	CANbus, EBI/EMI, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, WDT
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 1.32V
Data Converters	A/D 6x12b
Oscillator Type	External
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	225-LFBGA
Supplier Device Package	225-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5253vm140j

2 Functional Description

2.1 Version 2 ColdFire Core

The Version 2 ColdFire (CF2) core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size. The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function.

2.2 Module Inventory

Table 2 shows an alphabetical listing of the modules in the processor.

Table 2. Digital and Analog Modules

Block Mnemonic	Block Name	Functional Grouping	Brief Description
ATA	Advanced Technology Attachment Controller	Connectivity Peripheral	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disc drives and ATAPI optical disc drives.
ADC	Battery Level/Keypad Analog/Digital Converter	Analog Input	The six-channel ADC is based on the Sigma-Delta concept with 12-bit resolution. Both the analog comparator and digital sections are integrated in the MCF5253.
AB	Audio Bus	Audio Interface	The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission.
AIM	Audio Interface	Audio Interface	The audio interface module provides the necessary input and output features to receive and transmit digital audio signals over serial audio interfaces (IIS/EIAJ) and over digital audio interfaces (IEC958).
BROM	Bootloader	Boot ROM	The MCF5253 incorporates a ROM Bootloader, which enables booting from UART, I2C, SPI, or IDE devices.
FlexCAN	Twin Controller Area Network 2.0B Communication Unit	Connectivity Peripheral	The FlexCan module is a full implementation of the Bosch CAN protocol specification 2.0B, which supports both standard and extended message frames.
CSM	Chip Select Module	Connectivity Peripheral	Three programmable chip-select outputs ($\overline{CS0}$/$\overline{CS4}$, $\overline{CS1}$, and $\overline{CS2}$) provide signals that enable glueless connection to external memory and peripheral circuits.
DMAC	Direct Memory Access Controller Module	Connectivity Peripheral	There are four fully programmable DMA channels for quick data transfer.
eMAC	enhanced Multiply Accumulate Module	Core	The integrated eMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture.
MBUS	Memory Bus Interface	Bus Operation	The bus interface controller transfers data between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus.
MMC/SD	Multimedia Card/Secure Digital Interface	Flash Memory Card Interface	The interface is Sony® Memory Stick®, SecureDigital, and Multi-Media card compatible. **Note:** The Sony Memory Interface does not support Sony MagicGate™.

Table 2. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description
GPIO	General Purpose I/O Interface	System integration	GPIO signals are multiplexed with various other signals.
GPT	General Timer Module	Timer peripheral	The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer.
IDE	Integrated Drive Electronics	Connectivity peripheral	The IDE hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses from propagating to the IDE bus.
INC	Instruction Cache	Core	The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock cycle.
I^2C	Inter IC Communication Module	Connectivity peripheral	The two-wire I^2C bus interfaces, compliant with the Philips I^2C bus standard, are bidirectional serial buses that exchange data between devices.
SRAM	Internal 128-KB SRAM	Internal memory	The 128-Kbyte on-chip SRAM is split over two banks, SRAM0 (64K) and SRAM1 (64K). It provides single clock-cycle access for the ColdFire core.
LIN	Internal Voltage Regulator	Linear regulator	An internal 1.2 V regulator is used to supply the CPU and PLL sections of the MCF5253, reducing the number of external components required and allowing operation from a single supply rail, typically 3.3 volts.
JTAG	Joint Test Action Group	Test and debug	To help with system diagnostics and manufacturing testing, the MCF5253 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG.
QSPI	Queued Serial Peripheral Interface	Connectivity Interface	The QSPI module provides a serial peripheral interface with queued transfer capability.
RTC	Real-Time Clock	Timer Peripheral	The RTC is a clock that keeps track of the current time even if the clock is turned off.
BDM	Background Debug Interface	Test and debug	A background-debug mode (BDM) interface provides system debug.
SDRAMC	Synchronous DRAM Memory Controller	Peripheral Interface	The SDRAM controller provides a glueless interface for one bank of SDRAM, and can address up to 32MB. The controller supports a 16-bit data bus. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMs.
SIM	System Integration Module	System Integration	The SIM provides overall control of the internal and external buses and serves as the interface between the ColdFire core and the internal peripherals or external devices. The SIM is responsible for the two interrupt controllers (setting priorities and levels). And it also configures the GPIO ports.
PLL	System Oscillator and Phase Lock Loop	System Clocking	The oscillator operates from an external crystal connected across CRIN and CROUT. The circuit can also operate from an external clock connected to CRIN. The on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5–35 MHz).

Table 3. MCF5253 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Serial data out	SDATAO1/TOUT0/GPIO18 SDATAO2/GPIO34	Audio interfaces to serial data outputs	In/Out Out	–
Word clock	LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/AUDIOCLOCK/GPIO43	Audio interfaces to serial word clocks	In/Out	–
Bit clock	SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35	Audio interfaces to serial bit clocks	In/Out	–
Serial input	EF/RXD2/GPIO6	Error flag serial in	In/Out	–
Serial input	CFLG/GPIO5	C-flag serial in	In/Out	–
Subcode clock	RCK/QSPIDIN/QSPIDOUT/ GPIO26	Audio interfaces to subcode clock	In/Out	–
Subcode sync	QSPIDOUT/SFSY/GPIO27	Audio interfaces to subcode sync	In/Out	–
Subcode data	QSPICLK/SUBR/GPIO25	Audio interfaces to subcode data	In/Out	–
Clock frequency trim	XTRIM/TXD2/GPIO0	Clock trim control	Out	–
Audio clocks out	MCLK1/GPIO11 QSPICS2/MCLK2/GPIO24	DAC output clocks	Out	–
Audio clock in	LRCK3/AUDIOCLOCK/GPIO43	Optional audio clock input		–
MemoryStick/ SecureDigital interface	EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command lane—MemoryStick interface 2 data I/O	In/Out	–
	EBUIN2/SCLKOUT/GPIO13	Clock out for both MemoryStick interfaces and for Secure Digital	In/Out	–
	DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	SecureDigital serial data bit 0—MemoryStick interface 1 data I/O	In/Out	–
	SCL0/SDATA1_BS1/GPIO41	SecureDigital serial data bit 1—MemoryStick interface 1 strobe	In/Out	–
	DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	SecureDigital serial data bit 2—MemoryStick interface 2 strobe Reset output signal	In/Out	–
	SDA0/SDATA3/GPIO42	SecureDigital serial data bit 3	In/Out	–

Table 3. MCF5253 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
QSPI data out	RCK/QSPIDIN/QSPIDOUT/GPIO26 QSPIDOUT/SFSY/GPIO27	QSPI data out	In/Out	–
QSPI chip selects	QSPICS0/EBUIN4/GPIO15 QSPICS1/EBUOUT2/GPIO16 QSPICS2/MCLK2/GPIO24 $\overline{\text{CS1}}$/QSPICS3/GPIO28	QSPI chip selects	In/Out	–
System oscillator in	CRIN	System input	In	–
System oscillator out	CROUT	System output	Out	–
Reset In	$\overline{\text{RSTI}}$	Processor reset input	In	–
Freescale Test Mode	TEST[2:0]	TEST pins.	In	–
Linear regulator output	LINOUT	Output of 1.2 V to supply core	Out	–
Linear regulator input	LININ	Input, typically I/O supply (3.3V)	In	–
Linear regulator ground	LINGND			–
High Impedance	$\overline{\text{HI\_Z}}$	Assertion tri-states output signal pins	In	
Debug Data	DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1 DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2 DDATA2/$\overline{\text{CTS0}}$/GPIO3 DDATA3/$\overline{\text{RTS0}}$/GPIO4	Display of captured processor data and break-point statuses	In/Out	Hi-Z
Processor Status	PST0/GPIO50 PST1/GPIO49 PST2/INTMON2/GPIO48 PST3/INTMON1/GPIO47	Indication of internal processor status.	In/Out	Hi-Z
Processor clock	PSTCLK/GPIO51	Processor clock output	Out	–
Test Clock	TCK	Clock signal for IEEE 1149.1A JTAG	In	–
Test Reset/ Development Serial Clock	DSCLK/$\overline{\text{TRST}}$	Multiplexed signal that is asynchronous reset for JTAG controller. Also, clock input for debug module.	In	–
Test Mode Select/Break Point	TMS/$\overline{\text{BKPT}}$	Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode	In	–
Test Data Input/ Development Serial Input	TDI/DSI	Multiplexed serial input for the JTAG or background debug module.	In	–
Test Data Output/Development Serial Output	TDO/DSO	Multiplexed serial output for the JTAG or background debug module	Out	–

Table 6. Recommended Operating Supply Voltages (continued)

Pin Name	Min	Typ	Max	Unit
USBGND	–	GND	–	V
RTCVDDA	3.0	–	4.2	V
RTCVSSA	–	GND	–	V
PLLCOREVDD	1.08	1.2	1.32	V
PLLCOREGND	–	GND	–	V
LININ	3.0	3.3	3.6	V
GND	–	GND	–	V

Table 7 provides the operating parameters for the linear regulator.

Table 7. Linear Regulator Operating Parameters

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage (LININ)	Vin	3.0	3.3	3.6	V
Output Voltage (LINOUT)	Vout	1.08	1.2	1.32	V
Output Current	Iout	–	100	150	mA
Power Dissipation	Pd	–	–	500	mW
Load Regulation 10% Iout ≥ 90% Iout	–	–	50	60	mV
Power Supply Rejection	PSRR	–	40	–	dB

NOTE

A pmos regulator is used as a current source in this linear regulator, so a 10 µF capacitor (ESR 0... 5 Ohm) is needed on the output pin (LINOUT) to integrate the current. Typically, this requires the use of a tantalum type capacitor.

Table 8 provides the measured parameters related to temperature for the linear regulator.

Table 8. Linear Regulator—Measured Parameters Related to Temperature

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage (LININ)	Vin	2.97	3.3	3.63	V
Output Voltage (LINOUT) 100 mA load	Vout	125 ^{o}C: 1.16:	25 ^{o}C: 1.19	-40 ^{o}C: 1.22	V
Current Consumption	Icc	-40 ^{o}C: 44	25 ^{o}C: 56	125 ^{o}C: 68	mA
Power Dissipation	Pd	-40 ^{o}C: 131	25 ^{o}C: 185	125 ^{o}C: 247	mW
Load Regulation 10% Iout ≥ 90% Iout	–	-40 ^{o}C: 46	25 ^{o}C: 57	125 ^{o}C: 70	mV

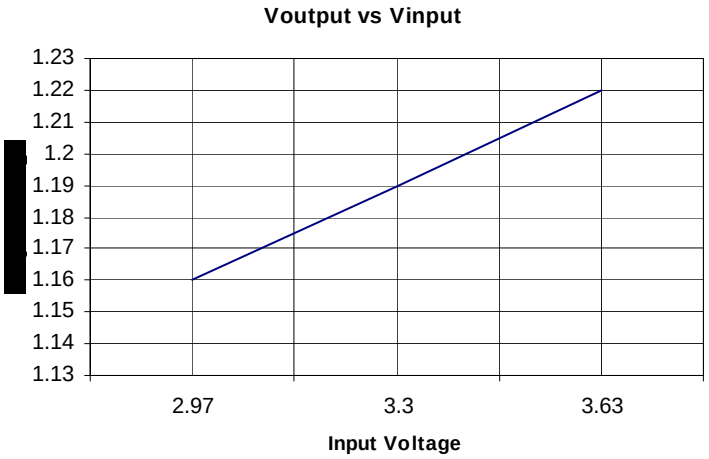

Figure 2. Linear Regulator—Voutput vs Vinput

Table 9 provides the operating parameters for the ADC DC electrical characteristics.

Table 9. Operating Parameters for ADC DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Operation Voltage Range for ADC	ADVDD	3	–	3.6	V
Common Mode Rejection	CMR	0	–	ADVDD–1.1	v
Reference Voltage (external)	ADREF	0	–	ADVDD–1.1	v
Input offset voltage	V_{offset}	–	10	–	mV
Input Hysteresis (ADINx = ADVDD/2)	V_{hyst}	0.73	0.78	0.85	mV
ADC Input Linear Operating Range	ADINx	0	–	ADVDD–1.1	V
AD Convertor Error		2			LSB
Note: Software and hardware sampling time is dependent on the external RC network used and the internal CPU Frequency and AD Converter clock divider.See Section 12.4.1 in the *MCF5253 Reference Manual* for more information.					

Table 10 provides the DC electrical specifications for the digital pins.

Table 10. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc)

Characteristic	Symbol	Min	Max	Units
Operation Voltage Range for I/O	V_{cc}	3.0	3.6	V
Input High Voltage	V_{IH}	2	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Reset Threshold Voltage - High	RtH	2.0	–	V
Reset Threshold Voltage - Low	TtL	–	0.8	V
Reset Input Rise Time	nS	10	–	–
Reset Input Fall Time	nS	10	–	–

Table 10. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc) (continued)

Characteristic	Symbol	Min	Max	Units
Input Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{in}	–	±1	µA
Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{TSI}	–	±1	µA
Output High Voltage I_{OH} = 11.9 mA[1], 6.3 mA[2],3.1 mA[3]	V_{OH}	2.4	–	V
Output Low Voltage I_{OL} = 7.1m A[1], 3.5 mA[2], 1.8 mA[3]	V_{OL}	–	0.4	V
Schmitt Trigger Low to High Threshold Point[4]	V_{T+}	1.67	1.79	V
Schmitt Trigger High to Low Threshold Point[4]	V_{T-}	1.01	1.15	V
Load Capacitance: D[31:16], SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[3:1], SDATAO[2:1], CFLG, EF, IDE_DIOR, IDE_DIOW, IDE_IORDY, MCLK1, MCLK2	C_L	–	50	pF
Load Capacitance: A[24:9], ATA_CS0, ATA_CS1, ATA_A[2:0], ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_D[15:0], SDATAI[3,1]	C_L	15	40	pF
Load Capacitance: A[8:1], ADOUT, ATA_RST BCLK, BCLKE, SDCAS, SDRAS, SDLDQM, SDCS0, SDUDQM, SDWE, BUFENB[2:1], CAN0_TX, CAN1_TX, EBUIN1, RXD[2:0]	C_L	–	30	pF
Load Capacitance: SDA0, SDA1, SCL0, SCL1, CMD_SDIO2, SDATA2_BS2, SDATA1_BS1, SDATA0_SDIO1, CS0/CS4, CS1, OE, RW, TA, TXD[2:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT0, QSPID_OUT, QSPICS[3:0], QSPICLK, GPIO[6:5]	C_L	–	20	pF
Load Capacitance: DDATA[3:0], PST[3:0], PSTCLK	C_L	–	15	pF
Capacitance[5], V_{in} = 0 V, f = 1 MHz	C_{IN}	–	6	pF

1 **8.0 mA:** SCL0, SDA0, SCL1, SDA1, PST[3:0], DDATA[3:0], TDSO, RW, ATA_RST, MCLK1, QSPICS2_MCLK2

2 **4.0 mA:** BUFENB1, BUFENB2, EBUOUT1, SCLKOUT, CMDSDIO, IDE_DIOR, IDE_DIOW, TOUT0, RTS[1:0], TXD[1:0], SCLK[4:1], LRCK[4:1], SDATAO1, SDATAO2, QSPICLK, QSPICS0, QSPICS1_EBUOUT2, QSPICS3, QSPIDOUT, RCK, XTRIM, A[8:1], ATA_CS0, ATA_CS1, ATA_A[2:0]

3 **2.0 mA:** TMS/BKPT, DSI/TDI, TRST/DSCLK

4 SCLK[4:1], SCL0, SCL1, SDA0, SDA1, ATA_DMARQ, ATA_INTRQ, ATA_IORDY

5 Capacitance C_{IN} is periodically sampled rather than 100% tested.

Table 12 shows the CRIN Crystal suggested parameters.

Table 12. CRIN Crystal Suggested Parameters

Parameter	Min	Typ	Max	Unit
Frequency	5	–	16.94	MHz
Frequency Tolerance	–	–	±50	ppm
Frequency Stability Over Operating Temperature Range	–	–	±50	ppm
ESR	–	40	–	Ω
Shunt Capacitance	–	7	–	pF
Load Capacitance	–	18	–	pF

4.1 SDRAM Bus Timing

The SDRAM bus is a synchronous bus. Propagation delays, set-up times and hold times with respect to the SDRAM clock BCLK are shown in Figure 4 and the parameters provided in Table 13. When BCLK clock is not active, SDRAM interface is not valid and the external bus cannot be used.

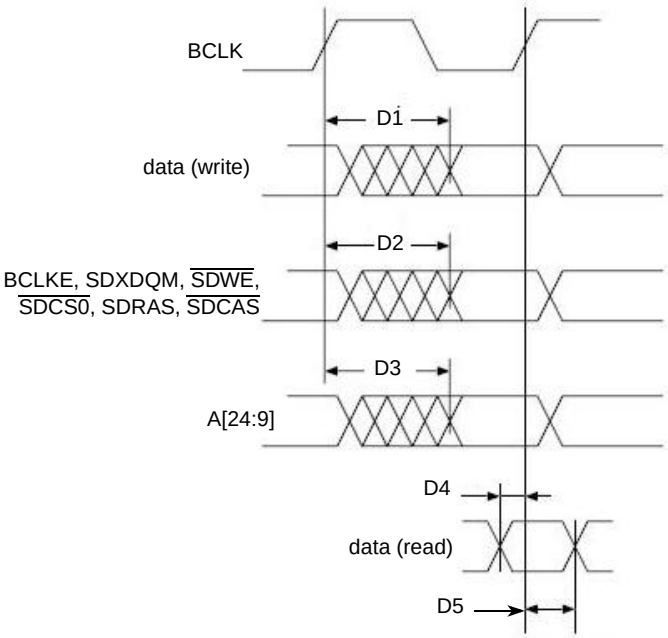

Figure 4. SDRAM Bus Timing Diagram

Table 13. SDRAM Bus Timing Parameters

ID	Characteristic	Timing to 50% Points Maximum			Units
		30 pF Load	40 pF Load	50 pF Load	
D1	Propagation delay BCLK rising to data valid	7.88	8.8	9.6	ns
D2	Propagation delay BCLK rising to BCLKE, $\overline{\text{SDLDQM}}$, $\overline{\text{SDUDQM}}$, $\overline{\text{SDWE}}$, $\overline{\text{SDCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$ valid	8.7	–	–	ns
D3	Propagation delay BCLK rising to A[24:9] valid	8.3	9.2	–	ns
D4	Set-up time data valid to BCLK rising	0	0	0	ns
D5	Hold time BCLK rising to data valid	0.7	0.7	0.7	ns

4.2 SPDIF Timing

The Sony/Philips Digital Interface (SPDIF) timing parameters are provided in Table 14. SPDIF timing is totally asynchronous, therefore there is no need for relationship with the clock. Table 14 shows the differences between high-low and low-high propagation delay which is called the skew.

Table 14. SPDIF Propagation Skew and Transition Parameters

Characteristic	Pin Load	Prop Delay Maximum	Skew[1] Maximum	Transition[2] Rise Maximum	Transition Fall Maximum	Units
EBUIN1, EBUIN2, EBUIN3, EBUIN4: asynchronous inputs, no specs apply	–	–	0.7	–	–	ns
EBUOUT1, EBUOUT2 output	40 pF	–	1.5	24.2	31.3	ns
EBUOUT1, EBUOUT2 output	20 pF	–	1.5	13.6	18.0	ns

1 Skew value does not include the skew introduced by different rise and fall times.

2 Transition times between 10% Vdd and 90% Vdd.

4.3 Serial Audio Interface Timing

The Serial Audio Interface fully complies with the Industry standard Philips IIS (InterIC Serial Audio Bus) timings.

4.4 DDATA/PST/PSTCLK Debug Interface

Table 15 provides the timing parameters.

Table 15. DDATA/PST/PSTCLK Debug Interface Timing Parameters

Characteristic	Pin Load	Min	Max	Units
PSTCLK clock rise edge to DDATA/PSTDATA[1] invalid	15 pF	–1.0	—	ns
PSTCLK clock rise edge to DDATA/PSTDATA[2] valid	15 pF	—	4.0	ns

Table 17. JTAG Timing Parameters

ID	Characteristic	Min	Max	Units
–	TCK Frequency of Operation	0	10	MHz
J1	TCK Cycle Time	100	—	ns
J2A	TCK Clock Pulse High Width	25	—	ns
J2B	TCK Clock Pulse Low Width	25	—	ns
J3A	TCK Fall Time (V_{IH}=2.4 V to V_{IL}=0.5 V)	—	5	ns
J3B	TCK Rise Time (V_{IL}=0.5 v to V_{IH}=2.4 V)	—	5	ns
J4	TDI, TMS to TCK rising (Input Setup)	8	—	ns
J5	TCK rising to TDI, TMS Invalid (Hold)	10	—	ns
J6	Boundary Scan Data Valid to TCK (Setup)	1	—	ns
J7	TCK to Boundary Scan Data Invalid to rising edge (Hold)	10	—	ns
J8	$\overline{\text{TRST}}$ Pulse Width (asynchronous to clock edges)	12	—	ns
J9	TCK falling to TDO Valid (signal from driven or three-state)	—	15	ns
J10	TCK falling to TDO High Impedance	2	15	ns
J11	TCK falling to Boundary Scan Data Valid (signal from driven or three-state)	—	15	ns
J12	TCK falling to Boundary Scan. Data High Impedance	1	15	ns

5 Power Consumption

Table 18 shows maximum power consumption for the MCF5253 device. Typicals will be supplied at a later time.

Table 18. Maximum Power Consumption

Supply	Maximum Current
1.2 V Core	150 mA
3.3 V I/O (with core supplied separately)	150 mA[1]
3.3 V I/O (with core supplied via internal 1.2 V regulator which is fed from the 3.3 V supply)	400 mA

1 This does not include the current required for any externally connected 3.3V device (e.g., flash, SDRAM, and other I/O devices).

6 Package Information and Pinout

This section includes the pin assignment information, contact connection diagram, and the mechanical package drawing.

The MCF5253 device is available in the following package:

- 225 MAPBGA 13 x 13 mm 0.8 mm pitch package as shown in Figure 6.

6.1 Pin Assignment

Table 19 defines all the settings of each pad. See Figure 7 for the ball map of pin locations and Table 21 for the device pin list, sorted by signal identification.

Table 19. 225 MAPBGA Pin Assignment

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
Address Bus								
A1	O / 2 mA	30	–	–	–	–	X	–
A2	O / 2 mA	30	–	–	–	–	X	–
A3	O / 2 mA	30	–	–	–	–	X	–
A4	O / 2 mA	30	–	–	–	–	X	–
A5	O / 2 mA	30	–	–	–	–	X	–
A6	O / 2 mA	30	–	–	–	–	X	–
A7	O / 2 mA	30	–	–	–	–	X	–
A8	O / 2 mA	30	–	–	–	–	X	–
A9	O / 8 mA	30	–	–	–	–	X	–
A10	O / 8 mA	30	–	–	–	–	X	–
A11	O / 8 mA	30	–	–	–	–	X	–
A12	O / 8 mA	30	–	–	–	–	X	–
A13	O / 8 mA	30	–	–	–	–	X	–
A14	O / 8 mA	30	–	–	–	–	X	–
A15	O / 8 mA	30	–	–	–	–	X	–
A16	O / 8 mA	30	–	–	–	–	X	–
A17	O / 8 mA	30	–	–	–	–	X	–
A18	O / 8 mA	30	–	–	–	–	X	–
A19	O / 8 mA	30	–	–	–	–	X	–
A20/A24	O / 8 mA	30	A20	A24	31	–	X	Audio Clock Select: 1-LRCK3 pin; 0-CRIN pin
A21	O / 8 mA	30	–	–	–	–	X	–
A22	O / 8 mA	30	–	–	–	–	X	–
A23/GPO54	O / 8 mA	30	A23	–	–	O54	X	Boot Mode Select:1-Memory connected to $\overline{CS0}$; 0-Internal boot rom
Data Bus								
D16	IO / 8 mA	40	–	–	–	–	HI_Z	–
D17	IO / 8 mA	40	–	–	–	–	HI_Z	–
D18	IO / 8 mA	40	–	–	–	–	HI_Z	–
D19	IO / 8 mA	40	–	–	–	–	HI_Z	–
D20	IO / 8 mA	40	–	–	–	–	HI_Z	–
D21	IO / 8 mA	40	–	–	–	–	HI_Z	–
D22	IO / 8 mA	40	–	–	–	–	HI_Z	–
D23	IO / 8 mA	40	–	–	–	–	HI_Z	–
D24	IO / 8 mA	40	–	–	–	–	HI_Z	–
D25	IO / 8 mA	40	–	–	–	–	HI_Z	–
D26	IO / 8 mA	40	–	–	–	–	HI_Z	–

Table 19. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
ATA_D15	IO / 8 mA	40	–	–	–	–	–	–
ATA_CS0	O / 2 mA	40	–	–	–	–	–	–
ATA_CS1	O / 2 mA	40	–	–	–	–	–	–
ATA_DIOR	O / 8 mA	40	–	–	–	–	–	–
ATA_DIOW	O / 8 mA	40	–	–	–	–	–	–
ATA_IORDY	I	–	–	–	–	–	–	–
ATA_INTRQ	I	–	–	–	–	–	–	–
ATA_DMARQ	I	–	–	–	–	–	–	–
ATA_DMACK	O / 8 mA	40	–	–	–	–	–	–
$\overline{\text{ATA\_RST}}$	O / 2 mA	40	–	–	–	–	–	–
Clock Generation								
CRIN	–	–	–	–	–	–	–	Main Processor Clock Input
CROUT	–	–	–	–	–	–	–	Main Processor Clock Output
RTC_CRIN	A	–	–	–	–	–	–	Real Time Clock (32.768 kHz) Input
RTCCROUT	A	–	–	–	–	–	–	Real Time Clock (32.768 kHz) Output
USB_CRIN	A	–	–	–	–	–	–	USB Clock (24 MHz) Input
USB_CROUT	A	–	–	–	–	–	–	USB Clock (24 MHz) Output
XTRIM/TXD2/GPIO0	IO / 2 mA	30	XTRIM	TXD2	0	IO0	–	Interrupt Capable Input
JTAG/BDM/Test								
TDO/DSO	O / 4 mA	30	–	–	–	–	–	See TEST0 Description
TDI/DSI	I	–	–	–	–	–	–	See TEST0 Description
TMS/$\overline{\text{BKPT}}$	I	–	–	–	–	–	–	See TEST0 Description
TCK	I	–	–	–	–	–	–	–
$\overline{\text{TRST}}$/DSCLK	I	–	–	–	–	–	–	See TEST0 Description
$\overline{\text{HI\_Z}}$	I	–	–	–	–	–	–	For Normal Operation Tie This Pin High
PSTCLK/GPIO51	IO / 8 mA	30	PSTCLK	–	–	IO51	–	–
PST0/GPIO50	IO / 4 mA	30	PST0	–	–	IO50	HI_Z	–
PST1/GPIO49	IO / 4 mA	30	PST1	–	–	IO49	HI_Z	–
PST2/INTMON2/ GPIO48	IO / 4 mA	30	PST2	INTMON2	17	IO48	HI_Z	–
PST3/INTMON1/ GPIO47	IO / 4 mA	30	PST3	INTMON1	18	IO47	HI_Z	–
DDATA0/$\overline{\text{CTS1}}$/ SDATA0_SDIO1/GPIO1	IO / 4 mA	30	DDATA0	$\overline{\text{CTS1}}$/SDATA 0_SDIO1	14,13	IO1	HI_Z	Interrupt Capable Input
DDATA1/$\overline{\text{RTS1}}$/ SDATA2_BS2/GPIO2	IO / 4 mA	30	DDATA1	$\overline{\text{RTS1}}$/SDATA 2_BS2	24,23	IO2	HI_Z	Interrupt Capable Input
DDATA2/$\overline{\text{CTS0}}$/GPIO3	IO / 4 mA	30	DDATA2	$\overline{\text{CTS0}}$	22	IO3	HI_Z	Interrupt Capable Input
DDATA3/$\overline{\text{RTS0}}$/GPIO4	IO / 4 mA	30	DDATA3	$\overline{\text{RTS0}}$	21	IO4	HI_Z	Interrupt Capable Input
TEST0	I	–	–	–	–	–	–	BDM/JTAG Select: 1-BDM; 0-JTAG
TEST1	I	–	–	–	–	–	–	For normal operation, tie this pin low.
TEST2	I	–	–	–	–	–	–	For normal operation, tie this pin low.
Reset/Wake-up								
RSTI	I	–	–	–	–	–	–	–

Table 19. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
$\overline{\text{WAKEUP}}$/GPIO21	IO / 2 mA	30	$\overline{\text{WAKEUP}}$	–	–	IO21	–	–
USB								
USBDN	A	–	–	–	–	–	–	–
USBDP	A	–	–	–	–	–	–	–
USBID	I	–	–	–	–	–	–	–
USBVBUS	A	–	–	–	–	–	–	–
USBRES	A	–	–	–	–	–	–	–
TESTOUT[1]	O	–	–	–	–	–	–	–
NC	–	–	–	–	–	–	–	–
Audio Interface								
SDATAI1/GPIO17	IO / 2 mA	30	SDATAI1	–	–	IO17	–	–
SDATAO1/TOUT0/ GPIO18	IO / 2 mA	30	SDATAO1	TOUT0	8	IO18	–	–
SCLK1/GPIO20	IO / 2 mA	30	SCLK1	–	–	IO20	–	–
LRCK1/GPIO19	IO / 2 mA	30	LRCK1	–	–	IO19	–	–
SDATAO2/GPIO34	IO / 2 mA	30	SDATAO2	–	–	IO34	–	–
SCLK2/GPIO22	IO / 2 mA	30	SCLK2	–	–	IO22	–	–
LRCK2/GPIO23	IO / 2 mA	30	LRCK2	–	–	IO23	–	–
SDATAI3/GPIO8	IO / 2 mA	30	SDATAI3	–	–	IO8	–	–
SCLK3/GPIO35	IO / 2 mA	30	SCLK3	–	–	IO35	–	–
LRCK3/AUDIOCLK/ GPIO43	IO / 2 mA	30	LRCK3	AUDIOCLK	–	IO43	–	See A20/A24 Description
EBUIN1/GPIO36	IO / 2 mA	30	EBUIN1	–	–	IO36	–	–
EBUIN2/SCLKOUT/ GPIO13	IO / 2 mA	30	EBUIN2	SCLKOUT	16	IO13	–	–
EBUIN3/ CMD_SDIO2/GPIO14	IO / 2 mA	30	EBUIN3	CMDSDIO2	15	IO14	–	–
QSPICS0/EBUIN4/ GPIO15	IO / 2 mA	30	QSPICS0	EBUIN4	30	IO15	–	–
EBUOUT1/GPIO37	IO / 2 mA	30	EBUOUT1	–	–	IO37	–	–
QSPICS1/ EBUOUT2/GPIO16	IO / 2 mA	30	QSPICS1	EBUOUT2	29	IO16	–	–
CFLG/GPIO5	IO / 2 mA	30	CFLG	–	–	IO5	–	Interrupt Capable Input
EF/RXD2/GPIO6	IO / 2 mA	30	EF	RXD2	–	IO6	–	Interrupt Capable Input
MCLK1/GPIO11	IO / 4 mA	30	MCLK1	–	–	IO11	–	–
QSPICS2/MCLK2/ GPIO24	IO / 4 mA	30	QSPICS2	MCLK2	28	IO24	–	–
Analog-to-Digital Converter								
ADIN0/GPI52	A	–	ADIN0	–	–	I52	–	–
ADIN1/GPI53	A	–	ADIN1	–	–	I53	–	–
ADIN2/GPI54	A	–	ADIN2	–	–	I54	–	–
ADIN3/GPI55	A	–	ADIN3	–	–	I55	–	–
ADIN4/GPI56	A	–	ADIN4	–	–	I56	–	–
ADIN5/GPI57	A	–	ADIN5	–	–	I57	–	–
ADREF	A	–	–	–	–	–	–	–
ADOUT/SCLK4/ GPIO58	IO / 2 mA	30	ADOUT	SCLK4	9	IO58	–	–

Table 19. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
FlexCAN								
CAN0_TX	O / 8 mA	30	–	–	–	–	–	–
CAN0_RX	I	–	–	–	–	–	–	–
CAN1_TX	O / 8 mA	30	–	–	–	–	–	–
CAN1_RX	I	–	–	–	–	–	–	–
QSPI								
QSPICLK/SUBR/ GPIO25	IO / 2 mA	30	QSPICLK	SUBR	27	IO25	–	–
RCK/QSPIDIN/ QSPIDOUT/GPIO26	IO / 2 mA	30	RCK	QSPIDIN/ QSPIDOUT	26	IO26	–	–
QSPIDOUT/SFSY/ GPIO27	IO / 2 mA	30	QSPIDOUT	SFSY	10	IO27	–	–
I^2C								
SDA0/SDATA3/ GPIO42	IO / 4 mA	30	SDA0	SDATA3	11	IO42	–	–
SCL0/SDATA1_BS1/ GPIO41	IO / 4 mA	30	SCL0	SDATA1_BS1	12	IO41	–	–
SDA1/RXD1/GPIO44	IO / 4 mA	30	SDA1	RXD1	19	IO44	–	–
SCL1/TXD1/GPIO10	IO / 4 mA	30	SCL1	TXD1	20	IO10	–	–
UART								
TXD0/GPIO45	IO / 2 mA	30	TXD0	–	–	IO45	–	–
RXD0/GPIO46	IO / 2 mA	30	RXD0	–	–	IO46	–	–
Power/Ground Pins								
LININ	–	–	–	–	–	–	–	3.3 Volt Supply Required
LINOUT	–	–	–	–	–	–	–	1.2 Volt Output (Approx 50% Efficient)
LINGND	–	–	–	–	–	–	–	–
PLLCOREVDD (3 Balls)	–	–	–	–	–	–	–	1.2 Volt Supply Required (M4, N3, P2)
PLLCOREGND (3 Balls)	–	–	–	–	–	–	–	N4,P3,R2
USBVDD (2 Balls)	–	–	–	–	–	–	–	3.3 Volt Supply Required (L13, M13)
USBVDDP	–	–	–	–	–	–	–	1.2 Volt Supply Required
USBGND (3 Balls)	–	–	–	–	–	–	–	K11, L11, M12
OSCPADVDD	–	–	–	–	–	–	–	3.3 Volt Supply Required
OSCPADGND	–	–	–	–	–	–	–	–
RTC_VDDA	–	–	–	–	–	–	–	3.3 Volt Supply Required
RTCVSSA	–	–	–	–	–	–	–	–
ADVDD	–	–	–	–	–	–	–	3.3 Volt Supply Required
ADGND	–	–	–	–	–	–	–	–
PADVDD (10 Balls)	–	–	–	–	–	–	–	3.3 Volt Supply Required (E7, E9, F10, H8, H11, K5, L6, L8, L10, R13)

Table 19. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
COREVDD (4 Balls)	–	–	–	–	–	–	–	1.2 Volt Supply Required (G8, H7, H9, J8)
COREVSS/PADVSS (18 Balls)[2]	–	–	–	–	–	–	–	A1, A15, E8, E10, F7, G6, G7, G9, G11, J7, J9, J10, J11, L5, L7, L9, R1, R15

1 For test purposes only. Leave ball as open circuit.

2 These pads are listed as “GND” in the ball map and the rest of the tables.

Table 21. MCF5253 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
ATA_A0	A08
ATA_A1	B07
ATA_A2	B08
ATA_CS0	C09
ATA_CS1	D09
ATA_D0	B09
ATA_D1	A09
ATA_D10	C11
ATA_D11	A11
ATA_D12	A12
ATA_D13	E11
ATA_D14	B12
ATA_D15	D12
ATA_D2	F08
ATA_D3	F09
ATA_D4	B10
ATA_D5	C10
ATA_D6	A10
ATA_D7	D10
ATA_D8	D11
ATA_D9	B11
ATA_DIOR	B15
ATA_DIOW	A13
ATA_DMACK	C12
ATA_DMARQ	A07
ATA_INTRQ	D08
ATA_IORDY	D07
$\overline{\text{ATA\_RST}}$	C08
BCLK/GPIO40	B05
BCLKE/GPIO63	E06
$\overline{\text{BUFENB1}}$/GPIO29	P05
$\overline{\text{BUFENB2}}$/GPIO30	K06
CAN0_RX	D13
CAN0_TX	C15
CAN1_RX	E12
CAN1_TX	C14
CFLG/GPIO5	M09
COREVDD	G08
COREVDD	H07
COREVDD	H09
COREVDD	J08
CRIN	M03
CROUT	N02
$\overline{\text{CS0}}$/$\overline{\text{CS4}}$	J03
$\overline{\text{CS1}}$/QSPICS3/GPIO28	M07
D16	C01

Table 21. MCF5253 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
D17	E04
D18	E05
D19	B01
D20	C02
D21	D04
D22	C03
D23	B02
D24	A02
D25	B03
D26	A03
D27	C04
D28	B04
D29	D05
D30	A04
D31	C05
DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	K10
DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	R11
DDATA2/$\overline{\text{CTS0}}$/GPIO3	J14
DDATA3/$\overline{\text{RTS0}}$/GPIO4	J12
EBUIN1/GPIO36	N06
EBUIN2/SCLKOUT/GPIO13	M06
EBUIN3/CMD_SDIO2/GPIO14	K07
EBUOUT1/GPIO37	P06
EF/RXD2/GPIO6	R09
GND	A01
GND	A15
GND	E08
GND	E10
GND	F07
GND	G06
GND	G07
GND	G09
GND	G11
GND	J07
GND	J09
GND	J10
GND	J11
GND	L05
GND	L07
GND	L09
GND	R01
GND	R15
$\overline{\text{HI\_Z}}$	B13
$\overline{\text{IDE\_DIOR}}$/GPIO31	M05
$\overline{\text{IDE\_DIOW}}$/GPIO32	P04
$\overline{\text{IDE\_IORDY}}$/GPIO33	R04

Table 21. MCF5253 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
LINGND	C13
LININ	A14
LINOUT	B14
LRCK1/GPIO19	P08
LRCK2/GPIO23	E14
LRCK3/AUDIOCLK/GPIO43	M10
MCLK1/GPIO11	D14
NC	R14
$\overline{OE}$	R03
OSCPADGND	P01
OSCPADVDD	N01
PADVDD	E07
PADVDD	E09
PADVDD	F10
PADVDD	H08
PADVDD	H11
PADVDD	K05
PADVDD	L06
PADVDD	L08
PADVDD	L10
PADVDD	R13
PLLAVDD	M04
PLLCOREGND	N04
PLLCOREGND	P03
PLLCOREGND	R02
PLLCOREVDD	N03
PLLCOREVDD	P02
PST0/GPIO50	G15
PST1/GPIO49	G12
PST2/INTMON2/GPIO48	H14
PST3/INTMON1/GPIO47	H13
PSTCLK/GPIO51	G14
QSPICLK/SUBR/GPIO25	P07
QSPICS0/EBUIN4/GPIO15	R07
QSPICS1/EBUOUT2/GPIO16	N08
QSPICS2/MCLK2/GPIO24	P09
QSPIDOUT/SFSY/GPIO27	M08
RCK/QSPIDIN/QSPIDOUT/GPIO26	N07
RSTI	E15
RTC_CRIN	J01
RTC_VDDA	J02
RTCCROUT	K02
RTCVSSA	K01
RW	J04
RXD0/GPIO46	H15
SCL0/SDATA1_BS1/GPIO41	P10

Table 21. MCF5253 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
SCL1/TXD1/GPIO10	J13
SCLK1/GPIO20	K08
SCLK2/GPIO22	E13
SCLK3/GPIO35	R10
SDA0/SDATA3/GPIO42	K09
SDA1/RXD1/GPIO44	J15
SDATAI1/GPIO17	N09
SDATAI3/GPIO8	N10
SDATAO1/TOUT0/GPIO18	R08
SDATAO2/GPIO34	D15
$\overline{\text{SDCAS}}$/GPIO39	D06
$\overline{\text{SDCS0}}$/GPIO60	B06
$\overline{\text{SDLDQM}}$/GPO52	C06
$\overline{\text{SDRAS}}$/GPIO59	A06
$\overline{\text{SDUDQM}}$/GPO53	A05
$\overline{\text{SDWE}}$/GPIO38	C07
$\overline{\text{TA}}$/GPIO12	N05
TCK	F13
TDI/DSI	F15
TDO/DSO	G13
TEST0	F11
TEST1	G10
TEST2	H10
TESTOUT	P13
TMS/$\overline{\text{BKPT}}$	F12
$\overline{\text{TRST}}$/DSCLK	F14
TXD0/GPIO45	H12
USB_CRIN	L14
USB_CROUT	L15
USBDN	N15
USBDP	M15
USBGND	K11
USBGND	L11
USBGND	M12
USBID	M11
USBRES	M14
USBVBUS	N14
USBVDD	L13
USBVDD	M13
USBVDDP	L12
$\overline{\text{WAKEUP}}$/GPIO21	R05
XTRIM/TXD2/GPIO0	R06

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