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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5633mf1mlq80r

MPC5634M_AD
Rev. 1.0, 01/2015

MPC5634M Microcontroller Datasheet Addendum

This addendum describes corrections to the *MPC5634M Microcontroller Datasheet*, order number MPC5634M. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/powerarchitecture for the latest updates.

The current version available of the *MPC5634M Microcontroller Datasheet* is Revision 9.

Table of Contents

freescale™ semiconductor

- Frequency Modulating Phase-locked loop (FMPLL)
  - Reference clock pre-divider (PREDIV) for finer frequency synthesis resolution
  - Reduced frequency divider (RFD) for reducing the FMPLL output clock frequency without forcing the FMPLL to re-lock
  - System clock divider (SYSDIV) for reducing the system clock frequency in normal or bypass mode
  - Input clock frequency range from 4 MHz to 20 MHz before the pre-divider, and from 4 MHz to 16 MHz at the FMPLL input
  - Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
  - VCO free-running frequency range from 25 MHz to 125 MHz
  - Four bypass modes: crystal or external reference with PLL on or off
  - Two normal modes: crystal or external reference
  - Programmable frequency modulation
    - Triangle wave modulation
    - Register programmable modulation frequency and depth
  - Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
    - User-selectable ability to generate an interrupt request upon loss of lock
    - User-selectable ability to generate a system reset upon loss of lock
  - Clock quality monitor (CQM) module provides loss-of-clock detection for the FMPLL reference and output clocks
    - User-selectable ability to generate an interrupt request upon loss of clock
    - User-selectable ability to generate a system reset upon loss of clock
    - Backup clock (reference clock or FMPLL free-running) can be applied to the system in case of loss of clock
- Calibration bus interface (EBI)
  - Available only in the calibration package (496 CSP package)
  - 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
  - Memory controller with support for various memory types
  - 16-bit data bus, up to 22-bit address bus
  - Selectable drive strength
  - Configurable bus speed modes
  - Bus monitor
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 80 I/O pins
  - Centralized pad control on a per-pin basis
    - Pin function selection
    - Configurable weak pull-up or pull-down
    - Drive strength
    - Slew rate
    - Hysteresis
  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
  - Critical Interrupt control
  - Non-Maskable Interrupt control
  - Internal multiplexer subblock (IMUX)
    - Allows flexible selection of eQADC trigger inputs (eTPU, eMIOS and external signals)

- Enabled out of reset

- Enhanced modular I/O system (eMIOS)
  - 16 timer channels (up to 14 channels in 144 LQFP)
  - 24-bit timer resolution
  - Supports a subset of the timer modes found in eMIOS on MPC5554
  - 3 selectable time bases plus shared time or angle counter bus from eTPU2
  - DMA and interrupt request support
  - Motor control capability
- Second-generation enhanced time processor unit (eTPU2)
  - Object-code compatible with eTPU—no changes are required to hardware or software if only eTPU features are used
  - Intelligent co-processor designed for timing control
  - High level tools, assembler and compiler available
  - 32 channels (each channel has dedicated I/O pin in all packages)
  - 24-bit timer resolution
  - 14 KB code memory and 3 KB data memory
  - Double match and capture on all channels
  - Angle clock hardware support
  - Shared time or angle counter bus with eMIOS
  - DMA and interrupt request support
  - Nexus Class 1 debug support
  - eTPU2 enhancements
    - Counters and channels can run at full system clock speed
    - Software watchdog
    - Real-time performance monitor
    - Instruction set enhancements for smaller more flexible code generation
    - Programmable channel mode for customization of channel operation
- Enhanced queued A/D converter (eQADC)
  - Two independent on-chip redundant signed digit (RSD) cyclic ADCs
    - 8-, 10-, and 12-bit resolution
    - Differential conversions
    - Targets up to 10-bit accuracy at 500 KSample/s (ADC_CLK = 7.5 MHz) and 8-bit accuracy at 1 MSample/s (ADC_CLK = 15 MHz) for differential conversions
    - Differential channels include variable gain amplifier (VGA) for improved dynamic range (×1; ×2; ×4)
    - Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ; 100 kΩ; low value of 5 kΩ)
    - Single-ended signal range from 0 to 5 V
    - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
    - Provides time stamp information when requested
    - Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
    - Supports both right-justified unsigned and signed formats for conversion results
    - Temperature sensor to enable measurement of die temperature
    - Ability to measure all power supply pins directly
  - Automatic application of ADC calibration constants
    - Provision of reference voltages (25% VREF and 75% VREF) for ADC calibration purposes
  - Up to 34[1] input channels available to the two on-chip ADCs

- Four pairs of differential analog input channels
- Full duplex synchronous serial interface to an external device
  - Has a free-running clock for use by the external device
  - Supports a 26-bit message length
  - Transmits a null message when there are no triggered CFIFOs with commands bound for external CBuffers, or when there are triggered CFIFOs with commands bound for external CBuffers but the external CBuffers are full
- Parallel Side Interface to communicate with an on-chip companion module
- Zero jitter triggering for queue 0. (Queue 0 trigger causes current conversion to be aborted and the queued conversions in the CBUFFER to be bypassed. Delay from Trigger to start of conversion is 13 system clocks + 1 ADC clock.)
- eQADC Result Streaming. Generation of a continuous stream of ADC conversion results from a single eQADC command word. Controlled by two different trigger signals; one to define the rate at which results are generated and the other to define the beginning and ending of the stream. Used to digitize waveforms during specific time/angle windows, e.g., engine knock sensor sampling.
- Angular Decimation. The ability of the eQADC to sample an analog waveform in the time domain, perform Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filtering also in the time domain, but to down sample the results in the angle domain. Resulting in a time domain filtered result at a given engine angle.
- Priority Based CFIFOs
  - Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
  - Supports software and several hardware trigger modes to arm a particular CFIFO
  - Generates interrupt when command coherency is not achieved
- External Hardware Triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Supports four external 8-to-1 muxes which can expand the input channel number from 34[1] to 59

- Two deserial serial peripheral interface modules (DSPI)
  - SPI
    - Full duplex communication ports with interrupt and DMA request support
    - Supports all functional modes from QSPI subblock of QSMCM (MPC5xx family)
    - Support for queues in RAM
    - 6 chip selects, expandable to 64 with external demultiplexers
    - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
    - Modified SPI mode for interfacing to peripherals with longer setup time requirements
    - LVDS option for output clock and data to allow higher speed communication
  - Deserial serial interface (DSI)
    - Pin reduction by hardware serialization and deserialization of eTPU, eMIOS channels and GPIO
    - 32 bits per DSPI module
    - Triggered transfer control and change in data transfer control (for reduced EMI)
    - Compatible with Microsecond Channel Version 1.0 downstream
- Two enhanced serial communication interface (eSCI) modules
  - UART mode provides NRZ format and half or full duplex interface
  - eSCI bit rate up to 1 Mbps

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.
1. 176-pin and 208-ball packages.

results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12 bit, 10 bit, 8 bit)
    - 12-bit conversion time – 1 µs (1M sample/sec)
    - 10-bit conversion time – 867 ns (1.2M sample/second)
    - 8-bit conversion time – 733 ns (1.4M sample/second)
  - Up to 10-bit accuracy at 500 KSample/s and 9-bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
- Up to 34[1] input channels (accessible by both ADCs)
- 23 additional internal channels for measuring control and monitoring voltages inside the device
  - Including Core voltage, I/O voltage, LVI voltages, etc.
- An internal bandgap reference to allow absolute voltage measurements
- 4 pairs of differential analog input channels
  - Programmable pull-up/pull-down resistors on each differential input for biasing and sensor diagnostic (200 kΩ, 100 kΩ, 5 kΩ)
- Silicon die temperature sensor
  - provides temperature of silicon as an analog value
  - read using an internal ADC analog channel
  - may be read with either ADC
- Decimation Filter
  - Programmable decimation factor (2 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Pre-fill mode to pre-condition the filter before the sample window opens
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based Queues
  - Supports six Queues with fixed priority. When commands of distinct Queues are bound for the same ADC, the higher priority Queue is always served first

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.

  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 MDO (message data out) pins
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- 17-pin Full Port interface in calibration package used on VertiCal boards
  - 3.3 V interface
  - Auxiliary Output port
    - 1 MCKO (message clock out) pin
    - 4 (reduced port mode) or 12 (full port mode) MDO (message data out) pins; 8 extra full port pins shared with calibration bus
    - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
    - 1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
    - 1 $\overline{\text{EVTI}}$ (event in) pin
- Host processor (e200) development support features
  - IEEE-ISTO 5001-2003 standard class 2 compliant
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint trigger enable of program trace messaging
  - Data Value Breakpoints (JTAG feature of the e200z335 core): allows CPU to be halted when the CPU writes a specific value to a memory location
    - 4 data value breakpoints
    - CPU only
    - Detects ‘equal’ and ‘not equal’
    - Byte, half word, word (naturally aligned)

NOTE

This feature is imprecise due to CPU pipelining.

  - Subset of Power Architecture software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support (JTAG feature of the eTPU)
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

2.2.20.2 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001

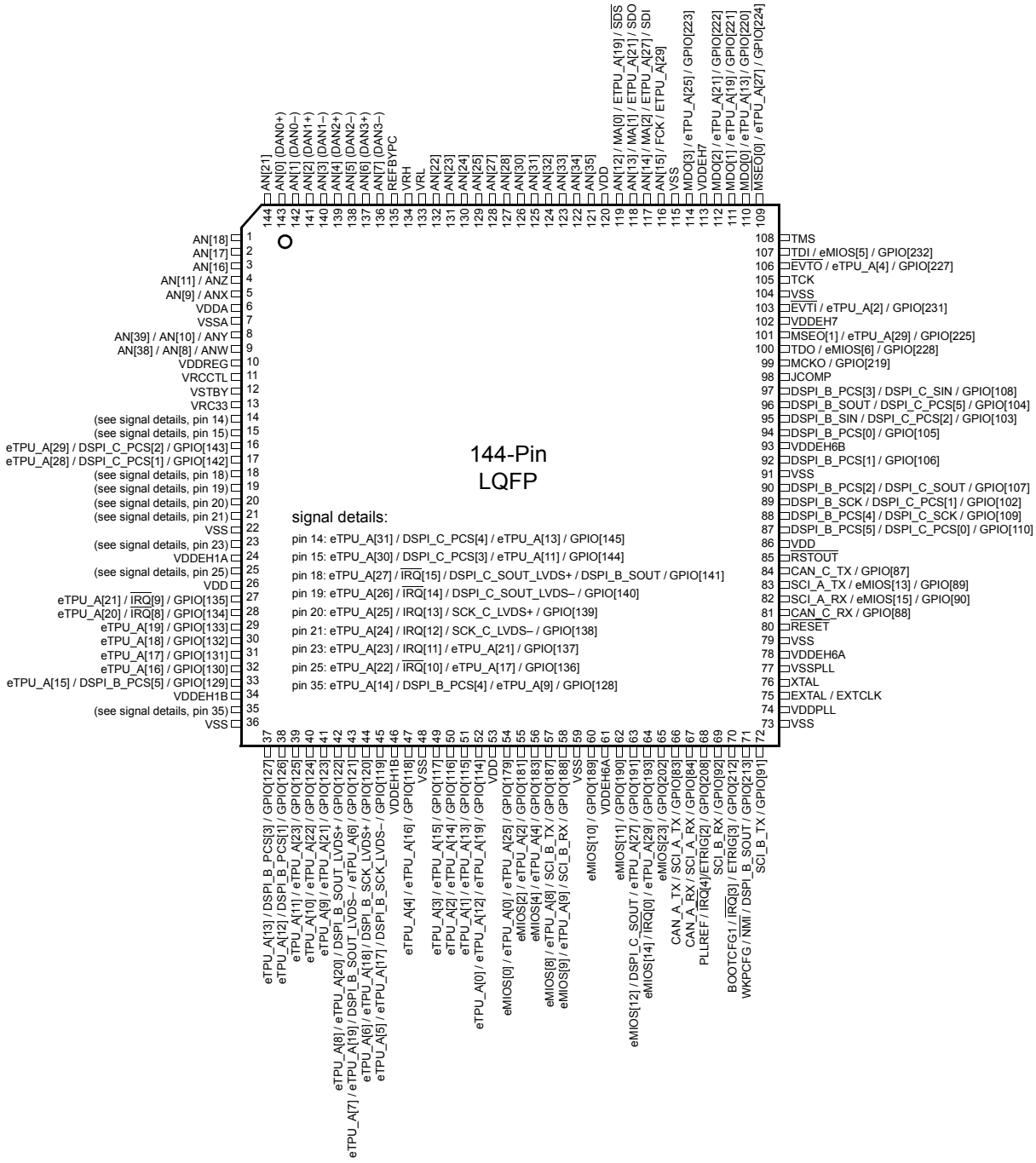

Figure 2. 144-pin LQFP pinout (top view; all 144-pin devices)

3.2 176 LQFP pinout (MPC5634M)

Figure 3 shows the 176-pin LQFP pinout for the MPC5634M (1536 KB flash memory).

3.5 208 MAPBGA ballmap (MPC5633M only)

Figure 6 shows the 208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	ALT_ MSEO0	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_EVTO	NIC[1]
E	ETPUA30	ETPUA31	NC[2]	VDD									VDDE7	TDI	ALT_ EVTI	ALT_ MSEO1
F	ETPUA28	ETPUA29	ETPUA26	NC[2]									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			NC[2]	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	NC[2]	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	RSTOUT	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	RESET
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[3]	EMIOS12	eTPUA19[4]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	NC[2]	VDDE7	NIC[1]	EMIOS8	eTPUA29[3]	eTPUA2[3]	eTPUA21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	NC[2]	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPUA27[3]	EMIOS23	CAN_A_ RX	NC[2]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	NC[2]	GPIO219	eTPUA25[3]	NC[2]	NC[2]	eTPUA4[3]	eTPUA13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 Pins marked “NC” may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.
3 This ball may be changed to “NC” (no connection) in a future revision.
4 eTPU output only channel.

Figure 6. 208-pin MAPBGA ballmap (MPC5633M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
CAL_ADDR[16][21] ALT_MDO[0][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	MDO / ALT_ADDR[12] / Low		—	17	A14
CAL_ADDR[17][21] ALT_MDO[1][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	18	B14
CAL_ADDR[18][21] ALT_MDO[2][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	19	A13
CAL_ADDR[19][21] ALT_MDO[3][12]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[15]	ALT_MDO / CAL_ADDR[12] / Low		—	20	B13
CAL_ADDR[20:27] ALT_MDO[4:11]	Calibration Address Bus Nexus Msg Data Out	PCR[345]	—	O O	VDDE12[13] Fast	O / Low	ALT_MDO / CAL_ADDR[16] / Low		—	—	—
CAL_ADDR[28][21] ALT_$\overline{\text{MSEO}}$[0][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	118	C15
CAL_ADDR[29][21] ALT_$\overline{\text{MSEO}}$[1][12]	Calibration Address Bus Nexus Msg Start/End Out	PCR[345]	—	O O	VDDE12[13] VDDE7[14] Fast	O / Low[17]	ALT_$\overline{\text{MSEO}}$[16] / CAL_ADDR[17]/ Low		—	117	E16
CAL_ADDR[30][21] ALT_$\overline{\text{EVTI}}$[12]	Calibration Address Bus Nexus Event In	PCR[345]	—	O I	VDDE12[13] VDDE7[14] Fast	—[18]	ALT_$\overline{\text{EVTI}}$ / CAL_ADDR[19]		—	116	E15
ALT_$\overline{\text{EVTO}}$	Nexus Event Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_$\overline{\text{EVTO}}$ / High		—	120	D15
ALT_MCKO	Nexus Msg Clock Out	PCR[344]	—	O	VDDE12[13] VDDE7[14] Fast	O / Low	ALT_MCKO / Enabled		—	14	F15
NEXUSCFG[11]	Nexus/Calibration bus selector	—	—	I	VDDE12 Fast	I / Down	NEXUSCFG / Down		—	—	—
CAL_$\overline{\text{CS}}$[0][11]	Calibration Chip Selects	PCR[336]	—	O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—
CAL_$\overline{\text{CS}}$[2][11] CAL_ADDR[10]	Calibration Chip Selects Calibration Address Bus	PCR[338]	11 10	O O	VDDE12 Fast	O / High	CAL_$\overline{\text{CS}}$ / High		—	—	—

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPB GA
eTPU_A[28][28] DSPI_C_PCS[1] GPIO[142]	eTPU_A Ch. (Input and Output) DSPI_C Periph Chip Select GPIO	PCR[142]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		17	24	F1
eTPU_A[29][28] DSPI_C_PCS[2] GPIO[143]	eTPU_A Ch. (Input and Output) DSPI_C Periph Chip Select GPIO	PCR[143]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		16	23	F2
eTPU_A[30] DSPI_C_PCS[3] eTPU_A[11] GPIO[144]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[144]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		15	22	E1
eTPU_A[31] DSPI_C_PCS[4] eTPU_A[13] GPIO[145]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[145]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		14	21	E2
eMIOS											
eMIOS[0] eTPU_A[0] eTPU_A[25][29] GPIO[179]	eMIOS Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[179]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		54	63	T4
eMIOS[1] eTPU_A[1] GPIO[180]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[180]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		—	64[7]	T5[8]
eMIOS[2] eTPU_A[2] GPIO[181]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[181]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		55	65	N7
eMIOS[4] eTPU_A[4] GPIO[183]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[183]	01 10 00	I/O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		56	67	R5
eMIOS[8] eTPU_A[8][30] SCI_B_TX GPIO[187]	eMIOS Ch. eTPU_A Ch. eSCI_B Transmit GPIO	PCR[187]	001 010 100 000	I/O O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		57	70	P8

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
eMIOS[9] eTPU_A[9][30] SCI_B_RX GPIO[188]	eMIOS Ch. eTPU_A Ch. eSCI_B Receive GPIO	PCR[188]	001 010 100 000	I/O O I I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		58	71	R7
eMIOS[10] GPIO[189]	eMIOS Ch. GPIO	PCR[189]	01 00	I/O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		60	73	N8
eMIOS[11] GPIO[190]	eMIOS Ch. GPIO	PCR[190]	01 00	I/O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		62	75	R8
eMIOS[12] DSPI_C_SOUT eTPU_A[27] GPIO[191]	eMIOS Ch. DSPI C Data Output eTPU_A Ch. GPIO	PCR[191]	001 010 100 000	I/O O O I/O	VDDEH6a Medium	– / WKPCFG	– / WKPCFG		63	76	N10
eMIOS[13] GPIO[192]	eMIOS Ch. GPIO	PCR[192]	01 00	I/O I/O	VDDEH6a	– / WKPCFG	– / WKPCFG		—	77[7]	T8[8]
eMIOS[14] $\overline{\text{IRQ}}$[0] eTPU_A[29] GPIO[193]	eMIOS Ch. External Interrupt Request eTPU_A Ch. GPIO	PCR[193]	001 010 100 000	O I O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		64	78	R9
eMIOS[15] $\overline{\text{IRQ}}$[1] GPIO[194]	eMIOS Ch. External Interrupt Request GPIO	PCR[194]	01 10 00	O I I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		—	79[7]	T9[8]
eMIOS[23] GPIO[202]	eMIOS Ch. GPIO	PCR[202]	01 00	I/O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		65	80	R11
Clock Synthesizer											
XTAL	Crystal Oscillator Output	—	—	O	VDDEH6a	O / –	XTAL[31] / –		76	93	P16
EXTAL EXTCLK	Crystal Oscillator Input External Clock Input	—	—	I	VDDEH6a	I / –	EXTAL[32] / –		75	92	N16
CLKOUT	System Clock Output	PCR[229]	—	O	VDDE5 Fast	CLKOUT / Enabled	CLKOUT / Enabled		—	—	T14
Power / Ground											
VDDPLL	PLL Supply Voltage	—	—	I	VDDPLL (1.2V)	I / –	—		74	91	R16
VSSPLL[33]	PLL Ground	—	—	I	VSSPLL	I / –	—		77	94	M16

[39] VDDEH6A and VDDEH6B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[40] If using JTAG or Nexus, the I/O segment that contains the JTAG and Nexus pins must be powered by a 5 V supply. The 3.3 V Nexus/JTAG signals are derived from the 5 volt power supply.

[41] In the calibration package this signal is named VDDE12.

Table 3. Pad types

Pad Type	Name	Supply Voltage
Slow	pad_ssr_hv	3.0 V – 5.25 V
Medium	pad_msr_hv	3.0 V – 5.25 V
Fast	pad_fc	3.0 V – 3.6 V
MultiV	pad_multv_hv	3.0 V – 5.25 V (high swing mode) 4.5 V – 5.25 V (low swing mode)
Analog	pad_ae_hv	0.0 – 5.25 V
LVDS	pad_lo_lv	—

Table 9. Thermal characteristics for 176-pin LQFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 10. Thermal characteristics for 208-pin MAPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2,3]	One layer board - 1s	39	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient natural convection[2,4]	Four layer board - 2s2p	24	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Single layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

4.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 19. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200–600[1]	mV
V_{BE}	Base-to-emitter voltage	0.4–1.0	V

[1] Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}

4.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification but use of the following sequence is strongly recommended when the internal regulator is bypassed:

5 V → 3.3 V and 1.2 V

This is also the normal sequence when the internal regulator is enabled.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to table Table 20 for all pins with fast pads and Table 21 for all pins with medium, slow and multi-voltage pads.[1]

Table 20. Power sequence pin states for fast pads

V_{DDE}	V_{RC33}	V_{DD}	Fast (pad_fc)
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 21. Power sequence pin states for medium, slow and multi-voltage pads

V_{DDEH}	V_{DD}	Medium (pad_msr_hv) Slow (pad_ssr_hv) Multi-voltage (pad_multv_hv)
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

1.If an external 3.3V external regulator is used to supply current to the 1.2V pass transistor and this supply also supplies current for the other 3.3V supplies, then the 5V supply must always be greater than or equal to the external 3.3V supply.

[8] V_{FLASH} is only available in the calibration package.

[9] Regulator is functional, with derated performance, with supply voltage down to 4.0 V.

[10] Multi-voltage pads (type pad_multv_hv) must be supplied with a power supply between 4.75 V and 5.25 V.

[11] The slew rate (SRC) setting must be 0b11 when in low-swing mode.

[12] While in low-swing mode there are no restrictions in transitioning to high-swing mode.

[13] Pin in low-swing mode can accept a 5 V input.

[14] Values are pending characterization.

[15] Pin in low-swing mode can accept a 5 V input.

[16] Characterization based capability:

IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with VDDEH=4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with VDDEH=3.0 V

[17] Characterization based capability:

IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with VDDE=3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with VDDE=2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with VDDE=1.62 V

[18] All VOL/VOH values 100% tested with ± 2 mA load.

[19] Run mode as follows:

System clock = 40/60/80 MHz + FM 2%
Code executed from flash memory
ADC0 at 16 MHz with DMA enabled
ADC1 at 8 MHz
eMIOS pads toggle in PWM mode with a rate between 100 kHz and 500 kHz
eTPU pads toggle in PWM mode with a rate between 10 kHz and 500 kHz
CAN configured for a bit rate of 500 kHz
DSPI configured in master mode with a bit rate of 2 MHz
eSCI transmission configured with a bit rate of 100 kHz

[20] Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 × PWM channels at 1 kHz, all other modules stopped.

[21] Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.

[22] When using the internal regulator only, a bypass capacitor should be connected to this pin. External circuits should not be powered by the internal regulator. The internal regulator can be used as a reference for an external debugger.

[23] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 23 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[24] Absolute value of current, measured at V_{IL} and V_{IH}.

[25] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: fast (pad_fc).

[26] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

[27] Applies to CLKOUT, external bus pins, and Nexus pins.

[28] Applies to the FCK, SDI, SDO, and $\overline{SDS}$ pins.

[29] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

[30] When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from external devices, the resulting pad voltage will be 0.5*V_{DDE} ± 2.5%

Table 26. DSPI LVDS pad specification [1, 2] (continued)

12	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	CC	D				0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D		95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

1 These are typical values that are estimated from simulation.

2 These specifications are subject to change per device characterization.

3 Preliminary target values. Actual specifications to be determined.

4.10 Oscillator and PLLMRFM electrical characteristics

Table 27. PLLMRFM electrical specifications[1]

(V_{DDPLL} =1.14 V to 1.32 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
$f_{ref\_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[2]		Crystal reference	4	20	MHz
		C			External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
f_{vco}	CC	P	VCO frequency range[3]		—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]		—	16	80	MHz
f_{sys}	CC	T	System frequency in bypass mode[4]		Crystal reference	4	20	MHz
		P			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[5]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [6,7]		—	1.2	75	MHz
C_{JITTER}	CC	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [12, 13]		—	—	10	ms
V_{IHEXT}	CC	T	EXTAL input high voltage		Crystal Mode[14], 0.8 ≤ Vxtal ≤ 1.5V[15]	Vxtal + 0.4	—	V
		T			External Reference[14, 16]	V_{RC33}/2 + 0.4	V_{RC33}	

Table 34. Pad AC specifications (3.3 V)[1] (continued)

Pad Type		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Fast	CC	D		2.5/2.5		1.2/1.2	10	00
	CC	D		2.5/2.5		1.2/1.2	20	01
	CC	D		2.5/2.5		1.2/1.2	30	10
	CC	D		2.5/2.5		1.2/1.2	50	11[8]
pad_i_hv[12]	CC	D	0.5/0.5	3/3	0.4/0.4	1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V, V_{DDEH} = 3 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads

6 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

7 Output delay is shown in Figure 8. Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Can be used on the tester

9 This drive select value is not supported. If selected, it will be approximately equal to 11.

10 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

11 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

12 Stand alone input buffer. Also has weak pull-up/pull-down.

Table 35. Pad AC specifications (1.8 V)

Pad Type		C	Output Delay (ns)[1,2] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Fast	CC	D		3.0/3.0	2.0/1.5		10	00
	CC	D		3.0/3.0	2.0/1.5		20	01
	CC	D		3.0/3.0	2.0/1.5		30	10
	CC	D		3.0/3.0	2.0/1.5		50	11[4]

1 This parameter is supplied for reference and is not guaranteed by design and not tested.

2 Delay and rise/fall are measured to 20% or 80% of the respective signal.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Can be used on the tester.

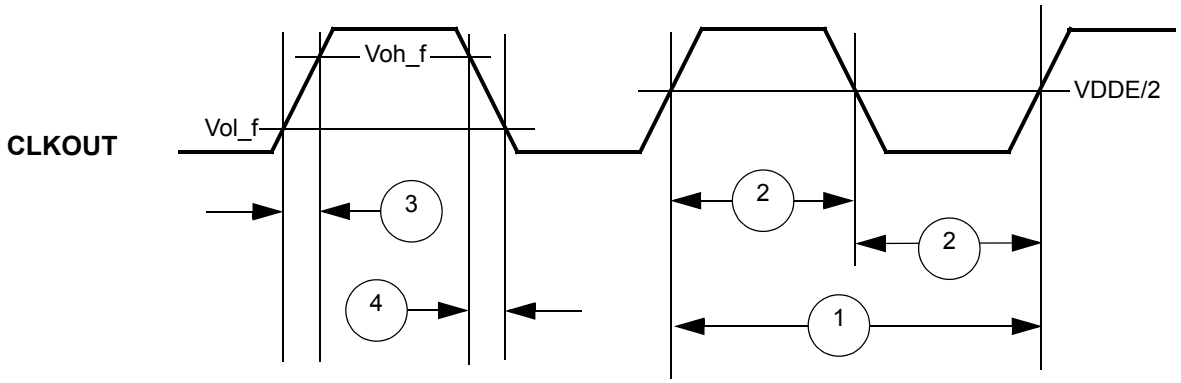

Figure 16. CLKOUT timing

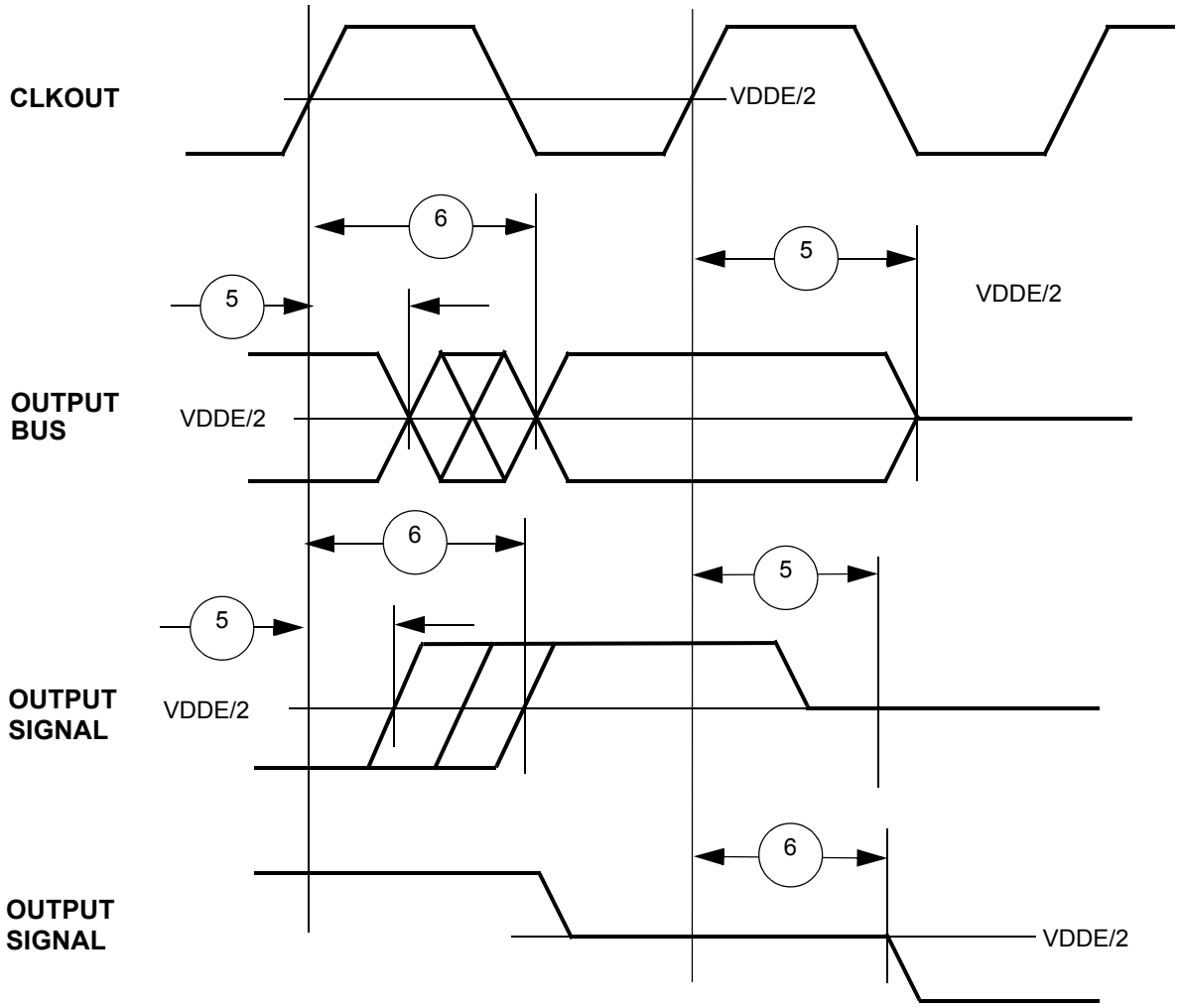

Figure 17. Synchronous output timing

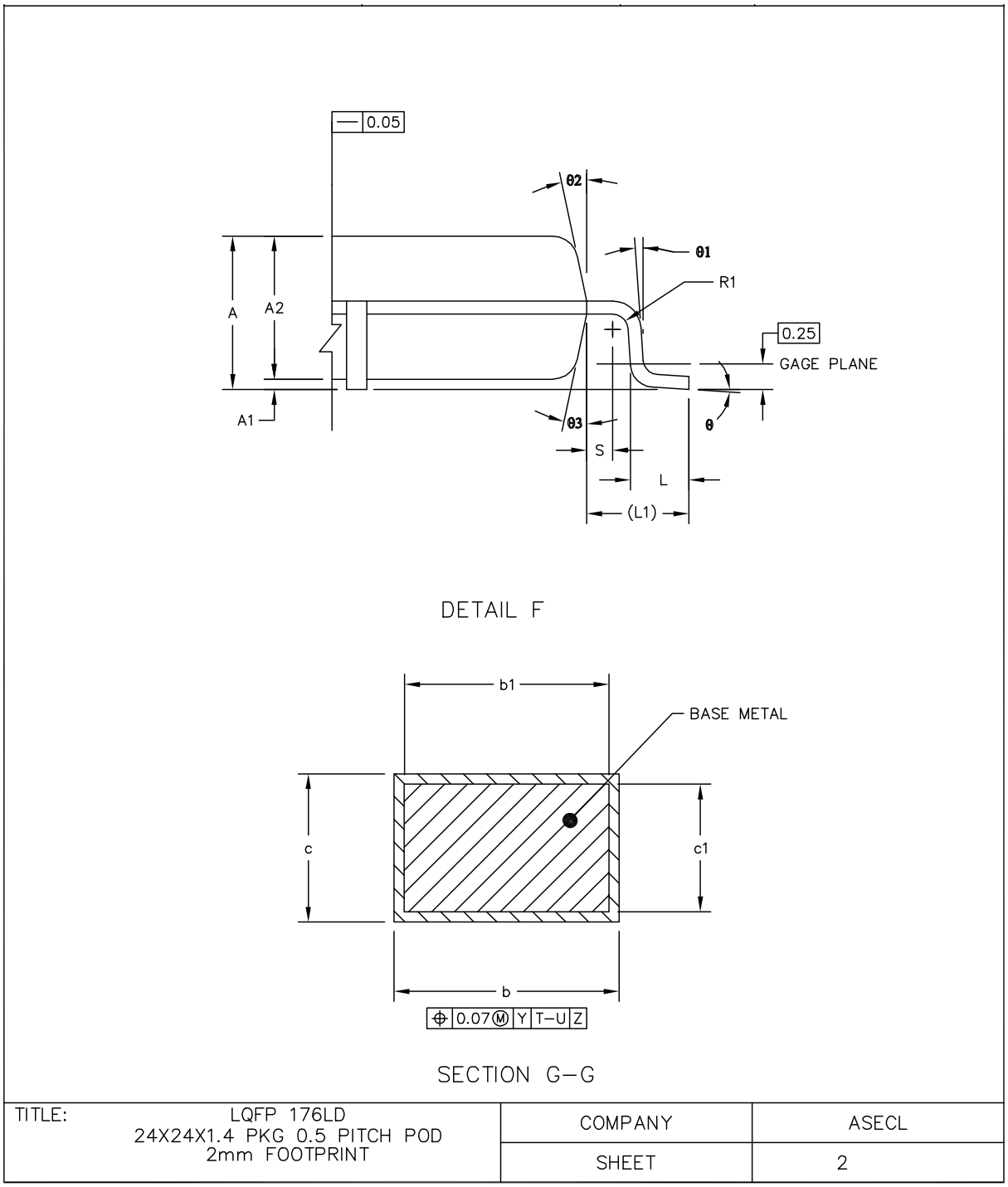

Figure 34. 176 LQFP package mechanical drawing (part 2)

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Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

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Freescale Semiconductor China Ltd.
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