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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5633mf2mlq60

MPC5634M_AD
Rev. 1.0, 01/2015

MPC5634M Microcontroller Datasheet Addendum

This addendum describes corrections to the *MPC5634M Microcontroller Datasheet*, order number MPC5634M. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/powerarchitecture for the latest updates.

The current version available of the *MPC5634M Microcontroller Datasheet* is Revision 9.

Table of Contents

freescale™ semiconductor

        - Allows selection of interrupt requests between external pins and DSPI
- Error correction status module (ECSM)
    - Configurable error-correcting codes (ECC) reporting
    - Single-bit error correction reporting
- On-chip flash memory
    - Up to 1.5 MB flash memory, accessed via a 64-bit wide bus interface
    - 16 KB shadow block
    - Fetch Accelerator
        - Provide single cycle flash access at 80 MHz
        - Quadruple 128-bit wide prefetch/burst buffers
        - Prefetch buffers can be configured to prefetch code or data or both
    - Censorship protection scheme to prevent flash content visibility
    - Flash divided into two independent arrays, allowing reading from one array while erasing/programming the other array (used for EEPROM emulation)
    - Memory block:
        - For MPC5634M: 18 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 10 × 128 KB)
        - For MPC5633M: 14 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 6 × 128 KB)
        - For MPC5632M: 12 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 4 × 128 KB)
    - Hardware programming state machine
- On-chip static RAM
    - For MPC5634M: 94 KB general purpose RAM of which 32 KB are on standby power supply
    - For MPC5633M: 64 KB general purpose RAM of which 32 KB are on standby power supply
    - For MPC5632M: 48 KB general purpose RAM of which 24 KB are on standby power supply
- Boot assist module (BAM)
    - Enables and manages the transition of MCU from reset to user code execution in the following configurations:
        - Execution from internal flash memory
        - Execution from external memory on the calibration bus
        - Download and execution of code via FlexCAN or eSCI
- Periodic interrupt timer (PIT)
    - 32-bit wide down counter with automatic reload
    - Four channels clocked by system clock
    - One channel clocked by crystal clock
    - Each channel can produce periodic software interrupt
    - Each channel can produce periodic triggers for eQADC queue triggering
    - One channel out of the five can be used as wake-up timer to wake device from low power stop mode
- System timer module (STM)
    - 32-bit up counter with 8-bit prescaler
    - Clocked from system clock
    - Four-channel timer compare hardware
    - Each channel can generate a unique interrupt request
    - Designed to address AUTOSAR task monitor function
- Software watchdog timer (SWT)
    - 32-bit timer
    - Clock by system clock or crystal clock
    - Can generate either system reset or non-maskable interrupt followed by system reset

1 Introduction

1.1 Document overview

This document provides an overview and describes the features of the MPC5634M series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. Electrical specifications and package mechanical drawings are included in this device data sheet. Pin assignments can be found in both the reference manual and data sheet.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices that contain all the features of the MPC5500 family and many new features coupled with high performance 90 nm CMOS technology to provide substantial reduction of cost per feature and significant performance improvement. The advanced and cost-efficient host processor core of this automotive controller family is built on Power Architecture® technology. This family contains enhancements that improve the architecture's fit in embedded applications, includes additional instruction support for digital signal processing (DSP), integrates technologies—such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system—that are important for today's lower-end powertrain applications. This device family is a completely compatible extension to Freescale's MPC5500 family. The device has a single level of memory hierarchy consisting of up to 94 KB on-chip SRAM and up to 1.5 MB of internal flash memory. The device also has an external bus interface (EBI) for 'calibration'. This external bus interface has been designed to support most of the standard memories used with the MPC5xx and MPC55xx families.

2 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5634M series of microcontroller units (MCUs). For functional characteristics, refer to the MPC5634M *Microcontroller Reference Manual.*

The MPC5634M series microcontrollers are system-on-chip devices that are built on Power Architecture® technology and:

- Are 100% user-mode compatible with the Power Architecture instruction set
- Contain enhancements that improve the architecture's fit in embedded applications
- Include additional instruction support for digital signal processing (DSP)
- Integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system

2.1 Device comparison

2.2 MPC5634M feature details

2.2.1 e200z335 core

The e200z335 processor utilizes a four stage pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), a 32×32 Hardware Multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated

- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - detects the quality of the crystal clock and cause interrupt request or system reset if error is detected
  - detects the quality of the PLL output clock. If an error is detected, causes a system reset or switches the system clock to the crystal clock and causes an interrupt request
- Programmable interrupt request or system reset on loss of lock

2.2.6 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the VertiCal connector in the calibration address space. The Calibration EBI is only available in the VertiCal Calibration System. The Calibration EBI includes a memory controller that generates interface signals to support a variety of external memories. The Calibration EBI memory controller supports legacy flash, SRAM, and asynchronous memories. In addition, the calibration EBI supports up to three regions via chip selects (two chip selects are multiplexed with two address bits), along with programmed region-specific attributes. The calibration EBI supports the following features:

- 22-bit address bus (two most significant signals multiplexed with two chip selects)
- 16-bit data bus
- Multiplexed mode with addresses and data signals present on the data lines

NOTE

The calibration EBI must be configured in multiplexed mode when the extended Nexus trace is used on the VertiCal Calibration System. This is because Nexus signals and address lines of the calibration bus share the same balls in the calibration package.

- Memory controller with support for various memory types:
  - Asynchronous/legacy flash and SRAM
  - Most standard memories used with the MPC5xx or MPC55xx family
- Bus monitor
  - User selectable
  - Programmable timeout period (with 8 external bus clock resolution)
- Configurable wait states (via chip selects)
- 3 chip-select (Cal_$\overline{CS}$[0], Cal_$\overline{CS}$[2:3]) signals (Multiplexed with 2 most significant address signals)
- 2 write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes
  - system frequency
  - 1/2 of system frequency
  - 1/4 of system frequency
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations)
- Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

2.2.18 System timers

The system timers provide two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

2.2.18.1 Periodic Interrupt Timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to be used to provide system ‘tick’ signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock, one is clocked by the crystal clock. This one channel is also referred to as Real Time Interrupt (RTI) and is used to wakeup the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered. Used to restart system clock after predefined timeout period
- Each channel can optionally generate an interrupt request or a trigger event (to trigger eQADC queues) when the timer reaches zero

2.2.18.2 System Timer Module (STM)

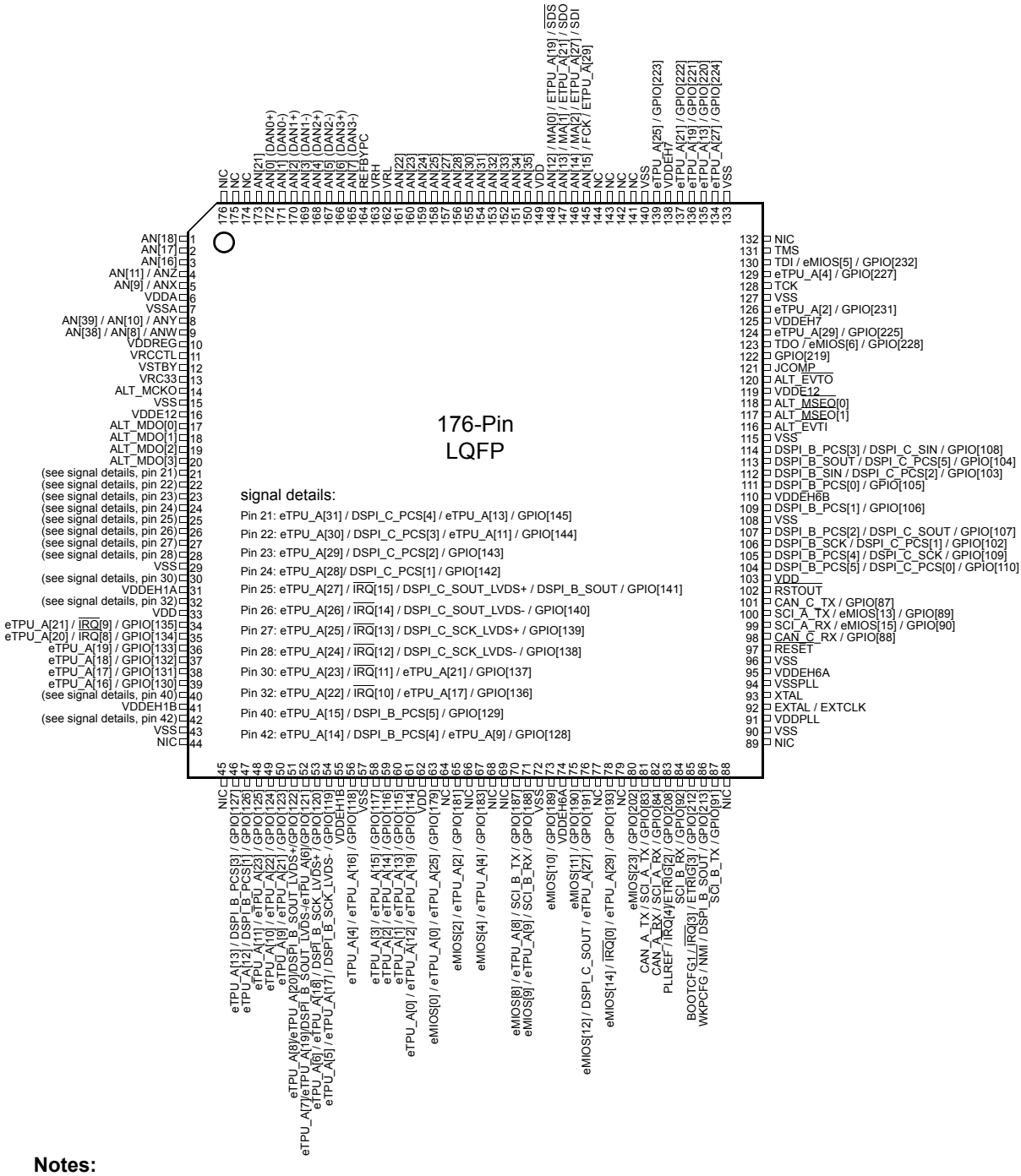
The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR (see http://www.autosar.org). It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels

3.3 176 LQFP pinout (MPC5633M)

Figure 4 shows the pinout for the 176-pin LQFP for the MPC5633M (1024 KB flash memory).



Notes:

1. Pins marked “NIC” have no internal connection.
2. Pins marked “NC” are not functional pins but may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.

Figure 4. 176-pin LQFP pinout (MPC5633M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI_B Periph Chip Select DSPI_C Periph Chip Select GPIO	PCR[110]	01 10 00	O O I/O	VDDEH6b Medium	– / Up	– / Up		87	104	J13
eQADC											
AN[0][27] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[0] / –		143	172	B5
AN[1][27] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[1] / –		142	171	A6
AN[2][27] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[2] / –		141	170	D6
AN[3][27] DAN1-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[3] / –		140	169	C7
AN[4][27] DAN2+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[4] / –		139	168	B6
AN[5][27] DAN2-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[5] / –		138	167	A7
AN[6][27] DAN3+	Single Ended Analog Input Positive Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[6] / –		137	166	D7
AN[7][27] DAN3-	Single Ended Analog Input Negative Terminal Diff. Input	—	—	I I	VDDA	I / –	AN[7] / –		136	165	C8
AN[8]	See AN[38]-AN[8]-ANW										
AN[9] ANX	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[9] / –		5	5	A2
AN[10]	See AN[39]-AN[10]-ANY										
AN[11] ANZ	Single Ended Analog Input External Multiplexed Analog Input	—	—	I I	VDDA	I / –	AN[11] / –		4	4	A3
AN[12] MA[0] ETPU_A[19] $\overline{SDS}$	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Strobe	PCR[215]	011 010 100 000	I O O O	VDDEH7	I / –	AN[12] / –		119	148	A12

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
AN[13] MA[1] ETPU_A[21] SDO	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Out	PCR[216]	011 010 100 000	I O O O	VDDEH7	I / –	AN[13] / –		118	147	B12
AN[14] MA[2] ETPU_A[27] SDI	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data In	PCR[217]	011 010 100 000	I O O I	VDDEH7	I / –	AN[14] / –		117	146	C12
AN[15] FCK ETPU_A[29]	Single Ended Analog Input eQADC Free Running Clock ETPU_A Ch.	PCR[218]	011 010 000	I O O	VDDEH7	I / –	AN[15] / –		116	145	C13
AN[16]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		3	3	C6
AN[17]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		2	2	C4
AN[18]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		1	1	D5
AN[21]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		144	173	B4
AN[22]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		132	161	B8
AN[23]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		131	160	C9
AN[24]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		130	159	D8
AN[25]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		129	158	B9
AN[27]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		128	157	A10
AN[28]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		127	156	B10
AN[30]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		126	155	D9
AN[31]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		125	154	D10
AN[32]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		124	153	C10
AN[33]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		123	152	C11
AN[34]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		122	151	C5
AN[35]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		121	150	D11
AN[36]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	174[7]	F4[8]
AN[37]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	175[7]	E3[8]

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
AN[38]-AN[8]-ANW	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[38] / –		9	9	B3
AN[39]-AN[10]-ANY	Single Ended Analog Input Multiplexed Analog Input	—	—	I	VDDA	I / –	AN[39] / –		8	8	D2
VRH	Voltage Reference High	—	—	I	VDDA	– / –	VRH		134	163	A8
VRL	Voltage Reference Low	—	—	I	VSSA0	– / –	VRL		133	162	A9
REFBYPC	Bypass Capacitor Input	—	—	I	VRL	– / –	REFBYPC		135	164	B7
eTPU2											
eTPU_A[0] eTPU_A[12] eTPU_A[19] GPIO[114]	eTPU_A Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[114]	011 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		52	61	L4, N3
eTPU_A[1] eTPU_A[13] GPIO[115]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[115]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		51	60	M3
eTPU_A[2] eTPU_A[14] GPIO[116]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[116]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		50	59	P2
eTPU_A[3] eTPU_A[15] GPIO[117]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[117]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		49	58	P1
eTPU_A[4] eTPU_A[16] GPIO[118]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[118]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		47	56	N2
eTPU_A[5] eTPU_A[17] DSPI_B_SCK_LVDS- GPIO[119]	eTPU_A Ch. eTPU_A Ch. DSPI_B CLOCK LVDS- GPIO	PCR[119]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		45	54	M4
eTPU_A[6] eTPU_A[18] DSPI_B_SCK_LVDS+ GPIO[120]	eTPU_A Ch. eTPU_A Ch. DSPI_B Clock LVDS+ GPIO	PCR[120]	001 010 100 000	I/O O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		44	53	L3

8 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

9 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

10 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

11 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

12 Total injection current for all analog input pins must not exceed 15 mA.

13 Lifetime operation at these specification limits is not guaranteed.

14 Solder profile per CDF-AEC-Q100.

15 Moisture sensitivity per JEDEC test method A112.

4.3 Thermal characteristics

Table 8. Thermal characteristics for 144-pin LQFP

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[1]	Single layer board – 1s	43	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board – 2s2p	35	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Single layer board –1s	34	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Four layer board – 2s2p	29	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[2]		22	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case (Top)[3]		8	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[4]		2	°C/W

1 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9. Thermal characteristics for 176-pin LQFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	@200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 10. Thermal characteristics for 208-pin MAPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2,3]	One layer board - 1s	39	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient natural convection[2,4]	Four layer board - 2s2p	24	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Single layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-ambient (@200 ft/min)[2,4]	Four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

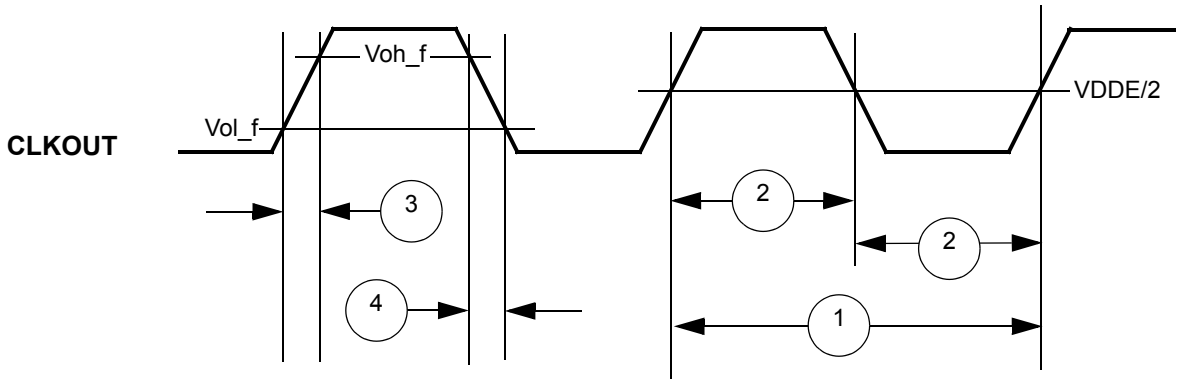


Figure 16. CLKOUT timing

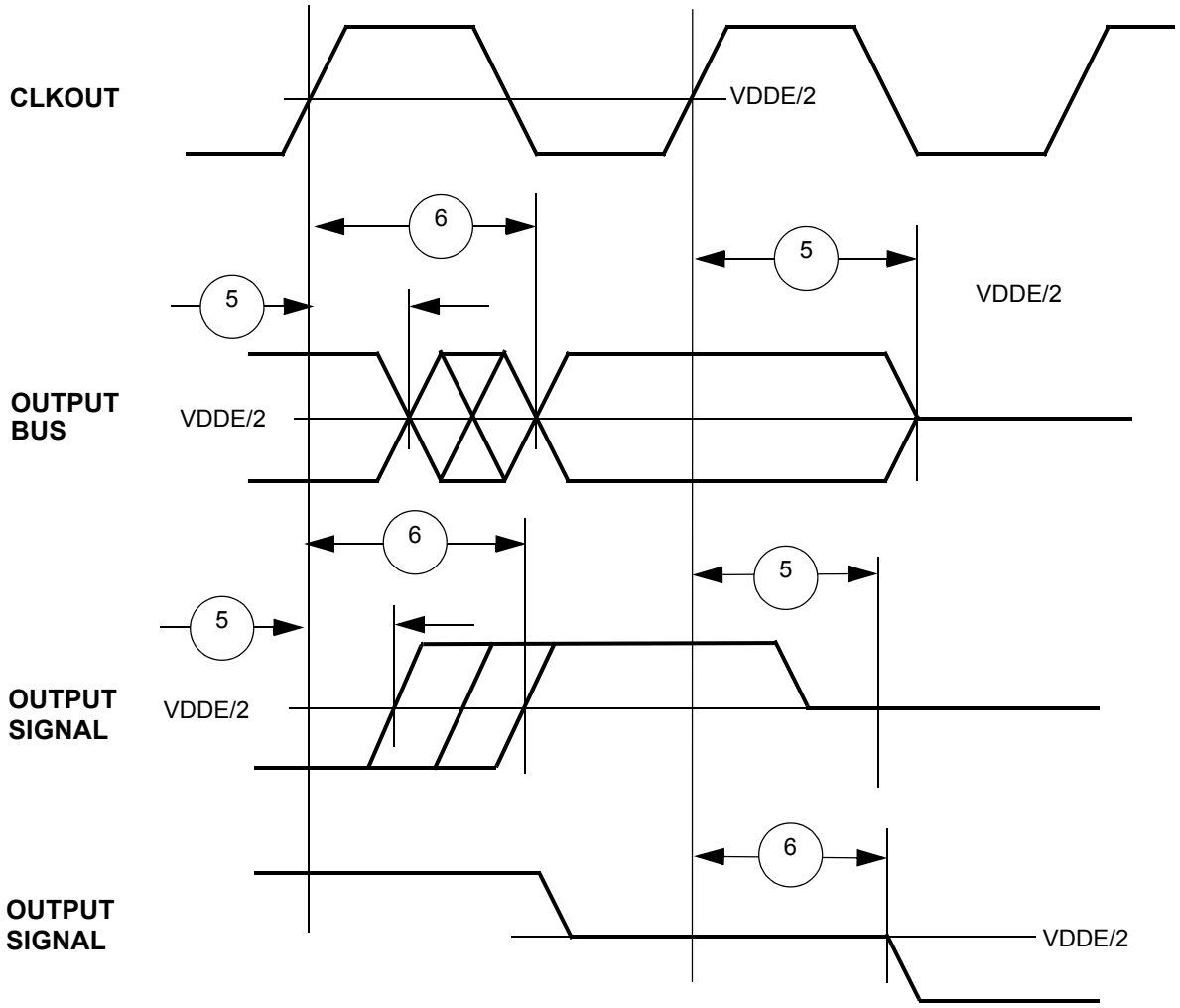


Figure 17. Synchronous output timing

Table 40. DSPI timing[1,2] (continued)

#	Symbol		C	Characteristic	40 MHz		60 MHz		80 MHz		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{HI}	CC	Data Hold Time for Inputs								
			D	Master (MTFE = 0)	–4	—	–4	—	–4	—	ns
			D	Slave	7	—	7	—	7	—	
			D	Master (MTFE = 1, CPHA = 0)[7]	45	—	25	—	21	—	
			D	Master (MTFE = 1, CPHA = 1)	–4	—	–4	—	–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)								
			D	Master (MTFE = 0)	—	6	—	6	—	6	ns
			D	Slave	—	25	—	25	—	25	
			D	Master (MTFE = 1, CPHA=0)	—	45	—	25	—	21	
			D	Master (MTFE = 1, CPHA=1)	—	6	—	6	—	6	
12	t_{HO}	CC	Data Hold Time for Outputs								
			D	Master (MTFE = 0)	–5	—	–5	—	–5	—	ns
			D	Slave	5.5	—	5.5	—	5.5	—	
			D	Master (MTFE = 1, CPHA = 0)	8	—	4	—	3	—	
			D	Master (MTFE = 1, CPHA = 1)	–5	—	–5	—	–5	—	

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at VDDEH = 3.0–5.25 V, TA = TL to TH, and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 62 MHz parts allow for a 60 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC5634M devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

4.16.6 eQADC SSI timing

Table 41. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency [2, 3]	1/17 f_{SYS_CLK}		1/2 f_{SYS_CLK}	Hertz
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2 t_{SYS_CLK}		17t_{SYS_CLK}	seconds
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} – 6.5		9* t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} – 6.5		8* t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		+7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		+7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

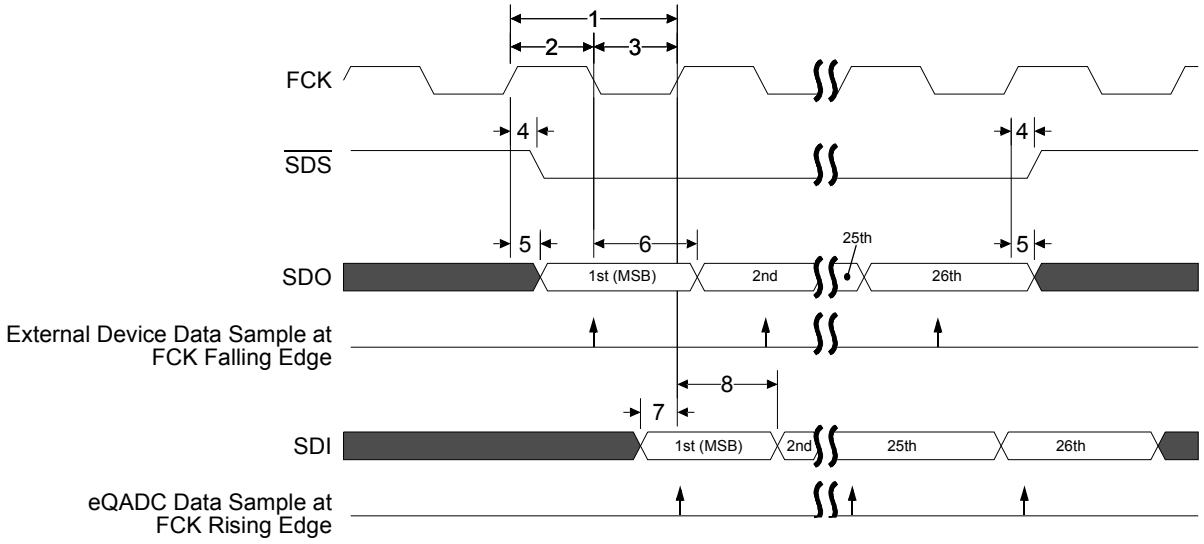


Figure 29. eQADC SSI timing

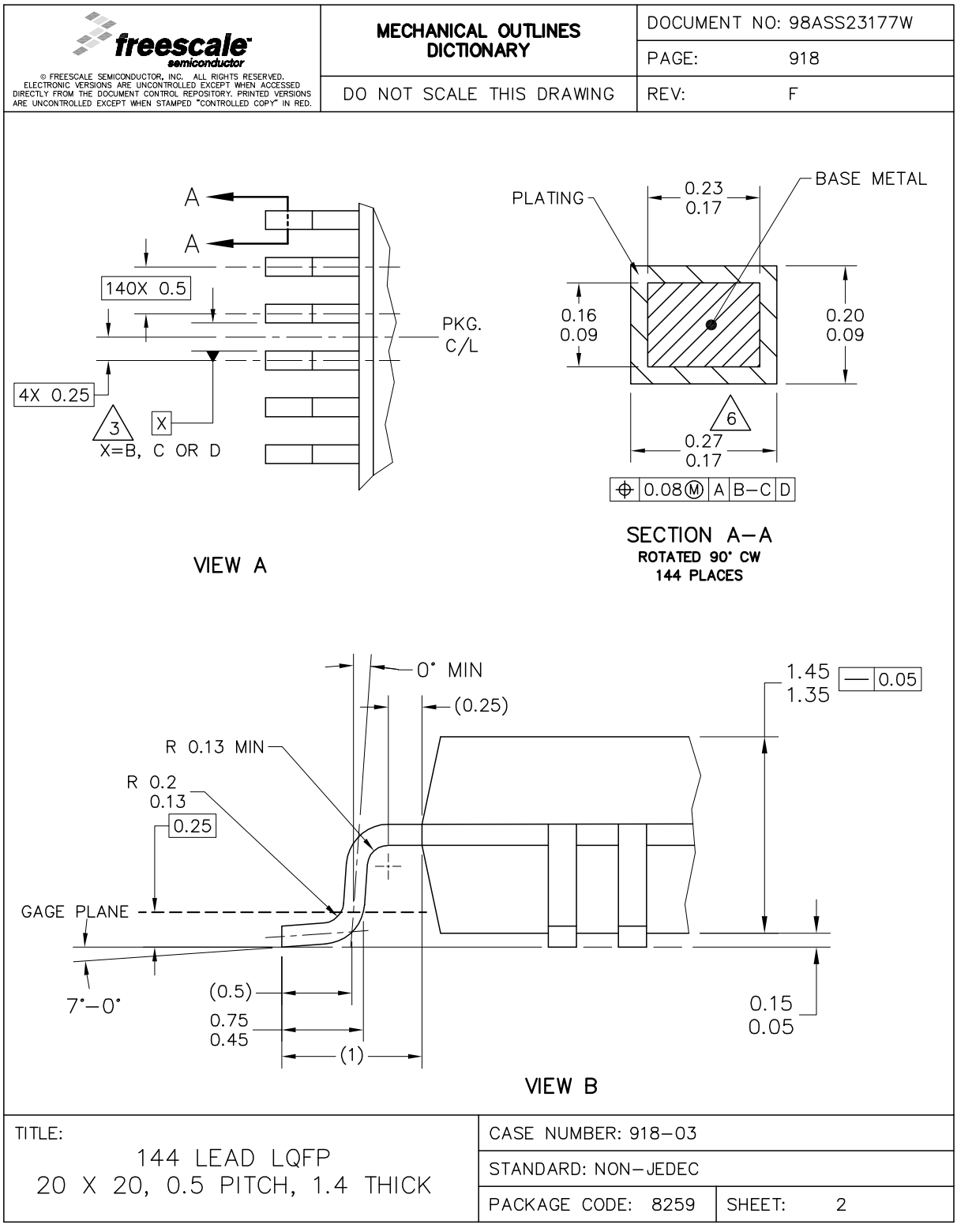


Figure 31. 144 LQFP package mechanical drawing (part 2)

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX
A	---		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		26 BSC	
D1		24 BSC	
e		0.5 BSC	
E		26 BSC	
E1		24 BSC	
L	0.45	0.6	0.75

DIM	MIN	NOM	MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S		0.2 REF	
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

DIM	MIN	NOM	MAX

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:	COMPANY	ASECL
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT	SHEET	3

Figure 35. 176 LQFP package mechanical drawing (part 3)

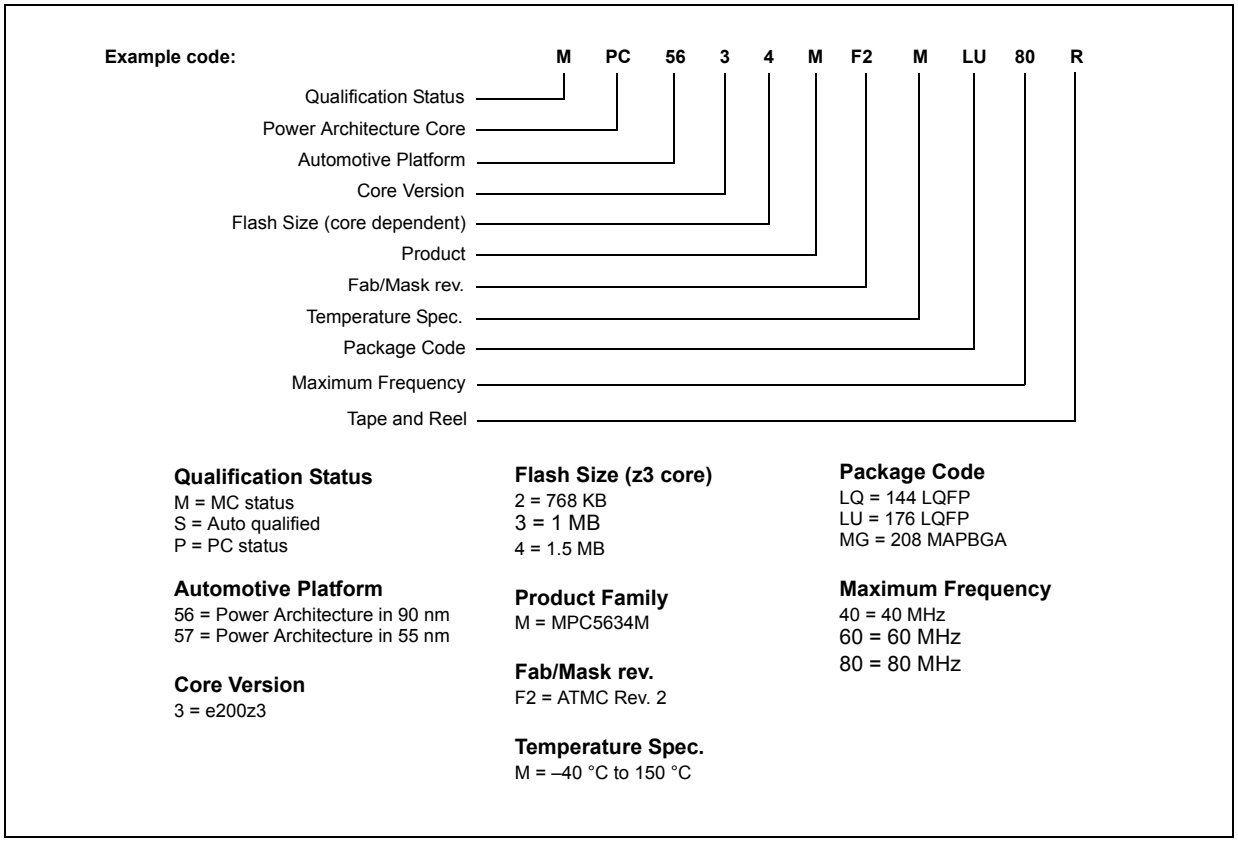


Figure 38. Commercial product code structure

7 Document revision history

Table 43 summarizes revisions to this document.

Table 43. Revision history

Revision	Date	Description of Changes
Rev. 1	4/2008	Initial release
Rev. 2	12/2008	• Maximum amount of flash increased from 1 MB to 1.5 MB. Flash memory type has changed. Rev. 1 and later devices use LC flash instead of FL flash. • Additional packages offered—now includes100 LQFP and 176 LQFP. Please note that the pinouts can vary for the same package depending on the amount of flash memory included in the device. • Device comparison table added. • Feature details section added • Signal summary table expanded. Now includes PCR register numbers and signal selection values and pin numbers for all production packages. • Electrical characteristics updated. • DSPI timing data added for 40 MHz and 60 MHz. • Thermal characteristics data updated. Data added for 100- and 176-pin packages. • DSPI LVDS pad specifications added.
Rev. 3	2/2009	Electrical characteristics updated • Flash memory electrical characteristics updated for LC flash • Power management control (PMC) and Power on Reset (POR) specifications updated • EMI characteristics data added • Maximum ratings updated • I/O pad current specifications updated • I/O Pad VRC33 current specifications added • Temperature sensor electrical characteristics added Pad type added to “Voltage” column of signal summary table Many signal names have changed to make them more understandable • DSPI: PCS_C[n] is now DSPI_C_PCS[n]; SOUT_C is now DSPI_C_SOUT, SIN_C is now DSPI_C_SIN, and SCK_C is now DSPI_C_SCK • CAN: CNTXB is now CAN_B_TX and CNRXB is now CAN_B_RC • SCI: RXDB is now SCI_B_RX and TXDB is now SCI_B_TX • In cases where multiple instances of the same IP block is incorporated into the device, e.g., 2 SCI blocks, the above nomenclature applies to all blocks “No connect” pins on pinouts clarified • Pins labelled “NIC” have no internal connection and should be tied to ground • Pins labelled “NC” are not functional pins but may be connected to internal circuits They are to be left floating Some of the longer multiplexed signal names appearing on pinouts have been moved to the inside of the package body to avoid having to use smaller fonts Orderable parts table updated Part number decoder added

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5	04/2010	Updates to features list: • MMU is 16-entry (previously noted as 8-entry) • ECSM features include single-bit error correction reporting • eTPU2 is object code compatible with previous eTPU versions Updates to feature details: • Programming feature: eTPU2 channel flags can be tested Pinout/ballmap changes: 144 pin LQFP package: • Pin 46 is now VDDEH1B (was VDDEH4A) • Pin 61 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 208 ball BGA package (all devices) Ball N9 changed to VDDEH1/6 (was VDDEH6). In a future revision of the device this may be changed to NC (no connect). Changes to calibration ball names on devices with 1 MB flash memory: • CAL_MDO0 changed to ALT_MDO0 • CAL_MDO1 changed to ALT_MDO1 • CAL_MDO2 changed to ALT_MDO2 • CAL_MDO3 changed to ALT_MDO3 • CAL_MSEO0 changed to ALT_MSEO0 • CAL_MSEO1 changed to ALT_MSEO1 • CAL_EVTI changed to ALT_EVTI • CAL_EVTO changed to ALT_EVTO • CAL_MCKO changed to ALT_MCKO Power/ground segment changes: • The following pins are on VDDE7 I/O segment only on the 208-ball BGA package: ALT_MDO[0:3], ALT_MSEO[0:1], ALT_EVTI, ALT_EVTO, ALT_MCKO. • Power segments VDDEH4, VDDEH4A and VDDEH4B have been removed. CLKOUT power segment is VDDE5 (was VDDE12) Thermal characteristics for 176-pin LQFP updated (all parameter values)

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