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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5633mf2mlq60r

1 Addendum List for Revision 9

Table 1. MPC5634M Rev 9 Addendum

Location	Description
Section 4.11, “Temperature Sensor Electrical Characteristics”, Page 81	In “Temperature Sensor Electrical Characteristics” table, update the Min and Max value of “Accuracy” parameter to -20^{o}C and +20^{o}C, respectively.

2 Revision History

Table 2 provides a revision history for this datasheet addendum document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release.	12/2014

- Four pairs of differential analog input channels
- Full duplex synchronous serial interface to an external device
  - Has a free-running clock for use by the external device
  - Supports a 26-bit message length
  - Transmits a null message when there are no triggered CFIFOs with commands bound for external CBuffers, or when there are triggered CFIFOs with commands bound for external CBuffers but the external CBuffers are full
- Parallel Side Interface to communicate with an on-chip companion module
- Zero jitter triggering for queue 0. (Queue 0 trigger causes current conversion to be aborted and the queued conversions in the CBUFFER to be bypassed. Delay from Trigger to start of conversion is 13 system clocks + 1 ADC clock.)
- eQADC Result Streaming. Generation of a continuous stream of ADC conversion results from a single eQADC command word. Controlled by two different trigger signals; one to define the rate at which results are generated and the other to define the beginning and ending of the stream. Used to digitize waveforms during specific time/angle windows, e.g., engine knock sensor sampling.
- Angular Decimation. The ability of the eQADC to sample an analog waveform in the time domain, perform Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filtering also in the time domain, but to down sample the results in the angle domain. Resulting in a time domain filtered result at a given engine angle.
- Priority Based CFIFOs
  - Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.
  - Supports software and several hardware trigger modes to arm a particular CFIFO
  - Generates interrupt when command coherency is not achieved
- External Hardware Triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Supports four external 8-to-1 muxes which can expand the input channel number from 34[1] to 59

- Two deserial serial peripheral interface modules (DSPI)
  - SPI
    - Full duplex communication ports with interrupt and DMA request support
    - Supports all functional modes from QSPI subblock of QSMCM (MPC5xx family)
    - Support for queues in RAM
    - 6 chip selects, expandable to 64 with external demultiplexers
    - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
    - Modified SPI mode for interfacing to peripherals with longer setup time requirements
    - LVDS option for output clock and data to allow higher speed communication
  - Deserial serial interface (DSI)
    - Pin reduction by hardware serialization and deserialization of eTPU, eMIOS channels and GPIO
    - 32 bits per DSPI module
    - Triggered transfer control and change in data transfer control (for reduced EMI)
    - Compatible with Microsecond Channel Version 1.0 downstream
- Two enhanced serial communication interface (eSCI) modules
  - UART mode provides NRZ format and half or full duplex interface
  - eSCI bit rate up to 1 Mbps

1. 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32.
1. 176-pin and 208-ball packages.

- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8, 9, 12 or 13 bits
- Separately enabled transmitter and receiver
- LIN support
- DMA support
- Interrupt request support
- Programmable clock source: system clock or oscillator clock
- Support Microsecond Channel (Timed Serial Bus - TSB) upstream Version 1.0

- Two FlexCAN
  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    - Run-time access of entire memory map
    - Calibration
  - Support for data value breakpoints / watchpoints
    - Run-time access of entire memory map
    - Calibration

      Table constants calibrated using MMU and internal and external RAM

      Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation
  - On-chip regulator 5 V to 3.3 V for internal supplies
  - On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic
- Low-power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

1 Introduction

1.1 Document overview

This document provides an overview and describes the features of the MPC5634M series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. Electrical specifications and package mechanical drawings are included in this device data sheet. Pin assignments can be found in both the reference manual and data sheet.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices that contain all the features of the MPC5500 family and many new features coupled with high performance 90 nm CMOS technology to provide substantial reduction of cost per feature and significant performance improvement. The advanced and cost-efficient host processor core of this automotive controller family is built on Power Architecture® technology. This family contains enhancements that improve the architecture's fit in embedded applications, includes additional instruction support for digital signal processing (DSP), integrates technologies—such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system—that are important for today's lower-end powertrain applications. This device family is a completely compatible extension to Freescale's MPC5500 family. The device has a single level of memory hierarchy consisting of up to 94 KB on-chip SRAM and up to 1.5 MB of internal flash memory. The device also has an external bus interface (EBI) for 'calibration'. This external bus interface has been designed to support most of the standard memories used with the MPC5xx and MPC55xx families.

2 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5634M series of microcontroller units (MCUs). For functional characteristics, refer to the MPC5634M *Microcontroller Reference Manual.*

The MPC5634M series microcontrollers are system-on-chip devices that are built on Power Architecture® technology and:

- Are 100% user-mode compatible with the Power Architecture instruction set
- Contain enhancements that improve the architecture's fit in embedded applications
- Include additional instruction support for digital signal processing (DSP)
- Integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system

2.1 Device comparison

2.2 MPC5634M feature details

2.2.1 e200z335 core

The e200z335 processor utilizes a four stage pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), a 32×32 Hardware Multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated

Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six instructions.

Branches can also be decoded at the instruction buffer and branch target addresses calculated prior to the branch reaching the instruction decode stage, allowing the branch target to be prefetched early. When a branch is detected at the instruction buffer, a prediction may be made on whether the branch is taken or not. If the branch is predicted to be taken, a target fetch is initiated and its target instructions are placed in the instruction buffer following the branch instruction. Many branches take zero cycle to execute by using branch folding. Branches are folded out from the instruction execution pipe whenever possible. These include unconditional branches and conditional branches with condition codes that can be resolved early.

Conditional branches which are not taken and not folded execute in a single clock. Branches with successful target prefetching which are not folded have an effective execution time of one clock. All other taken branches have an execution time of two clocks. Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching. Vectored and autovectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The hardware floating-point unit utilizes the IEEE-754 single-precision floating-point format and supports single-precision floating-point operations in a pipelined fashion. The general purpose register file is used for source and destination operands, thus there is a unified storage model for single-precision floating-point data types of 32 bits and the normal integer type. Single-cycle floating-point add, subtract, multiply, compare, and conversion operations are provided. Divide instructions are multi-cycle and are not pipelined.

The Signal Processing Extension (SPE) Auxiliary Processing Unit (APU) provides hardware SIMD operations and supports a full complement of dual integer arithmetic operation including Multiply Accumulate (MAC) and dual integer multiply (MUL) in a pipelined fashion. The general purpose register file is enhanced such that all 32 of the GPRs are extended to 64 bits wide and are used for source and destination operands, thus there is a unified storage model for 32×32 MAC operations which generate greater than 32-bit results.

The majority of both scalar and vector operations (including MAC and MUL) are executed in a single clock cycle. Both scalar and vector divides take multiple clocks. The SPE APU also provides extended load and store operations to support the transfer of data to and from the extended 64-bit GPRs. This SPE APU is fully binary compatible with e200z6 SPE APU used in MPC5554 and MPC5553.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements. This enables the classic Power Architecture instruction set to be represented by a modified instruction set made up from a mixture of 16- and 32-bit instructions. This results in a significantly smaller code size footprint without noticeably affecting performance. The Power Architecture instruction set and VLE instruction set are available concurrently. Regions of the memory map are designated as PPC or VLE using an additional configuration bit in each of Table Look-aside Buffers (TLB) entries in the MMU.

The CPU core is enhanced by the addition of two additional interrupt sources; Non-Maskable Interrupt and Critical Interrupt. These two sources are routed directly from package pins, via edge detection logic in the SIU to the CPU, bypassing completely the Interrupt Controller. Once the edge detection logic is programmed, it cannot be disabled, except by reset. The non-maskable Interrupt is, as the name suggests, completely un-maskable and when asserted will always result in the immediate execution of the respective interrupt service routine. The non-maskable interrupt is not guaranteed to be recoverable. The Critical Interrupt is very similar to the non-maskable interrupt, but it can be masked by other exceptional interrupts in the CPU and is guaranteed to be recoverable (code execution may be resumed from where it stopped).

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash with the CPU to provide single cycle random access to the flash up to 80 MHz system clock speed
  - Configurable read buffering and line prefetch support
  - Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller is pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 64 bits (two words)
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

2.2.10 SRAM

The MPC5634M SRAM module provides a general-purpose up to 94 KB memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB or 24 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 32-bit data element

2.2.11 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by Freescale and is identical for all MPC5634M MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on calibration bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the MPC5634M hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation

- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using Freescale protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the software watchdog timer

2.2.12 eMIOS

The eMIOS (Enhanced Modular Input Output System) module provides the functionality to generate or measure time events. The channels on this module provide a range of operating modes including the capability to perform dual input capture or dual output compare as well as PWM output.

The eMIOS provides the following features:

- 16 channels (24-bit timer resolution)
- For compatibility with other family members selected channels and timebases are implemented:
  - Channels 0 to 6, 8 to 15, and 23
  - Timebases A, B and C
- Channels 1, 3, 5 and 6 support modes:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
- Channels 2, 4, 11 and 13 support all the modes above plus:
  - Output Pulse Width Modulation Buffered (OPWMB)
- Channels 0, 8, 9, 10, 12, 14, 15, 23 support all the modes above plus:
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (set flag on both matches) (DAOC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width and Frequency Modulation Buffered (OPWFMB)
- Three 24-bit wide counter buses
  - Counter bus A can be driven by channel 23 or by the eTPU2 and all channels can use it as a reference
  - Counter bus B is driven by channel 0 and channels 0 to 6 can use it as a reference
  - Counter bus C is driven by channel 8 and channels 8 to 15 can use it as a reference
- Shared time bases with the eTPU2 through the counter buses
- Synchronization among internal and external time bases

2.2.13 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host

  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Streaming mode operation of Queue_0 to execute some commands several times
  - Supports software and hardware trigger modes to arm a particular Queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Supports four external 8-to-1 muxes which can expand the input channels to 56 channels total

2.2.15 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MPC5634M MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that supports the Microsecond Channel protocol. There are two identical DSPI blocks on the MPC5634M MCU. The DSPI output pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) according to the Microsecond Channel specification.

The DSPIs have three configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as an up to 16-bit SPI with support for queues
- Enhanced deserial serial interface (DSI) configuration where DSPI serializes up to 32 bits with three possible sources per bit
  - eTPU, eMIOS, new virtual GPIO registers as possible bit source
  - Programmable inter-frame gap in continuous mode
  - Bit source selection allows microsecond channel downstream with command or data frames up to 32 bits
  - Microsecond channel dual receiver mode
- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software.

The DSPI supports these SPI features:

- Full-duplex, synchronous transfers
- Selectable LVDS Pads working at 40 MHz for SOUT and SCK pins
- Master and Slave Mode
- Buffered transmit operation using the TX FIFO with parameterized depth of 4 entries
- Buffered receive operation using the RX FIFO with parameterized depth of 4 entries
- TX and RX FIFOs can be disabled individually for low-latency updates to SPI queues
- Visibility into the TX and RX FIFOs for ease of debugging
- FIFO Bypass Mode for low-latency updates to SPI queues
- Programmable transfer attributes on a per-frame basis:
  - Parameterized number of transfer attribute registers (from two to eight)
  - Serial clock with programmable polarity and phase
  - Various programmable delays:
    - PCS to SCK delay

3.4 208 MAPBGA ballmap (MPC5634M)

Figure 5 shows the 208-pin MAPBGA ballmap for the MPC5634M (1536 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12- $\overline{SDS}$	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	$\overline{ALT\_MSEO0}$	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_$\overline{EVTO}$	NIC[1]
E	ETPUA30	ETPUA31	AN37	VDD									VDDE7	TDI	ALT_$\overline{EVTI}$	$\overline{ALT\_MSEO1}$
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO99	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	GPIO98	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	$\overline{RSTOUT}$	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	$\overline{RESET}$
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[2]	EMIOS12	eTPU_A19[3]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	GPIO207	VDDE7	NIC[1]	EMIOS8	eTPU_A29[3]	eTPU_A2[3]	eTPU_A21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	GPIO206	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPU_A27[3]	EMIOS23	CAN_A_ RX	NIC[1]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	EMIOS1	GPIO219	eTPU_A25[3]	EMIOS13	EMIOS15	eTPU_A4[3]	eTPU_A13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 This ball may be changed to “NC” (no connection) in a future revision.
3 eTPU output only channel.

Figure 5. 208-pin MAPBGA ballmap (MPC5634M; top view)

3.5 208 MAPBGA ballmap (MPC5633M only)

Figure 6 shows the 208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	ALT_ MSEO0	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_EVTO	NIC[1]
E	ETPUA30	ETPUA31	NC[2]	VDD									VDDE7	TDI	ALT_ EVTI	ALT_ MSEO1
F	ETPUA28	ETPUA29	ETPUA26	NC[2]									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			NC[2]	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	NC[2]	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	RSTOUT	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	RESET
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[3]	EMIOS12	eTPUA19[4]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	NC[2]	VDDE7	NIC[1]	EMIOS8	eTPUA29[3]	eTPUA2[3]	eTPUA21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	NC[2]	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPUA27[3]	EMIOS23	CAN_A_ RX	NC[2]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	NC[2]	GPIO219	eTPUA25[3]	NC[2]	NC[2]	eTPUA4[3]	eTPUA13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 Pins marked “NC” may be connected to internal circuitry. Connections to external circuits or other pins on this device can result in unpredictable system behavior or damage.
3 This ball may be changed to “NC” (no connection) in a future revision.
4 eTPU output only channel.

Figure 6. 208-pin MAPBGA ballmap (MPC5633M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
VSTBY	Power Supply for Standby RAM	—	—	I	VSTBY	I / –	—		12	12	C1
VRC33	3.3V Voltage Regulator Bypass Capacitor	—	—	O	VRC33	O / –	—		13	13	A15, D1, N6, N12
VRCCTL	Voltage Regulator Control Output	—	—	O	NA	O / –	—		11	11	N14
VDDA[34]	Analog Power Input for eQADC	—	—	I	VDDA (5.0 V)	I / –	—		6	6	—
VDDA0	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	B11
VSSA0	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A11
VDDA1	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	A4
VSSA1	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A5
VSSA[35]	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		7	7	—
VDDREG	Voltage Regulator Supply	—	—	I	VDDREG (5.0 V)	I / –	—		10	10	K16
VDD	Internal Logic Supply Input	—	—	I	VDD (1.2 V)	I / –	—		26, 53, 86, 120	33, 62, 103, 149	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15

Table 5. MPC563x Power/Ground Segmentation (continued)

Power Segment		144-LQFP Pin Number	176-LQFP Pin Number	208-BGA Pin Number	Voltage Range[1]	I/O Pins Powered by Segment
VDDEH6 (a,b)		78, 93	95, 110	F13	3.3 V – 5.0 V	RESET, RSTOUT, WKPCFG, BOOTCFG1, PLLREF, SCK_B, PCKCFG[0], CAN_A_TX, CAN_A_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_B_RX, SCK_B, SIN_B, SOUT_B, DSPI_B_PCS_B[0:5], eMIOS[4], eMIOS[8:15], eMIOS[23], XTAL, EXTAL
VDDEH7[2]		102, 113	125, 138	D12	3.3 V – 5.0 V	PCKCFG[1], MDO[0:3], EVTI, EVTO, MCKO, MSEO[0:1], TDO, TDI, TMS, TCK, JCOMP, AN[12:15] (GPIO[98:99], GPIO[206:207])
VDDE12[3] VDDE7		—	16, 119	E13, P6	1.8 V – 3.3 V	CAL_ADDR[12:30], CAL_DATA[0:15], CAL_CS[0], CAL_CS[2:3], CAL_RD_WR, CAL_WE[0:1], CAL_OE, CAL_TS, ALT_MCKO, ALT_EVTO, NEXUSCFG

1 These are nominal voltages. All VDDE and VDDEH voltages are –5%, +10% (VDDE 1.62 V to 3.6 V, VDDEH 3.0 V to 5.5 V). VDDA is +5%, –10%.

2 The VDDEH7 segment may be powered from 3.0 V to 5.0 V for mux address or SSI functions, but must meet the VDDA specifications of 4.5 V to 5.25 V for analog input function.

3 In the calibration package this signal is named VDDE12; it is named VDDE7 in all other packages.

4 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5634M series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.1 Parameter classification

The electrical parameters shown in this document are guaranteed by various methods. To provide a better understanding, the classifications listed in Table 6 are used and the parameters are tagged accordingly in the tables. Note that only controller characteristics (“CC”) are classified. System requirements (“SR”) are operating conditions that must be provided to ensure normal device operation.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.2 Maximum ratings

Table 7. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DD}	SR	1.2 V core supply voltage[2]		– 0.3	1.32	V
V_{FLASH}	SR	Flash core voltage[3]		– 0.3	5.5	V
V_{STBY}	SR	SRAM standby voltage[4]		– 0.3	5.5	V
V_{DDPLL}	SR	Clock synthesizer voltage		– 0.3	1.32	V
V_{RC33}[5]	SR	Voltage regulator control input voltage		– 0.3	3.6	V

4.6 Power Management Control (PMC) and Power On Reset (POR) electrical specifications

Table 13. PMC Operating conditions and external regulators supply voltage

ID	Name		C	Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage VDDREG	4.75[1]	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V VDD when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)[2]	1.26[3]	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V VDD when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum DC output current[4]	400	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)[5]	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1 During start up operation the minimum required voltage to come out of reset state is 4.6 V.

2 An internal regulator controller can be used to regulate core supply.

3 The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.

4 The onchip regulator can support a minimum of 400 ma although the worst case core current is 180 ma.

5 An internal regulator can be used to regulate 3.3 V supply.

Table 14. PMC electrical characteristics

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
1	Vbg	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	Vbg–7%	Vbg	Vbg+6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)[1]	Vbg–10mV	Vbg	Vbg+10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
I_{DDH1} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[23] supplies @ 80 MHz	V_{DDEH1}	—	—	See note [23]	mA
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[24]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.25 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[24]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[25]	—	–2.5	—	2.5	µA
I_{IC}	CC	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	CC	P	Analog input current, channel off, AN[0:7], AN38, AN39[26]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins (ANx)[26]	—	–150	—	150	

Table 29. eQADC conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
TUE8	CC	C	Total unadjusted error (TUE) at 8 MHz[9]		–4	4	Counts
TUE16	CC	C	Total unadjusted error at 16 MHz[10]		–8	8	Counts
SNR	CC	T	Signal to Noise Ratio[11]		55.2		dB
THD	CC	T	Total Harmonic Distorsion		70.0		dB
SFDR	CC	T	Spurious Free Dynamic Range		65.0		dB
SINAD	CC	T	Signal to Noise and Distorsion		55.0		dB
ENOB	CC	T	Effective Number of Bits		8.8		Counts
GAINVGA1	CC	–	Variable gain amplifier accuracy (gain=1)[12]				
	CC	C	INL	8 MHz ADC	–4	4	Counts[13]
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3[14]	3[14]	Counts
	CC	C		16 MHz ADC	–3[14]	3[14]	Counts
GAINVGA2	CC	–	Variable gain amplifier accuracy (gain=2)[12]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4	CC	–	Variable gain amplifier accuracy (gain=4)[12]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)	PREGAIN set to 1X setting	–	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	–	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	–	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[15]		(VRH - VRL)/2 - 5%	(VRH - VRL)/2 + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV. Without using pregain.

3 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.

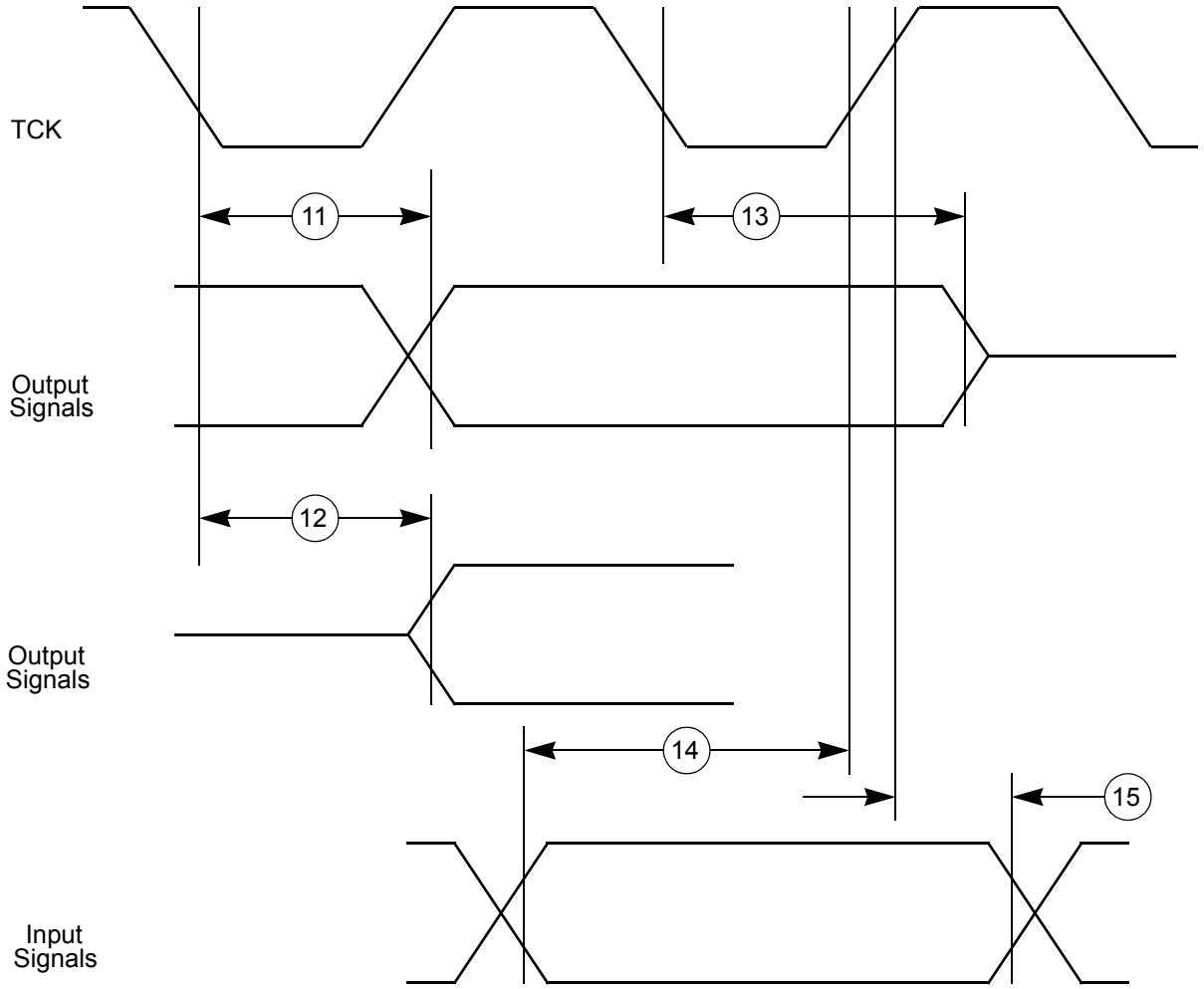
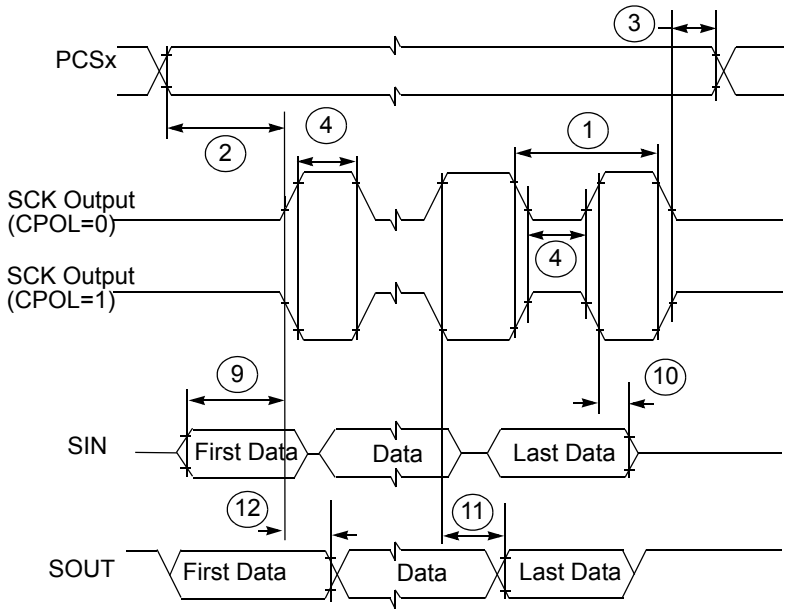


Figure 12. JTAG boundary scan timing

4.16.2 Nexus timing

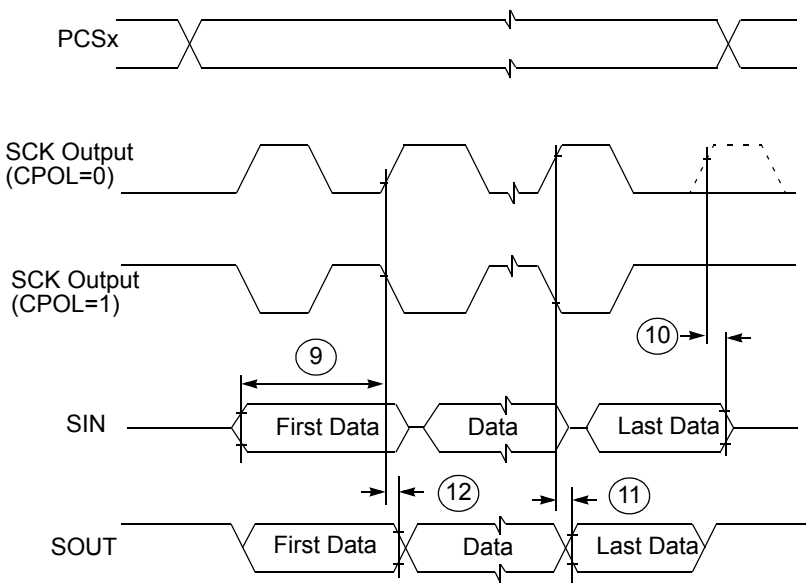
Table 37. Nexus debug port timing[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MCYC}	CC	D	MCKO Cycle Time	$2^{2,3}$	8	t_{CYC}
1a	t_{MCYC}	CC	D	Absolute Minimum MCKO Cycle Time	100[4]	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid[5]	– 0.1	0.2	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[5]	0.1	0.2	t_{MCYC}
6	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[5]	– 0.1	0.2	t_{MCYC}
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}
8	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ Pulse Width	1	—	t_{MCYC}



These numbers reference Table 40.

Figure 24. DSPI modified transfer format timing – master, CPHA = 0



These numbers reference Table 40.

Figure 25. DSPI modified transfer format timing – master, CPHA = 1

6 Ordering information

Table 42 shows the orderable part numbers for the MPC5634M series.

Table 42. Orderable part number summary

Part Number	Flash/SRAM (Kbytes)	Package	Speed (MHz)
SPC5632MF2MLQ60	768 / 48	144 LQFP Pb-free	60
SPC5632MF2MLQ40	768 / 48	144 LQFP Pb-free	40
SPC5633MF2MMG80	1024 / 64	208 MAPBGA Pb-free	80
SPC5633MF2MLU80	1024 / 64	176 LQFP Pb-free	80
SPC5633MF2MLQ80	1024 / 64	144 LQFP Pb-free	80
SPC5633MF2MMG60	1024 / 64	208 MAPBGA Pb-free	60
SPC5633MF2MLU60	1024 / 64	176 LQFP Pb-free	60
SPC5633MF2MLQ60	1024 / 64	144 LQFP Pb-free	60
SPC5633MF2MLQ40	1024 / 64	144 LQFP Pb-free	40
SPC5634MF2MMG80	1536 / 94	208 MAPBGA Pb-free	80
SPC5634MF2MLU80	1536 / 94	176 LQFP Pb-free	80
SPC5634MF2MLQ80	1536 / 94	144 LQFP Pb-free	80
SPC5634MF2MMG60	1536 / 94	208 MAPBGA Pb-free	60
SPC5634MF2MLU60	1536 / 94	176 LQFP Pb-free	60
SPC5634MF2MLQ60	1536 / 94	144 LQFP Pb-free	60
SPC563M60L3CPBY			
SPC563M60L3CPAY			

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev. 5	04/2010	Updates to features list: • MMU is 16-entry (previously noted as 8-entry) • ECSM features include single-bit error correction reporting • eTPU2 is object code compatible with previous eTPU versions Updates to feature details: • Programming feature: eTPU2 channel flags can be tested Pinout/ballmap changes: 144 pin LQFP package: • Pin 46 is now VDDEH1B (was VDDEH4A) • Pin 61 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 176 pin LQFP package (1.5M devices) • Pin 55 is now VDDEH1B (was VDDEH4A) • Pin 74 is now VDDEH6A (was VDDEH4B) 208 ball BGA package (all devices) Ball N9 changed to VDDEH1/6 (was VDDEH6). In a future revision of the device this may be changed to NC (no connect). Changes to calibration ball names on devices with 1 MB flash memory: • CAL_MDO0 changed to ALT_MDO0 • CAL_MDO1 changed to ALT_MDO1 • CAL_MDO2 changed to ALT_MDO2 • CAL_MDO3 changed to ALT_MDO3 • CAL_MSEO0 changed to ALT_MSEO0 • CAL_MSEO1 changed to ALT_MSEO1 • CAL_EVTI changed to ALT_EVTI • CAL_EVTO changed to ALT_EVTO • CAL_MCKO changed to ALT_MCKO Power/ground segment changes: • The following pins are on VDDE7 I/O segment only on the 208-ball BGA package: ALT_MDO[0:3], ALT_MSEO[0:1], ALT_EVTI, ALT_EVTO, ALT_MCKO. • Power segments VDDEH4, VDDEH4A and VDDEH4B have been removed. CLKOUT power segment is VDDE5 (was VDDE12) Thermal characteristics for 176-pin LQFP updated (all parameter values)