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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5633mf2mlu60

1 Addendum List for Revision 9

Table 1. MPC5634M Rev 9 Addendum

Location	Description
Section 4.11, “Temperature Sensor Electrical Characteristics”, Page 81	In “Temperature Sensor Electrical Characteristics” table, update the Min and Max value of “Accuracy” parameter to -20^{o}C and +20^{o}C, respectively.

2 Revision History

Table 2 provides a revision history for this datasheet addendum document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release.	12/2014

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Document Number: MPC5634M_AD
Rev. 1.0
01/2015

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash with the CPU to provide single cycle random access to the flash up to 80 MHz system clock speed
  - Configurable read buffering and line prefetch support
  - Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller is pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 64 bits (two words)
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

2.2.10 SRAM

The MPC5634M SRAM module provides a general-purpose up to 94 KB memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB or 24 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 32-bit data element

2.2.11 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by Freescale and is identical for all MPC5634M MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on calibration bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the MPC5634M hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation

        - SCK to PCS delay
        - Delay between frames
    - Programmable serial frame size of 4 to 16 bits, expandable with software control
    - Continuously held chip select capability
- 6 Peripheral Chip Selects, expandable to 64 with external demultiplexer
- Deglitching support for up to 32 Peripheral Chip Selects with external demultiplexer
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO:
    - TX FIFO is not full (TFFF)
    - RX FIFO is not empty (RFDF)
- 6 Interrupt conditions:
    - End of queue reached (EOQF)
    - TX FIFO is not full (TFFF)
    - Transfer of current frame complete (TCF)
    - Attempt to transmit with an empty Transmit FIFO (TFUF)
    - RX FIFO is not empty (RFDF)
    - FIFO Underrun (slave only and SPI mode, the slave is asked to transfer data when the TxFIFO is empty)
    - FIFO Overrun (serial frame received while RX FIFO is full)
- Modified transfer formats for communication with slower peripheral devices
- Continuous Serial Communications Clock (SCK)
- Power savings via support for Stop Mode
- Enhanced DSI logic to implement a 32-bit Timed Serial Bus (TSB) configuration, supporting the Microsecond Channel downstream frame format

The DSPIs also support these features unique to the DSI and CSI configurations:

- 2 sources of the serialized data:
    - eTPU_A and eMIOS output channels
    - Memory-mapped register in the DSPI
- Destinations for the deserialized data:
    - eTPU_A and eMIOS input channels
    - SIU External Interrupt Request inputs
    - Memory-mapped register in the DSPI
- Deserialized data is provided as Parallel Output signals and as bits in a memory-mapped register
- Transfer initiation conditions:
    - Continuous
    - Edge sensitive hardware trigger
    - Change in data
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics
- Continuous serial communications clock
- Support for parallel and serial chaining of up to four DSPI blocks

2.2.16 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to Local Interconnect Network (LIN) slave devices. The eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format

- Independent interrupt source for each channel
- Counter can be stopped in debug mode

2.2.19 Software Watchdog Timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

2.2.20 Debug features

2.2.20.1 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time development support capabilities for the MPC5634MPower Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NPC block is an integration of several individual Nexus blocks that are selected to provide the development support interface for MPC5634M. The NPC block interfaces to the host processor (e200z335), eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace and run-time access to the MCUs internal memory map and access to the Power Architecture and eTPU internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. MPC5634Min the production 144 LQFP supports a 3.3 V reduced (4-bit wide) Auxiliary port. These Nexus port pins can also be used as 5 V I/O signals to increase usable I/O count of the device. When using this Nexus port as IO, Nexus trace is still possible using VertiCal calibration. In the VertiCal calibration package, the full 12-bit Auxiliary port is available.

NOTE

In the VertiCal package, the full Nexus Auxiliary port shares balls with the addresses of the calibration bus. Therefore multiplexed address/data bus mode must be used for the calibration bus when using full width Nexus trace in VertiCal assembly.

The following features are implemented:

- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Always available in production package
  - Supports both JTAG Boundary Scan and debug modes
  - 3.3 V interface
  - Supports Nexus class 1 features
  - Supports Nexus class 3 read/write feature
- 9-pin Reduced Port interface in 144 LQFP production package
  - Alternate function as IO
  - 5 V (in GPIO or alternate function mode), 3.3 V (in Nexus mode) interface

3 Pinout and signal description

This section contains the pinouts for all production packages for the MPC5634M family of devices. Please note the following:

- Pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.
- Pins labeled “NIC” have no internal connection.

3.1 144 LQFP pinout

Figure 2 shows the pinout for the 144-pin LQFP.

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
AN[13] MA[1] ETPU_A[21] SDO	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Out	PCR[216]	011 010 100 000	I O O O	VDDEH7	I / –	AN[13] / –		118	147	B12
AN[14] MA[2] ETPU_A[27] SDI	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data In	PCR[217]	011 010 100 000	I O O I	VDDEH7	I / –	AN[14] / –		117	146	C12
AN[15] FCK ETPU_A[29]	Single Ended Analog Input eQADC Free Running Clock ETPU_A Ch.	PCR[218]	011 010 000	I O O	VDDEH7	I / –	AN[15] / –		116	145	C13
AN[16]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		3	3	C6
AN[17]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		2	2	C4
AN[18]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		1	1	D5
AN[21]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		144	173	B4
AN[22]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		132	161	B8
AN[23]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		131	160	C9
AN[24]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		130	159	D8
AN[25]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		129	158	B9
AN[27]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		128	157	A10
AN[28]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		127	156	B10
AN[30]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		126	155	D9
AN[31]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		125	154	D10
AN[32]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		124	153	C10
AN[33]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		123	152	C11
AN[34]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		122	151	C5
AN[35]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		121	150	D11
AN[36]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	174[7]	F4[8]
AN[37]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	175[7]	E3[8]

[9] The GPIO functions on GPIO[206] and GPIO[207] can be selected as trigger functions in the SIU for the ADC by making the proper selections in the SIU_ETISR and SIU_ISEL3 registers in the SIU.

[10] Some signals in this section are available only on calibration package.

[11] These pins are only available in the 496 CSP/MAPBGA calibration/development package.

[12] On the calibration package, the Nexus function on this pin is enabled when the NEXUSCFG pin is high and Nexus is configured to full port mode. On the 176-pin and 208-pin packages, the Nexus function on this pin is enabled permanently. Do not connect the Nexus MDO or MSEO pins directly to a power supply or ground.

[13] In the calibration package, the I/O segment containing this pin is called VDDE12.

[14] 208-ball BGA package only

[15] When configured as Nexus (208-pin package or calibration package with NEXUSCFG=1), and JCOMP is asserted during reset, MDO[0] is driven high until the crystal oscillator becomes stable, at which time it is then negated.

[16] The function of this pin is Nexus when NEXUSCFG is high.

[17] High when the pin is configured to Nexus, low otherwise.

[18] O/Low for the calibration with NEXUSCFG=0; I/Up otherwise.

[19] ALT_ADDR/Low for the calibration package with NEXUSCFG=0; $\overline{\text{EVTI}}$/Up otherwise.

[20] In 176-pin and 208-pin packages, the Nexus function is disabled and the pin/ball has the secondary function

[21] This signal is not available in the 176-pin and 208-pin packages.

[22] The primary function is not selected via the PA field when the pin is a Nexus signal. Instead, it is activated by the Nexus controller.

[23] TDI and TDO are required for JTAG operation.

[24] The primary function is not selected via the PA field when the pin is a JTAG signal. Instead, it is activated by the JTAG controller.

[25] The function and state of the CAN_A and eSCI_A pins after execution of the BAM program is determined by the BOOTCFG1 pin.

[26] Connect an external 10K pull-up resistor to the SCI_A_RX pin to ensure that the pin is driven high during CAN serial boot.

[27] For pins AN[0:7], during and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

[28] ETPUA[24:29] are input and output. The input muxing is controlled by SIU_ISEL8 register.

[29] eTPU_A[25] is an output only function.

[30] Only the output channels of eTPU[8:9] are connected to pins.

[31] The function after reset of the XTAL pin is determined by the value of the signal on the PLLCFG[1] pin. When bypass mode is chosen XTAL has no function and should be grounded.

[32] The function after reset of the EXTAL_EXTCLK pin is determined by the value of the signal on the PLLCFG[1] pin. If the EXTCLK function is chosen, the valid operating voltage for the pin is 1.62 V to 3.6 V. If the EXTAL function is chosen, the valid operating voltage is 3.3 V.

[33] VSSPLL and VSSREG are connected to the same pin.

[34] This pin is shared by two pads: VDDA_AN, using pad_vdde_hv, and VDDA_DIG, using pad_vdde_int_hv.

[35] This pin is shared by two pads: VSSA_AN, using pad_vsse_hv, and VSSA_DIG, using pad_vsse_int_hv.

[36] VDDEH1A, VDDEH1B, and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[37] LVDS pins will not work at 3.3 V.

[38] The VDDEH6 segment may be powered from 3.0 V to 5.0 V for mux address or SSI functions, but must meet the VDDA specifications of 4.5 V to 5.25 V for analog input function.

8 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

9 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

10 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

11 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

12 Total injection current for all analog input pins must not exceed 15 mA.

13 Lifetime operation at these specification limits is not guaranteed.

14 Solder profile per CDF-AEC-Q100.

15 Moisture sensitivity per JEDEC test method A112.

4.3 Thermal characteristics

Table 8. Thermal characteristics for 144-pin LQFP

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[1]	Single layer board – 1s	43	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board – 2s2p	35	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Single layer board –1s	34	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Four layer board – 2s2p	29	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[2]		22	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case (Top)[3]		8	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[4]		2	°C/W

1 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.4 Electromagnetic Interference (EMI) characteristics

Table 11. EMI testing specifications[1]

Symbol	Parameter	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (Typ)	Unit
Radiated Emissions	V_{EME}	Device Configuration, test conditions and EM testing per standard IEC61967-2; Supply Voltage = 5.0V DC, Ambient Temperature = 25°C, Worst-case Orientation	Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; No PLL Frequency Modulation	150 kHz – 50 MHz	26	dBμV
				50–150 MHz	24	
				150–500 MHz	24	
				500–1000 MHz	21	
				IEC Level	K	—
			Oscillator Frequency = 8 MHz; System Bus Frequency = 80 MHz; 1% PLL Frequency Modulation	150 kHz – 50 MHz	20	dBμV
				50–150 MHz	19	
				150–500 MHz	14	
				500–1000 MHz	7	
				IEC Level	L	—

1 IEC Classification Level: L = 24dBuV; K = 30dBuV.

4.5 Electromagnetic static discharge (ESD) characteristics

Table 12. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for field induced charge Model (FCDM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset	Vdd33 – 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA	
5e	Vdd33 ILim[6]	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[5]	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[5]	Lvi3p3–6%	Lvi3p3	Lvi3p3+6%	V	See note [7]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[5]	Lvi3p3–3%	Lvi3p3	Lvi3p3+3%	V	See note 7
6c	—	CC	C	Trimming step LVI 3.3 V[5]	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis[5]	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the Vddeh POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r–35%	Por3.3V_r	Por3.3V_r+35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f–35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply[5]	—	4.290	—	V	
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset[5]	Lvi5p0–6%	Lvi5p0	Lvi5p0+6%	V	
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset[5]	Lvi5p0–3%	Lvi5p0	Lvi5p0+3%	V	
8c	—	CC	C	Trimming step LVI 5 V[5]	—	20	—	mV	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
I_{DDH1} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[23] supplies @ 80 MHz	V_{DDEH1}	—	—	See note [23]	mA
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[24]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.25 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[24]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[25]	—	–2.5	—	2.5	µA
I_{IC}	CC	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	CC	P	Analog input current, channel off, AN[0:7], AN38, AN39[26]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins (ANx)[26]	—	–150	—	150	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
C_L	CC	D	Load capacitance (fast I/O)[27]	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins[28])	—	—	—	12	pF
$R_{PUPD200K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 200 kΩ Option	—	130	—	280	kΩ
$R_{PUPDMATCH}$	CC	C	200KΩ Option		–2.5		2.5	%
$R_{PUPD100K}$	CC	P	Weak Pull-Up/Down Resistance[29,30] 100 kΩ Option	—	65	—	140	kΩ
$R_{PUPDMATCH}$	CC	C	100KΩ Option		–2.5		2.5	%
R_{PUPD5K}	CC	D	Weak Pull-Up/Down Resistance[29] 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
T_A (T_L to T_H)	SR	—	Operating temperature range - ambient (packaged)	—	–40.0	—	125.0	°C
—	SR	—	Slew rate on power supply pins	—	—	—	50	V/ms

1 These specifications are design targets and subject to change per device characterization.

2 TBD: To Be Defined.

3 V_{DDE} must be lower than V_{RC33}, otherwise there is additional leakage on pins supplied by V_{DDE}.

4 These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).

5 ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no bad behavior, but the accuracy will be degraded.

6 Internal structures hold the input voltage less than V_{DDA} + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.

7 The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.

4.16.4 eMIOS timing

Table 39. eMIOS timing[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

[1] eMIOS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

4.16.5 DSPI timing

Table 40. DSPI timing[1,2]

#	Symbol		C	Characteristic	40 MHz		60 MHz		80 MHz		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{SCK}	CC	D	SCK Cycle Time[3,4]	48.8 ns	5.8 ms	28.4 ns	3.5 ms	24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay[5]	46	—	26	—	22	—	ns
3	t_{ASC}	CC	D	After SCK Delay[6]	45	—	25	—	21	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle	$(½t_{SC})-2$	$(½t_{SC})+2$	$(½t_{SC})-2$	$(½t_{SC})+2$	$(½t_{SC})-2$	$(½t_{SC})+2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)	—	25	—	25	—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	—	25	—	25	—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	4	—	4	—	4	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	5	—	5	—	5	—	ns
9	t_{SUI}	CC	Data Setup Time for Inputs								
			D	Master (MTFE = 0)	20	—	20	—	20	—	ns
			D	Slave	2	—	2	—	2	—	
			D	Master (MTFE = 1, CPHA = 0)[7]	–4	—	6	—	8	—	
			D	Master (MTFE = 1, CPHA = 1)	20	—	20	—	20	—	

Table 40. DSPI timing[1,2] (continued)

#	Symbol		C	Characteristic	40 MHz		60 MHz		80 MHz		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{HI}	CC	Data Hold Time for Inputs								
			D	Master (MTFE = 0)	–4	—	–4	—	–4	—	ns
			D	Slave	7	—	7	—	7	—	
			D	Master (MTFE = 1, CPHA = 0)[7]	45	—	25	—	21	—	
			D	Master (MTFE = 1, CPHA = 1)	–4	—	–4	—	–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)								
			D	Master (MTFE = 0)	—	6	—	6	—	6	ns
			D	Slave	—	25	—	25	—	25	
			D	Master (MTFE = 1, CPHA=0)	—	45	—	25	—	21	
			D	Master (MTFE = 1, CPHA=1)	—	6	—	6	—	6	
12	t_{HO}	CC	Data Hold Time for Outputs								
			D	Master (MTFE = 0)	–5	—	–5	—	–5	—	ns
			D	Slave	5.5	—	5.5	—	5.5	—	
			D	Master (MTFE = 1, CPHA = 0)	8	—	4	—	3	—	
			D	Master (MTFE = 1, CPHA = 1)	–5	—	–5	—	–5	—	

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at VDDEH = 3.0–5.25 V, TA = TL to TH, and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 62 MHz parts allow for a 60 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC5634M devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

4.16.6 eQADC SSI timing

Table 41. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency [2, 3]	1/17 f_{SYS_CLK}		1/2 f_{SYS_CLK}	Hertz
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2 t_{SYS_CLK}		17t_{SYS_CLK}	seconds
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} – 6.5		9* t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} – 6.5		8* t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		+7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		+7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

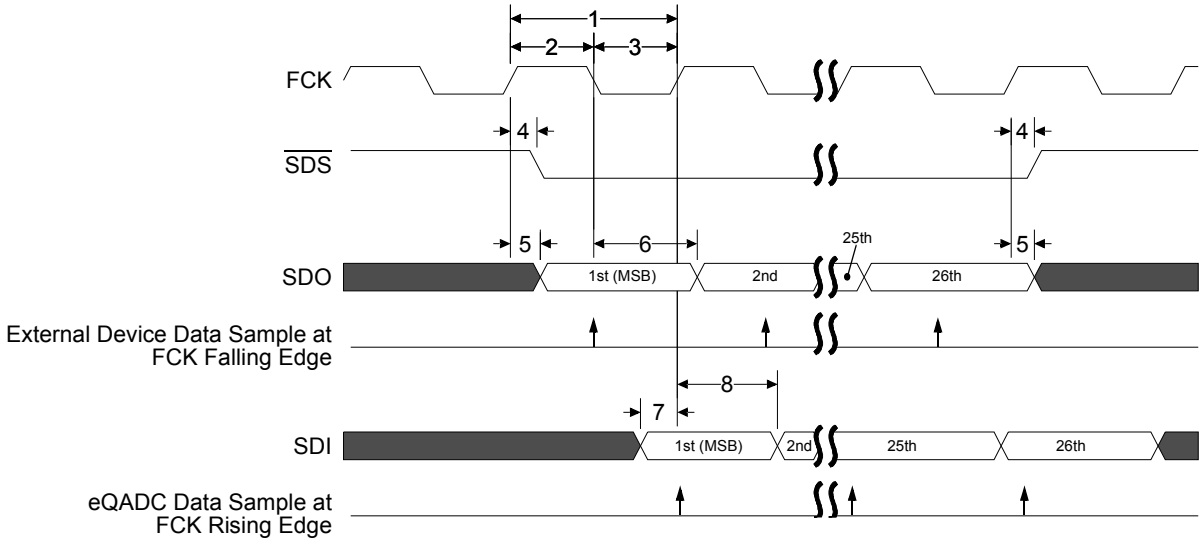


Figure 29. eQADC SSI timing

5.1.2 176 LQFP

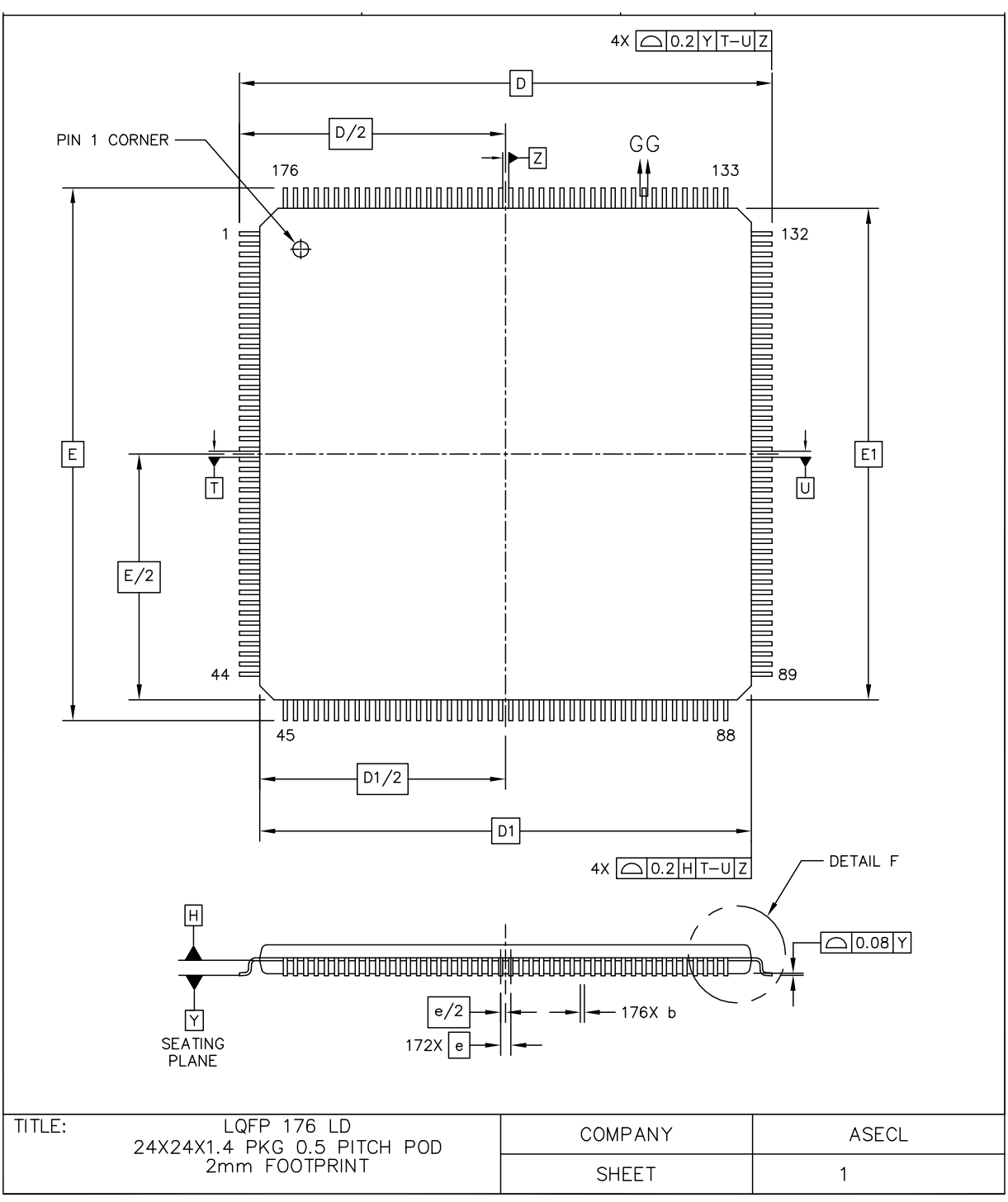
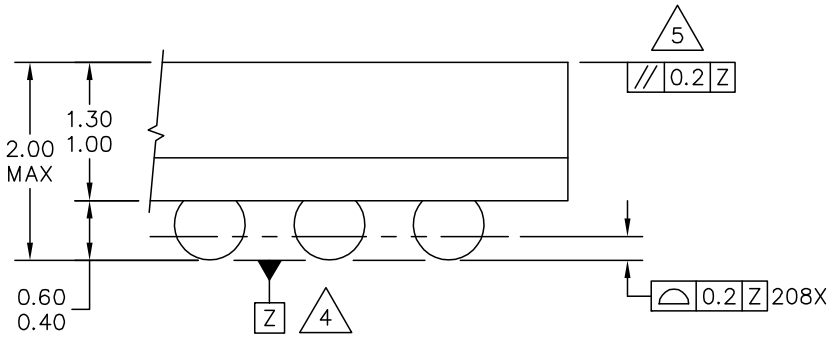


Figure 33. 176 LQFP package mechanical drawing (part 1)

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARS23882W
	PAGE: 1159A
DO NOT SCALE THIS DRAWING	REV: D



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2 OF 3

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev.4	12/2009	208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) has changed. Power Management Control (PMC) and Power On Reset (POR) electrical specifications updated Temperature sensor data added Specifications now indicate how each controller characteristic parameter is guaranteed. I/O pad current specifications updated I/O Pad VRC33 current specifications updated PAD AC characteristics updated VGA gain specifications added to eQADC electrical characteristics DC electrical specifications updated: • Footnote added to RPUPD100K and RPUPD200K: When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from other devices, the resulting pad voltage will be 0.5*VDDE ± 2.5% • I_{OL} condition added to V_{OL_LS}. • I_{OH} condition added to V_{OH_LS}. • Minimum V_{OH_LS} is 2.3 V (was 2.7 V). • Separate I_{DDPLL} removed from I_{DD} spec because we can only measure I_{DD} + I_{DDPLL}. I_{DD} increased by 15 mA (to 195 mA) to account for I_{DDPLL}. I_{DD} now documented as I_{DD} + I_{DDPLL}. Footnote added detailing runtime configuration used to measure I_{DD} + I_{DDPLL}. • Specifications for I_{DDSTBY} and $I_{DDSTBY150}$ reformatted to make more clear. • V_{STBY} is now specified by two ranges. The area in between those ranges is indeterminate. LVDS pad specifications updated: • Min value for V_{OD} at SRC=0b01 is 90 mV (was 120); and 160 mV (was 180) at SRC = 0b10 Changes to Signal Properties table: • VDDE7 removed as voltage segment from Calibration bus pins. Calibration bus pins are powered by VDDE12 only. • GPIO[139] and GPIO[87] pins changed to Medium pads • Some signal names have changed on 176-pin QFP package pinout: “CAL_x” signals renamed to “ALT_x”. Changes to Pad Types table: • Column heading changed from “Voltage” to “Supply Voltage” • MultiV pad high swing mode voltage changed to 3.0 V – 5.25 V (was 4.5 V – 5.25 V) • MultiV pad low swing mode voltage changed to 4.5 V – 5.25 V (was 3.0 V – 3.6 V) Signal details table added Power/ground segmentation table added 100-pin package is no longer available

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