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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf2mlq60r

1 Addendum List for Revision 9

Table 1. MPC5634M Rev 9 Addendum

Location	Description
Section 4.11, “Temperature Sensor Electrical Characteristics”, Page 81	In “Temperature Sensor Electrical Characteristics” table, update the Min and Max value of “Accuracy” parameter to -20^{o}C and +20^{o}C, respectively.

2 Revision History

Table 2 provides a revision history for this datasheet addendum document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release.	12/2014

- Frequency Modulating Phase-locked loop (FMPLL)
  - Reference clock pre-divider (PREDIV) for finer frequency synthesis resolution
  - Reduced frequency divider (RFD) for reducing the FMPLL output clock frequency without forcing the FMPLL to re-lock
  - System clock divider (SYSDIV) for reducing the system clock frequency in normal or bypass mode
  - Input clock frequency range from 4 MHz to 20 MHz before the pre-divider, and from 4 MHz to 16 MHz at the FMPLL input
  - Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
  - VCO free-running frequency range from 25 MHz to 125 MHz
  - Four bypass modes: crystal or external reference with PLL on or off
  - Two normal modes: crystal or external reference
  - Programmable frequency modulation
    - Triangle wave modulation
    - Register programmable modulation frequency and depth
  - Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
    - User-selectable ability to generate an interrupt request upon loss of lock
    - User-selectable ability to generate a system reset upon loss of lock
  - Clock quality monitor (CQM) module provides loss-of-clock detection for the FMPLL reference and output clocks
    - User-selectable ability to generate an interrupt request upon loss of clock
    - User-selectable ability to generate a system reset upon loss of clock
    - Backup clock (reference clock or FMPLL free-running) can be applied to the system in case of loss of clock
- Calibration bus interface (EBI)
  - Available only in the calibration package (496 CSP package)
  - 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
  - Memory controller with support for various memory types
  - 16-bit data bus, up to 22-bit address bus
  - Selectable drive strength
  - Configurable bus speed modes
  - Bus monitor
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 80 I/O pins
  - Centralized pad control on a per-pin basis
    - Pin function selection
    - Configurable weak pull-up or pull-down
    - Drive strength
    - Slew rate
    - Hysteresis
  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
  - Critical Interrupt control
  - Non-Maskable Interrupt control
  - Internal multiplexer subblock (IMUX)
    - Allows flexible selection of eQADC trigger inputs (eTPU, eMIOS and external signals)

intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

The eTPU2 includes these distinctive features:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- 32 channels, each channel is associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity.
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations

Table 1. MPC5634M series block summary (continued)

Block	Function
DMA (direct memory access)	Performs complex data movements with minimal intervention from the core
DSPI (deserial serial peripheral interface)	Provides a synchronous serial interface for communication with external devices
eMIOS (enhanced modular input-output system)	Provides the functionality to generate or measure events
eQADC (enhanced queued analog-to-digital converter)	Provides accurate and fast conversions for a wide range of applications
eSCI (serial communication interface)	Allows asynchronous serial communications with peripheral devices and other microcontroller units
eTPU (enhanced time processor unit)	Processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports the programmable frequency modulation of these clocks
INTC (interrupt controller)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
NPC (Nexus Port Controller)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
PIT (peripheral interrupt timer)	Produces periodic interrupts and triggers
Temperature sensor	Provides the temperature of the device as an analog value
SWT (Software Watchdog Timer)	Provides protection from runaway code
STM (System Timer Module)	Timer providing a set of output compare events to support AutoSAR and operating system tasks

3.4 208 MAPBGA ballmap (MPC5634M)

Figure 5 shows the 208-pin MAPBGA ballmap for the MPC5634M (1536 KB flash memory) as viewed from above.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12- $\overline{SDS}$	ALT_ MDO2	ALT_ MDO0	VRC33	VSS
B	VDD	VSS	AN38	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	ALT_ MDO3	ALT_ MDO1	VSS	VDD
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15 FCK	VSS	$\overline{ALT\_MSEO0}$	TCK
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	ALT_$\overline{EVTO}$	NIC[1]
E	ETPUA30	ETPUA31	AN37	VDD									VDDE7	TDI	ALT_$\overline{EVTI}$	$\overline{ALT\_MSEO1}$
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6	TDO	ALT_MCKO	JCOMP
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO99	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	GPIO98	DSPI_B_ SCK
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1			VSS	VSS	VSS	VSS			CAN_C_ TX	SCI_A_RX	$\overline{RSTOUT}$	VDDREG
L	ETPUA12	ETPUA11	ETPUA6	ETPUA0									SCI_B_TX	CAN_C_ RX	WKPCFG	$\overline{RESET}$
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSSPLL
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH1/6[2]	EMIOS12	eTPU_A19[3]	VRC33	VSS	VRCCTL	NIC[1]	EXTAL
P	ETPUA3	ETPUA2	VSS	VDD	GPIO207	VDDE7	NIC[1]	EMIOS8	eTPU_A29[3]	eTPU_A2[3]	eTPU_A21[3]	CAN_A_ TX	VDD	VSS	NIC[1]	XTAL
R	NIC[1]	VSS	VDD	GPIO206	EMIOS4	NIC[1]	EMIOS9	EMIOS11	EMIOS14	eTPU_A27[3]	EMIOS23	CAN_A_ RX	NIC[1]	VDD	VSS	VDDPLL
T	VSS	VDD	NIC[1]	EMIOS0	EMIOS1	GPIO219	eTPU_A25[3]	EMIOS13	EMIOS15	eTPU_A4[3]	eTPU_A13[3]	NIC[1]	VDDE5	CLKOUT	VDD	VSS

1 Pins marked “NIC” have no internal connection.
2 This ball may be changed to “NC” (no connection) in a future revision.
3 eTPU output only channel.

Figure 5. 208-pin MAPBGA ballmap (MPC5634M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPB GA
eTPU_A[28][28] DSPI_C_PCS[1] GPIO[142]	eTPU_A Ch. (Input and Output) DSPI_C Periph Chip Select GPIO	PCR[142]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		17	24	F1
eTPU_A[29][28] DSPI_C_PCS[2] GPIO[143]	eTPU_A Ch. (Input and Output) DSPI_C Periph Chip Select GPIO	PCR[143]	10 01 00	I/O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		16	23	F2
eTPU_A[30] DSPI_C_PCS[3] eTPU_A[11] GPIO[144]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[144]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		15	22	E1
eTPU_A[31] DSPI_C_PCS[4] eTPU_A[13] GPIO[145]	eTPU_A Ch. DSPI_C Periph Chip Select eTPU_A Ch. GPIO	PCR[145]	011 010 001 000	I/O O O I/O	VDDEH1a Medium	– / WKPCFG	– / WKPCFG		14	21	E2
eMIOS											
eMIOS[0] eTPU_A[0] eTPU_A[25][29] GPIO[179]	eMIOS Ch. eTPU_A Ch. eTPU_A Ch. GPIO	PCR[179]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		54	63	T4
eMIOS[1] eTPU_A[1] GPIO[180]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[180]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		—	64[7]	T5[8]
eMIOS[2] eTPU_A[2] GPIO[181]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[181]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		55	65	N7
eMIOS[4] eTPU_A[4] GPIO[183]	eMIOS Ch. eTPU_A Ch. GPIO	PCR[183]	01 10 00	I/O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		56	67	R5
eMIOS[8] eTPU_A[8][30] SCI_B_TX GPIO[187]	eMIOS Ch. eTPU_A Ch. eSCI_B Transmit GPIO	PCR[187]	001 010 100 000	I/O O O I/O	VDDEH6a Slow	– / WKPCFG	– / WKPCFG		57	70	P8

[39] VDDEH6A and VDDEH6B are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[40] If using JTAG or Nexus, the I/O segment that contains the JTAG and Nexus pins must be powered by a 5 V supply. The 3.3 V Nexus/JTAG signals are derived from the 5 volt power supply.

[41] In the calibration package this signal is named VDDE12.

Table 3. Pad types

Pad Type	Name	Supply Voltage
Slow	pad_ssr_hv	3.0 V – 5.25 V
Medium	pad_msr_hv	3.0 V – 5.25 V
Fast	pad_fc	3.0 V – 3.6 V
MultiV	pad_multv_hv	3.0 V – 5.25 V (high swing mode) 4.5 V – 5.25 V (low swing mode)
Analog	pad_ae_hv	0.0 – 5.25 V
LVDS	pad_lo_lv	—

8 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

9 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

10 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

11 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

12 Total injection current for all analog input pins must not exceed 15 mA.

13 Lifetime operation at these specification limits is not guaranteed.

14 Solder profile per CDF-AEC-Q100.

15 Moisture sensitivity per JEDEC test method A112.

4.3 Thermal characteristics

Table 8. Thermal characteristics for 144-pin LQFP

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[1]	Single layer board – 1s	43	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board – 2s2p	35	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Single layer board –1s	34	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Ambient (@200 ft/min)[2]	Four layer board – 2s2p	29	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[2]		22	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case (Top)[3]		8	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[4]		2	°C/W

1 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset	Vdd33 – 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA	
5e	Vdd33 ILim[6]	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply[5]	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset[5]	Lvi3p3–6%	Lvi3p3	Lvi3p3+6%	V	See note [7]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset[5]	Lvi3p3–3%	Lvi3p3	Lvi3p3+3%	V	See note 7
6c	—	CC	C	Trimming step LVI 3.3 V[5]	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis[5]	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the Vddeh POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r–35%	Por3.3V_r	Por3.3V_r+35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f–35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply[5]	—	4.290	—	V	
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset[5]	Lvi5p0–6%	Lvi5p0	Lvi5p0+6%	V	
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset[5]	Lvi5p0–3%	Lvi5p0	Lvi5p0+3%	V	
8c	—	CC	C	Trimming step LVI 5 V[5]	—	20	—	mV	

4.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 19. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200–600[1]	mV
V_{BE}	Base-to-emitter voltage	0.4–1.0	V

[1] Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}

4.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification but use of the following sequence is strongly recommended when the internal regulator is bypassed:

5 V → 3.3 V and 1.2 V

This is also the normal sequence when the internal regulator is enabled.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to table Table 20 for all pins with fast pads and Table 21 for all pins with medium, slow and multi-voltage pads.[1]

Table 20. Power sequence pin states for fast pads

V_{DDE}	V_{RC33}	V_{DD}	Fast (pad_fc)
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 21. Power sequence pin states for medium, slow and multi-voltage pads

V_{DDEH}	V_{DD}	Medium (pad_msr_hv) Slow (pad_ssr_hv) Multi-voltage (pad_multv_hv)
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

1.If an external 3.3V external regulator is used to supply current to the 1.2V pass transistor and this supply also supplies current for the other 3.3V supplies, then the 5V supply must always be greater than or equal to the external 3.3V supply.

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

4.13 Platform flash controller electrical characteristics

Table 30. APC, RWSC, WWSC settings vs. frequency of operation[1]

Target Max Frequency (MHz)	APC[2]	RWSC[2]	WWSC
21[3]	000	000	01
41[3]	001	001	01
62[3]	010	010	01
82[3]	011	011	01
All	111	111	111

1 Illegal combinations exist, all entries must be taken from the same row

2 APC must be equal to RWSC

3 Maximum Frequency includes FM modulation

4.14 Flash memory electrical characteristics

Table 31. Program and erase specifications

Symbol		Parameter	Min Value	Typical Value[1]	Initial Max[2]	Max[3]	Unit
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[4]	—	22	50	500	µs
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{64kpperase}$	P	64 KB Block Pre-program and Erase Time	—	600	900	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

4.15 AC specifications

4.15.1 Pad AC specifications

Table 33. Pad AC specifications (5.0 V)[1,2]

Name		C	Output Delay (ns)[3,4] Low-to-High / High-to-Low		Rise/Fall Edge ( )[4,5]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[6,7,8]	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11[9]
	CC	D	13/10	32/32	9/9	22/22	200	
	N/A							10[10]
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	23/23	52/59	11/14	31/31	200	
	CC	D	69/71	152/165	34/35	74/74	50	00
	CC	D	95/90	205/220	44/51	96/96	200	
Slow[8,11]	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11[9]
	CC	D	24/19	58/58	17/15	42/42	200	
	N/A							10[10]
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	49/45	115/115	27/23	61/61	200	
	CC	D	137/142	320/330	72/74	164/164	50	00
	CC	D	182/172	420/420	90/85	200/200	200	
MultiV[12] (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11[9]
	CC	D	10.4/10.2	24.2/23.6	12.7/11.54	29/29	200	
	N/A							10[10]
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	15.9/13.6	31/28.5	14.6/13.1	31/31	200	
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
	CC	D	85.5/37.3	132.6/ 78.9	57.7/46.4	85/85	200	
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	7/7	30	11[9]
Fast[13]	N/A							
pad_i_hv[14]	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000	—	5000/5000	50	N/A

1 These are worst case values that are estimated from simulation and not tested. Values in the table are simulated at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 1.62 V to 1.98 V, V_{DDEH} = 4.5 V to 5.25 V, $T_A = T_L$ to T_H.

2 TBD: To Be Defined.

3 This parameter is supplied for reference and is not guaranteed by design and not tested.
4 Delay and rise/fall are measured to 20% or 80% of the respective signal.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
7 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
8 Output delay is shown in Figure 8. Add a maximum of one system clock to the output delay for delay with respect to system clock.
9 Can be used on the tester.
10 This drive select value is not supported. If selected, it will be approximately equal to 11.
11 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
12 Selectable high/low swing IO pad with selectable slew in high swing mode only.
13 Fast pads are 3.3 V pads.
14 Stand alone input buffer. Also has weak pull-up/pull-down.

Table 34. Pad AC specifications (3.3 V)[1]

Pad Type		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7,10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7,11] (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11[8]
	CC	D		46/49		37/37	200	
	N/A							10[9]
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	

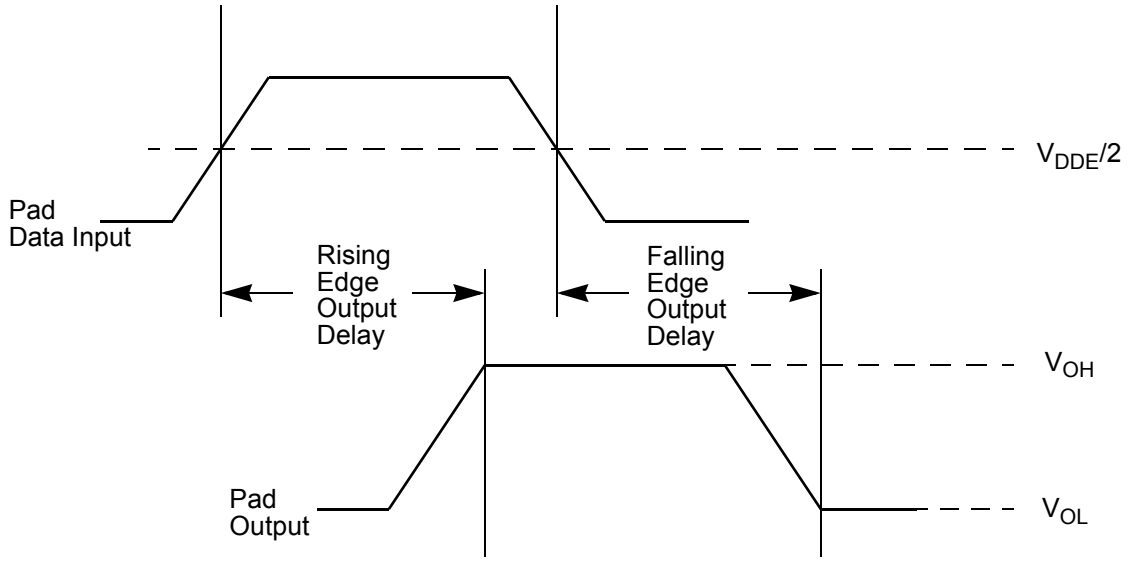

Figure 8. Pad output delay

4.16 AC timing

4.16.1 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% – 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	23	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	20	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns

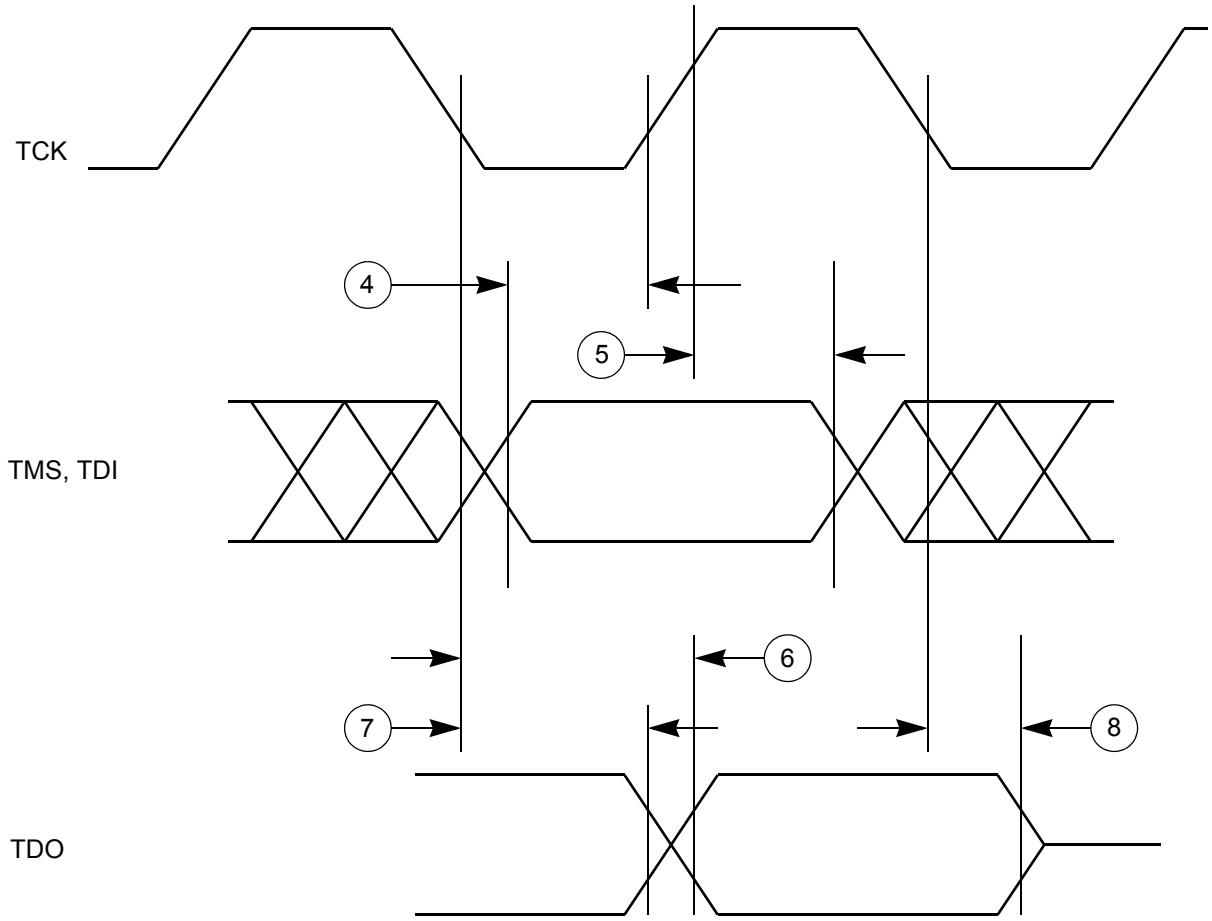

Figure 10. JTAG test access port timing

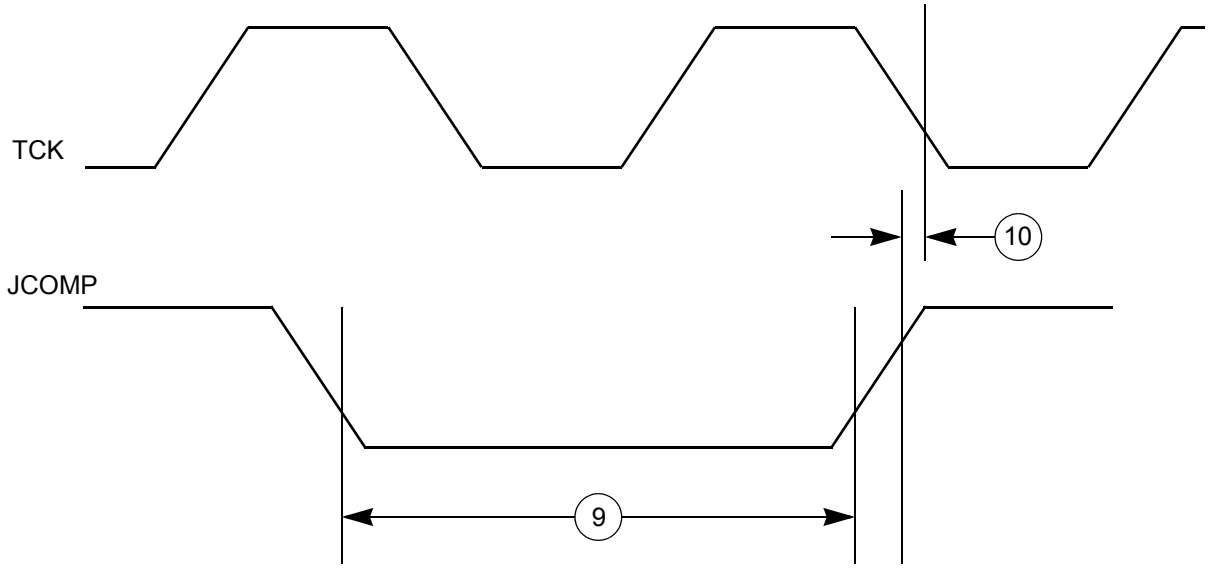

Figure 11. JTAG JCOMP timing

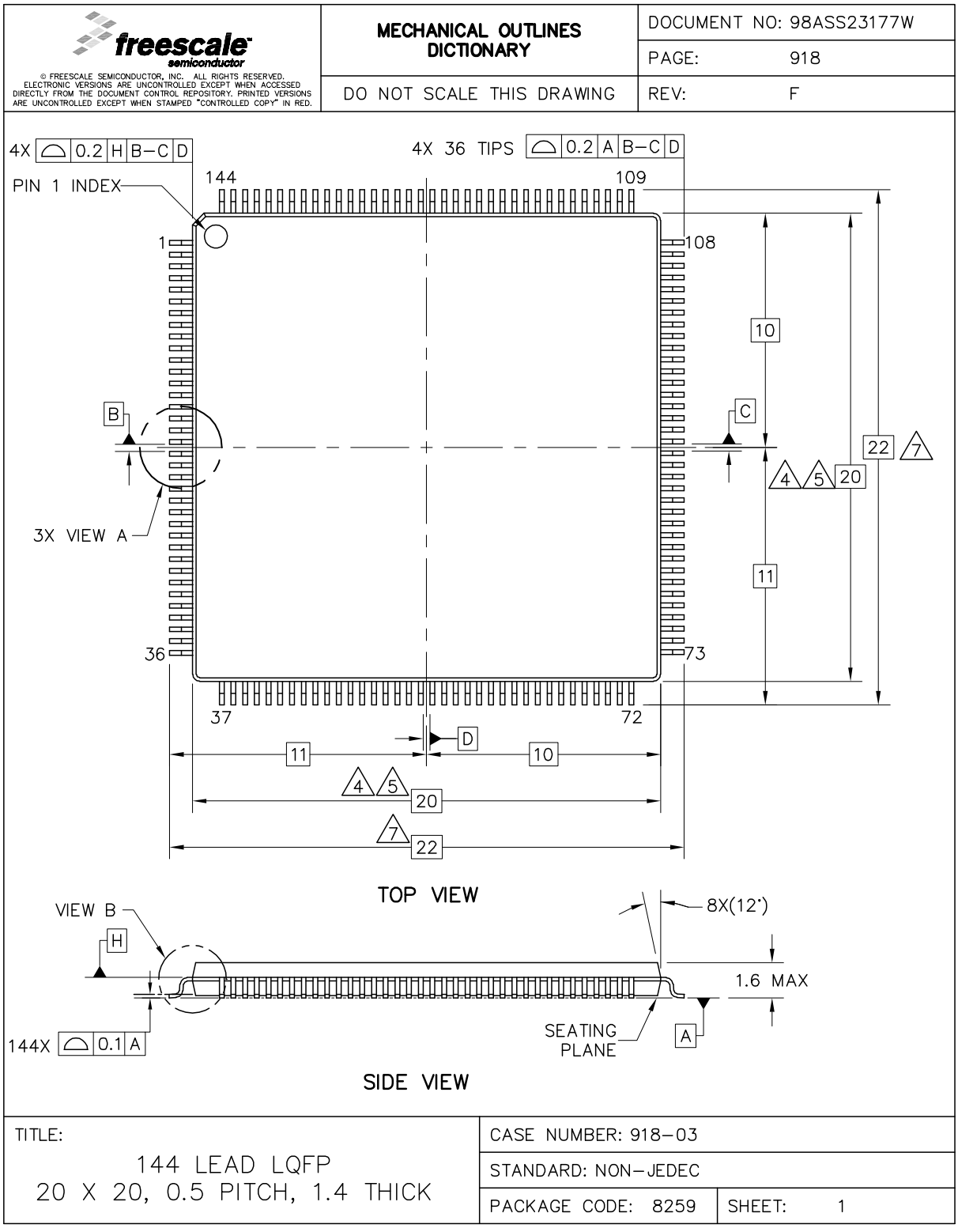

Figure 30. 144 LQFP package mechanical drawing (part 1)

5.1.2 176 LQFP

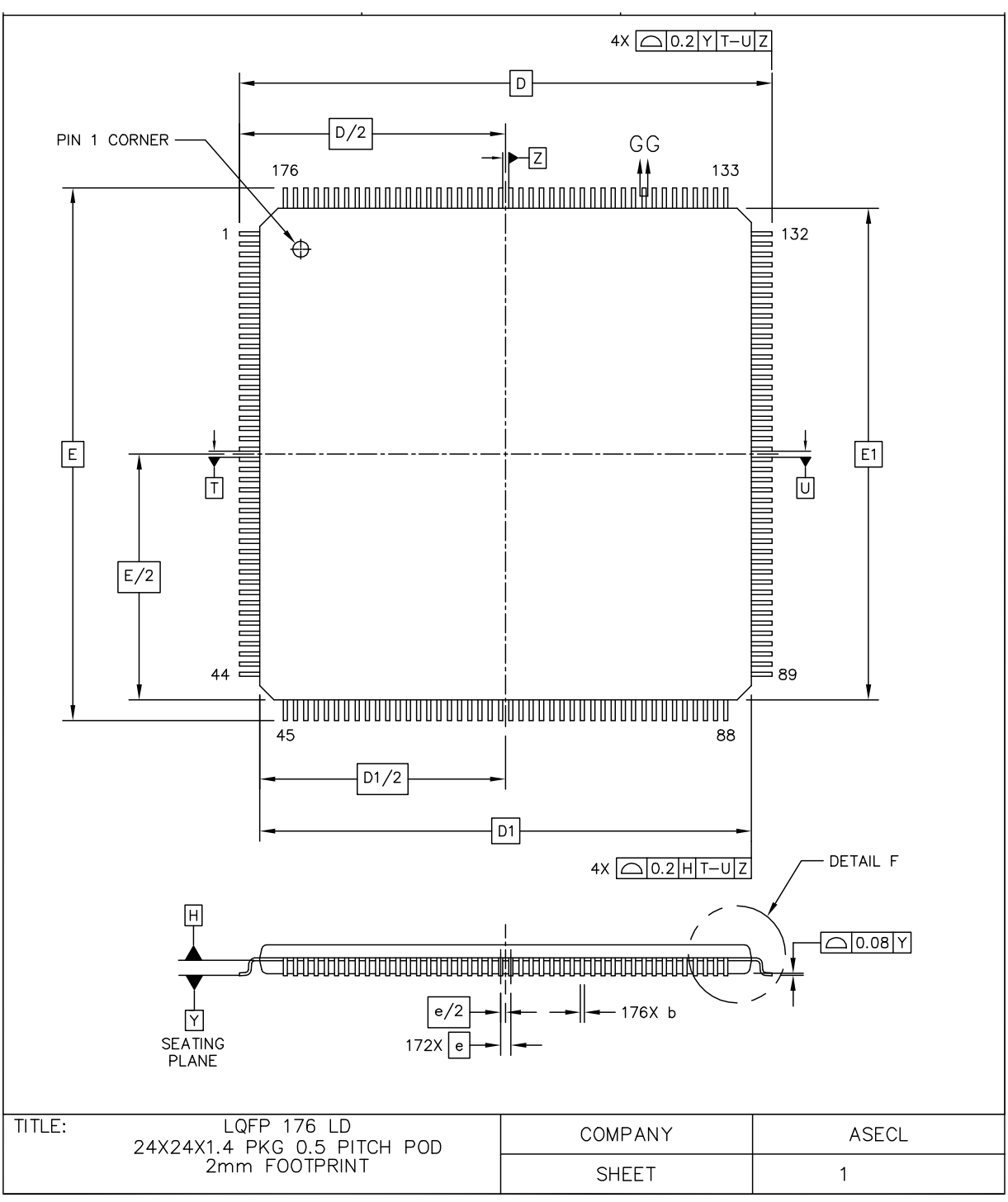

Figure 33. 176 LQFP package mechanical drawing (part 1)

7 Document revision history

Table 43 summarizes revisions to this document.

Table 43. Revision history

Revision	Date	Description of Changes
Rev. 1	4/2008	Initial release
Rev. 2	12/2008	• Maximum amount of flash increased from 1 MB to 1.5 MB. Flash memory type has changed. Rev. 1 and later devices use LC flash instead of FL flash. • Additional packages offered—now includes100 LQFP and 176 LQFP. Please note that the pinouts can vary for the same package depending on the amount of flash memory included in the device. • Device comparison table added. • Feature details section added • Signal summary table expanded. Now includes PCR register numbers and signal selection values and pin numbers for all production packages. • Electrical characteristics updated. • DSPI timing data added for 40 MHz and 60 MHz. • Thermal characteristics data updated. Data added for 100- and 176-pin packages. • DSPI LVDS pad specifications added.
Rev. 3	2/2009	Electrical characteristics updated • Flash memory electrical characteristics updated for LC flash • Power management control (PMC) and Power on Reset (POR) specifications updated • EMI characteristics data added • Maximum ratings updated • I/O pad current specifications updated • I/O Pad VRC33 current specifications added • Temperature sensor electrical characteristics added Pad type added to “Voltage” column of signal summary table Many signal names have changed to make them more understandable • DSPI: PCS_C[n] is now DSPI_C_PCS[n]; SOUT_C is now DSPI_C_SOUT, SIN_C is now DSPI_C_SIN, and SCK_C is now DSPI_C_SCK • CAN: CNTXB is now CAN_B_TX and CNRXB is now CAN_B_RC • SCI: RXDB is now SCI_B_RX and TXDB is now SCI_B_TX • In cases where multiple instances of the same IP block is incorporated into the device, e.g., 2 SCI blocks, the above nomenclature applies to all blocks “No connect” pins on pinouts clarified • Pins labelled “NIC” have no internal connection and should be tied to ground • Pins labelled “NC” are not functional pins but may be connected to internal circuits They are to be left floating Some of the longer multiplexed signal names appearing on pinouts have been moved to the inside of the package body to avoid having to use smaller fonts Orderable parts table updated Part number decoder added

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev.4	12/2009	208-pin MAPBGA ballmap for the MPC5633M (1024 KB flash memory) has changed. Power Management Control (PMC) and Power On Reset (POR) electrical specifications updated Temperature sensor data added Specifications now indicate how each controller characteristic parameter is guaranteed. I/O pad current specifications updated I/O Pad VRC33 current specifications updated PAD AC characteristics updated VGA gain specifications added to eQADC electrical characteristics DC electrical specifications updated: • Footnote added to RPUPD100K and RPUPD200K: When the pull-up and pull-down of the same nominal 200 KΩ or 100 KΩ value are both enabled, assuming no interference from other devices, the resulting pad voltage will be 0.5*VDDE ± 2.5% • I_{OL} condition added to V_{OL_LS}. • I_{OH} condition added to V_{OH_LS}. • Minimum V_{OH_LS} is 2.3 V (was 2.7 V). • Separate I_{DDPLL} removed from I_{DD} spec because we can only measure I_{DD} + I_{DDPLL}. I_{DD} increased by 15 mA (to 195 mA) to account for I_{DDPLL}. I_{DD} now documented as I_{DD} + I_{DDPLL}. Footnote added detailing runtime configuration used to measure I_{DD} + I_{DDPLL}. • Specifications for I_{DDSTBY} and $I_{DDSTBY150}$ reformatted to make more clear. • V_{STBY} is now specified by two ranges. The area in between those ranges is indeterminate. LVDS pad specifications updated: • Min value for V_{OD} at SRC=0b01 is 90 mV (was 120); and 160 mV (was 180) at SRC = 0b10 Changes to Signal Properties table: • VDDE7 removed as voltage segment from Calibration bus pins. Calibration bus pins are powered by VDDE12 only. • GPIO[139] and GPIO[87] pins changed to Medium pads • Some signal names have changed on 176-pin QFP package pinout: “CAL_x” signals renamed to “ALT_x”. Changes to Pad Types table: • Column heading changed from “Voltage” to “Supply Voltage” • MultiV pad high swing mode voltage changed to 3.0 V – 5.25 V (was 4.5 V – 5.25 V) • MultiV pad low swing mode voltage changed to 4.5 V – 5.25 V (was 3.0 V – 3.6 V) Signal details table added Power/ground segmentation table added 100-pin package is no longer available