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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf2mlq80r

1 Addendum List for Revision 9

Table 1. MPC5634M Rev 9 Addendum

Location	Description
Section 4.11, “Temperature Sensor Electrical Characteristics”, Page 81	In “Temperature Sensor Electrical Characteristics” table, update the Min and Max value of “Accuracy” parameter to -20^{o}C and +20^{o}C, respectively.

2 Revision History

Table 2 provides a revision history for this datasheet addendum document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release.	12/2014

standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

2.3 MPC5634M series architecture

2.3.1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5634M series.

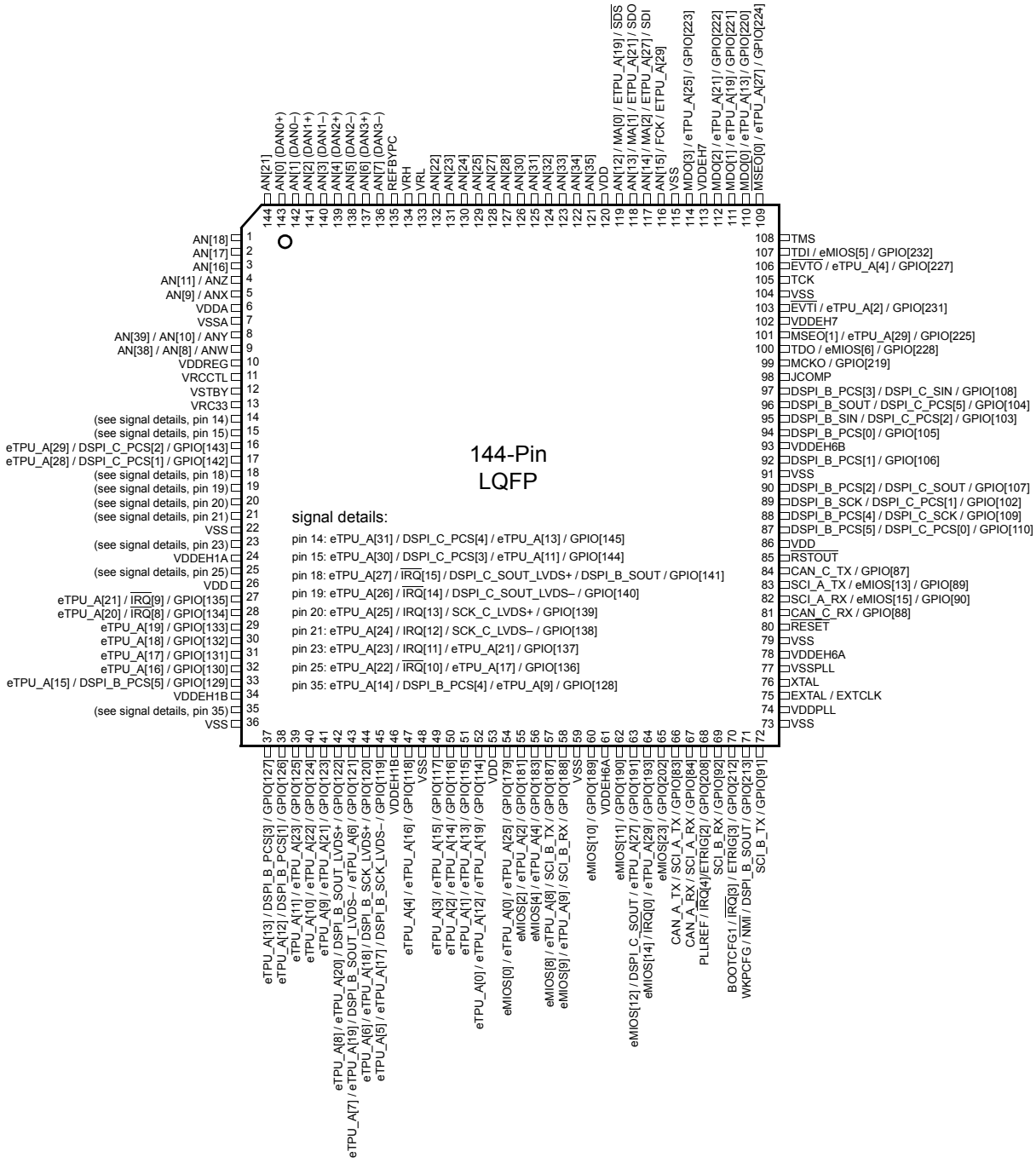
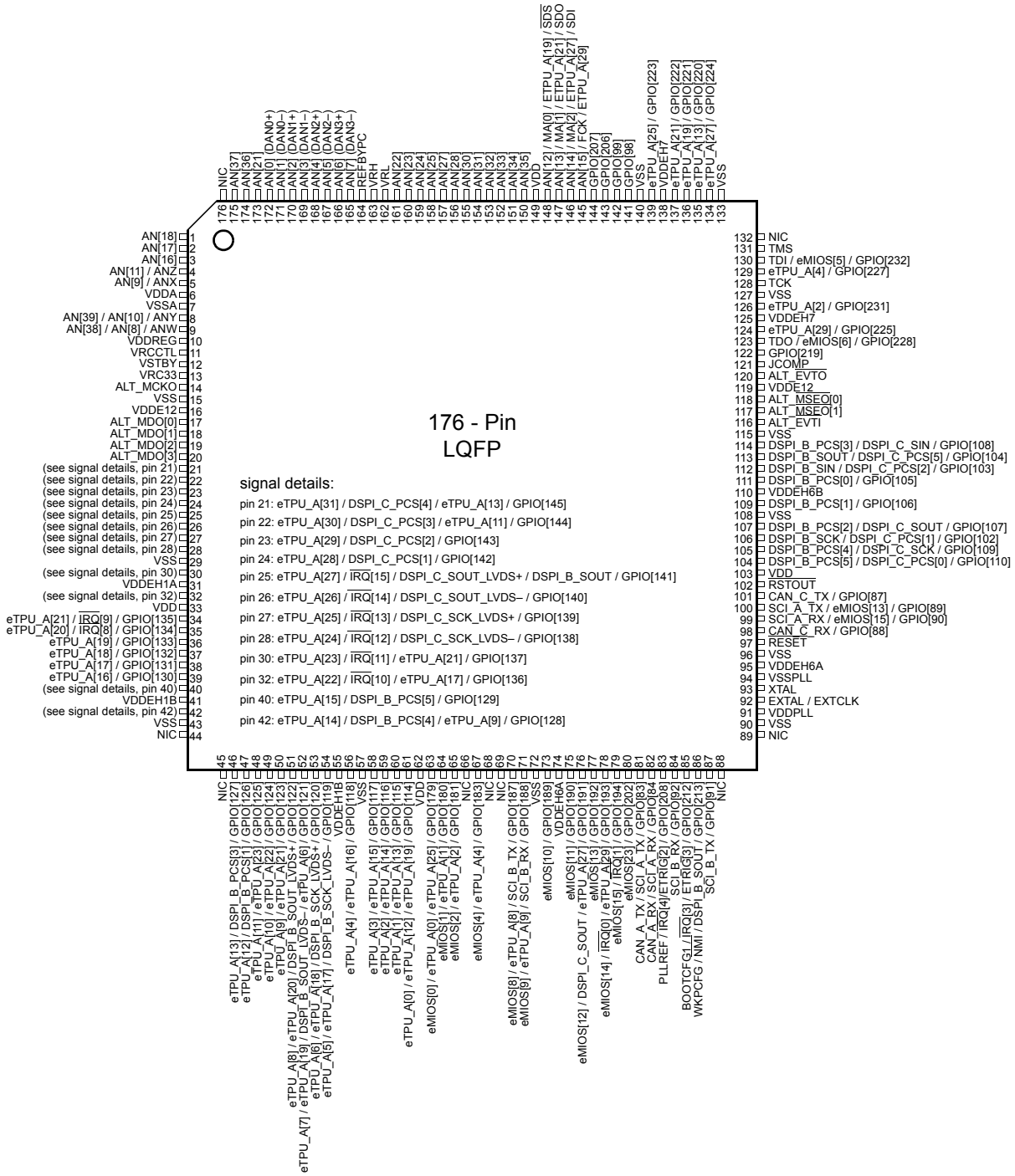


Figure 2. 144-pin LQFP pinout (top view; all 144-pin devices)

3.2 176 LQFP pinout (MPC5634M)

Figure 3 shows the 176-pin LQFP pinout for the MPC5634M (1536 KB flash memory).



Note: Pins marked “NIC” have no internal connection.

Figure 3. 176-pin LQFP pinout (MPC5634M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]		Pin No.		
									144 LQFP	176 LQFP	208 MAPBGA
VSTBY	Power Supply for Standby RAM	—	—	I	VSTBY	I / –	—		12	12	C1
VRC33	3.3V Voltage Regulator Bypass Capacitor	—	—	O	VRC33	O / –	—		13	13	A15, D1, N6, N12
VRCCTL	Voltage Regulator Control Output	—	—	O	NA	O / –	—		11	11	N14
VDDA[34]	Analog Power Input for eQADC	—	—	I	VDDA (5.0 V)	I / –	—		6	6	—
VDDA0	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	B11
VSSA0	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A11
VDDA1	Analog Power Input for eQADC	—	—	I	VDDA	I / –	—		—	—	A4
VSSA1	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		—	—	A5
VSSA[35]	Analog Ground Input for eQADC	—	—	I	VSSA	I / –	—		7	7	—
VDDREG	Voltage Regulator Supply	—	—	I	VDDREG (5.0 V)	I / –	—		10	10	K16
VDD	Internal Logic Supply Input	—	—	I	VDD (1.2 V)	I / –	—		26, 53, 86, 120	33, 62, 103, 149	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15

3.7 Signal details

Table 4 contains details on the multiplexed signals that appear in Table 2, “MPC563xM signal properties”.

Table 4. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	MPC5634M clock output for the external/calibration bus interface
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
EXTCLK	Clock Generation	External clock input
PLLREF	Clock Generation	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode.
XTAL	Clock Generation	Crystal oscillator input
SCK_B_LVDS– SCK_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SOUT_B_LVDS– SOUT_B_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
SCK_C_LVDS– SCK_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
SOUT_C_LVDS– SOUT_C_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
PCS_B[0] PCS_C[0]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—slave select when used in slave mode
PCS_B[1:5] PCS_C[1:5]	DSPI_B – DSPI_C	Peripheral chip select when device is in master mode—not used in slave mode
SCK_B SCK_C	DSPI_B – DSPI_C	DSPI clock—output when device is in master mode; input when in slave mode
SIN_B SIN_C	DSPI_B – DSPI_C	DSPI data in
SOUT_B SOUT_C	DSPI_B – DSPI_C	DSPI data out
CAL_ADDR[12:30]	Calibration Bus	The CAL_ADDR[12:30] signals specify the physical address of the bus transaction.
CAL_$\overline{\text{CS}}$[0:3]	Calibration Bus	$\overline{\text{CS}}$x is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the Primary external bus.
CAL_DATA[0:15]	Calibration Bus	The CAL_DATA[0:15] signals contain the data to be transferred for the current transaction.
CAL_$\overline{\text{OE}}$	Calibration Bus	$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip-select accesses.

Table 4. Signal details (continued)

Signal	Module or Function	Description
CAL_RD_$\overline{WR}$	Calibration Bus	RD_$\overline{WR}$ indicates whether the current transaction is a read access or a write access.
CAL_$\overline{TS}$_ALE	Calibration Bus	The Transfer Start signal ($\overline{TS}$) is asserted by the MPC5634M to indicate the start of a transfer. The Address Latch Enable (ALE) signal is used to demultiplex the address from the data bus.
CAL_$\overline{EVTO}$	Calibration Bus	Nexus Event Out
CAL_MCKO	Calibration Bus	Nexus Message Clock Out
NEXUSCFG	Nexus/Calibration Bus	Nexus/Calibration Bus selector
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
FCK	eQADC	eQADC free running clock for eQADC SSI.
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX	eSCI_A – eSCI_B	eSCI receive
SCI_A_TX SCI_B_TX	eSCI_A – eSCI_B	eSCI transmit
ETPU_A[0:31]	eTPU	eTPU I/O channel
CAN_A_TX CAN_C_TX	FlexCan_A – FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_C_RX	FlexCAN_A – FlexCAN_C	FlexCAN receive
JCOMP	JTAG	Enables the JTAG TAP controller.
TCK	JTAG	Clock input for the on-chip test and debug logic.
TDI	JTAG	Serial test instruction and data input for the on-chip test and debug logic.
TDO	JTAG	Serial test data output for the on-chip test logic.
TMS	JTAG	Controls test mode operations for the on-chip test and debug logic.

Table 4. Signal details (continued)

Signal	Module or Function	Description
EVTI	Nexus	EVTI is an input that is read on the negation of RESET to enable or disable the Nexus Debug port. After reset, the EVTI pin is used to initiate program synchronization messages or generate a breakpoint.
EVTO	Nexus	Output that provides timing to a development tool for a single watchpoint or breakpoint occurrence.
MCKO	Nexus	MCKO is a free running clock output to the development tools which is used for timing of the MDO and MSEO signals.
MDO[3:0]	Nexus	Trace message output to development tools. This pin also indicates the status of the crystal oscillator clock following a power-on reset, when MDO[0] is driven high until the crystal oscillator clock achieves stability and is then negated.
MSEO[1:0]	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins
BOOTCFG[1]	SIU – Configuration	The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode The following values are for BOOTCFG[0:1}: 0 Boot from internal flash memory 1 FlexCAN/eSCI boot
WKPCFG	SIU – Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of RSTOUT), and is sampled 4 clock cycles before the negation of the RSTOUT pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0: Weak pulldown applied to eTPU and eMIOS pins at reset 1: Weak pullup applied to eTPU and eMIOS pins at reset.
ETRIG[2:3]	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
IRQ[0:15]	SIU – External Interrupts	The IRQ[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the IRQ[0:15] pins as inputs to the IRQs.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)
$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)
Ψ_{JT} = thermal characterization parameter ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications”, Electronic Packaging and Production, pp. 53-58, March 1998.

Table 14. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Min	Typ	Max	Unit	Notes
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis[5]	—	60	—	mV	
9	Por5V_r	CC	C	Nominal POR for rising 5 V VDDREG supply	—	2.67	—	V	
9a	—	CC	C	Variation of POR for rising 5 V VDDREG supply	Por5V_r – 35%	Por5V_r	Por5V_r + 50%	V	
9b	Por5V_f	CC	C	Nominal POR for falling 5 V VDDREG supply	—	2.47	—	V	
9c	—	CC	C	Variation of POR for falling 5 V VDDREG supply	Por5V_f – 35%	Por5V_f	Por5V_f + 50%	V	

1 The limits will be reviewed after data collection from 3 different lots in a full production environment.

2 Using external ballast transistor.

3 Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.

4 LVI for falling supply is calculated as LVI rising - LVI hysteresis.

5 The internal voltage regulator can be disabled by tying the VDDREG pin to ground. When the internal voltage regulator is disabled, the LVI specifications are not applicable because all LVI monitors are disabled. POR specifications remain valid when the internal voltage regulator is disabled as long as VDDEH and VDD33 supplies are within the required ranges.

6 This parameter is the “inrush” current of the internal 3.3V regulator when it is turned on. This spec. is the current at which the regulator will go into current limit mode.

7 Lvi3p3 tracks DC target variation of internal Vdd33 regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum Vdd33 DC target respectively.

4.8 DC electrical specifications

Table 22. DC electrical specifications[1]

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14	—	1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62	—	3.6[3]	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0	—	5.25	V
V_{RC33}	SR	—	3.3 V external voltage[4]	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75[5]	—	5.25	V
V_{INDC}	SR	—	Analog input voltage[6]	—	V_{SSA} – 0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	V_{RL} differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA} – 0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage [7]	—	1.14	—	1.32	V
V_{FLASH}[8]	SR	—	Flash read voltage	—	4.75	—	5.25	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
				Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	—	Voltage regulator supply voltage[9]	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDEH}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDEH}	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDE}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDE}	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

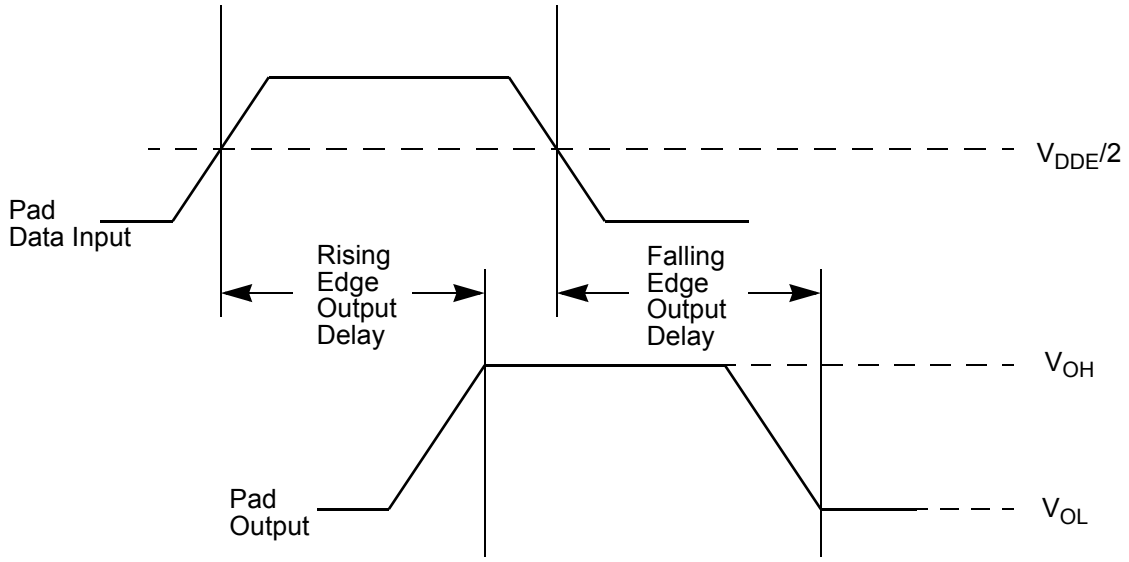


Figure 8. Pad output delay

4.16 AC timing

4.16.1 IEEE 1149.1 interface timing

Table 36. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% – 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	23	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	20	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns

Table 36. JTAG pin AC electrical characteristics[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	50	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	50	—	ns

1 JTAG timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 37 for functional specifications.

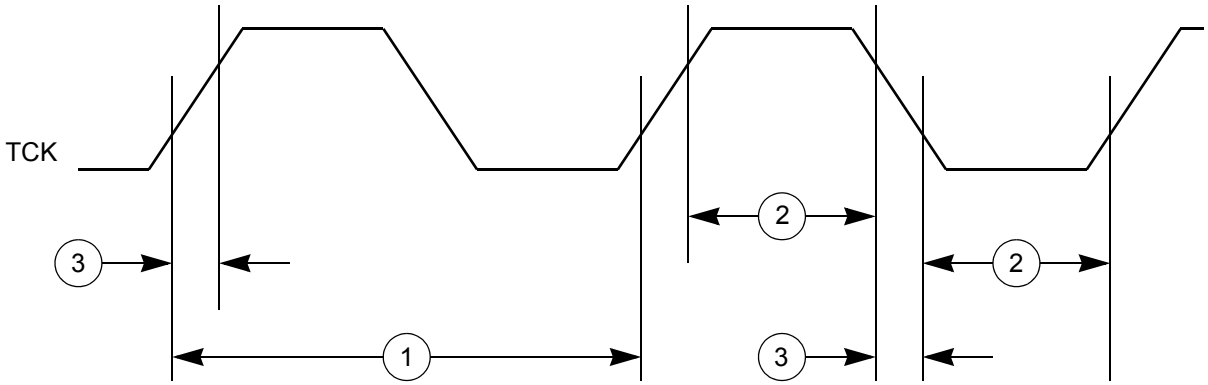


Figure 9. JTAG test clock input timing

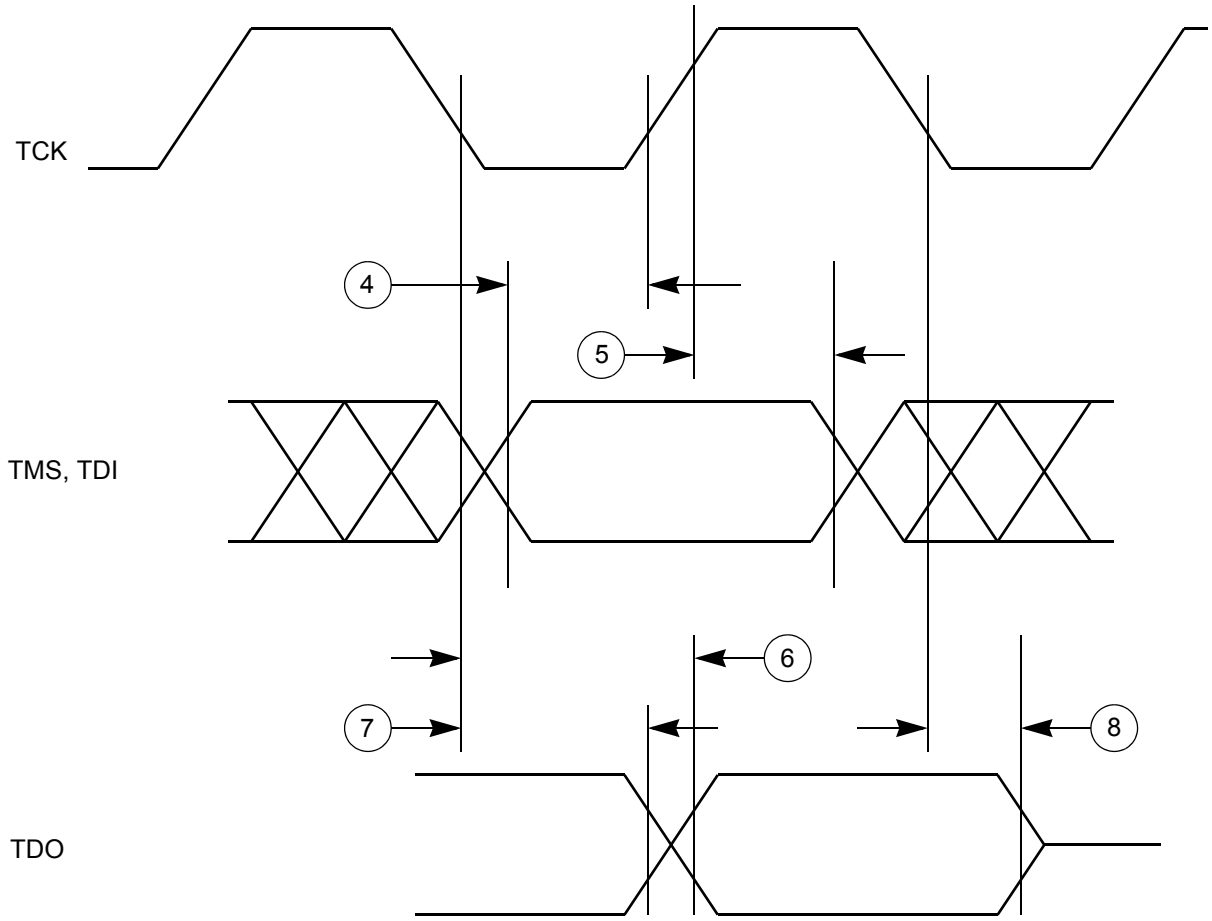


Figure 10. JTAG test access port timing

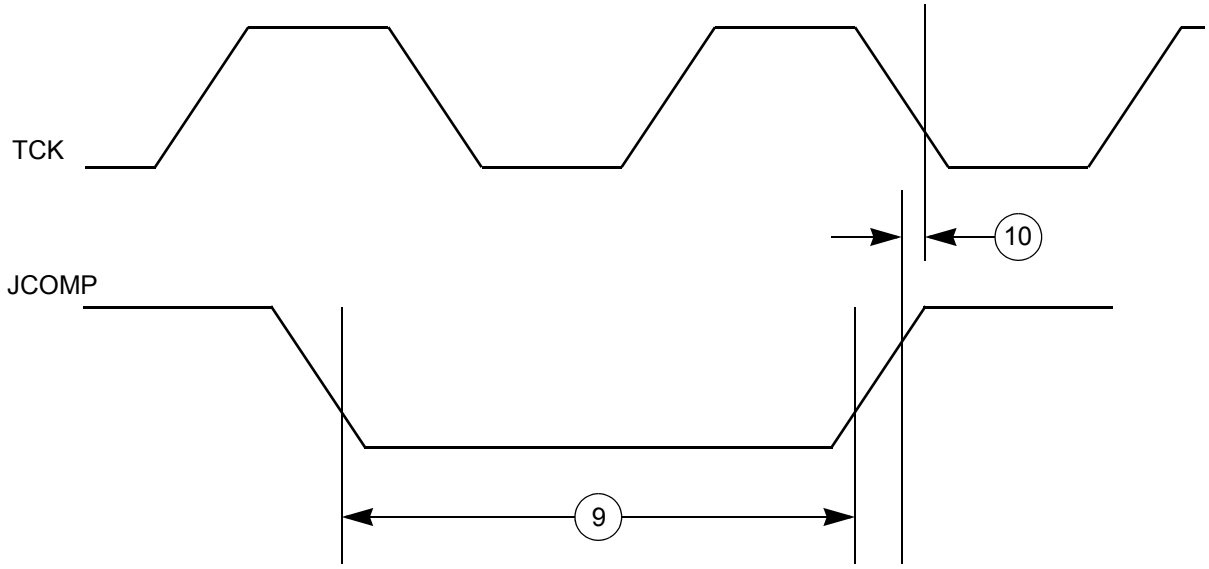


Figure 11. JTAG JCOMP timing

Table 37. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6,7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	t_{JOV}	CC	D	TCK Low to TDO Data Valid	10	20	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, T_A = TL to TH, and CL = 30 pF with DSC = 0b10.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.

3 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4 This may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

5 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

6 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

8 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

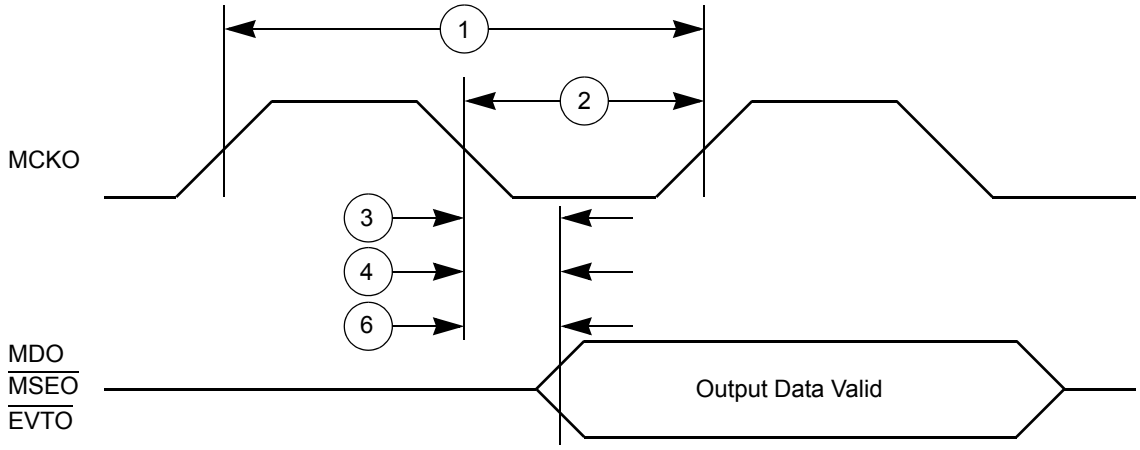


Figure 13. Nexus output timing

5 Packages

5.1 Package mechanical data

5.1.1 144 LQFP

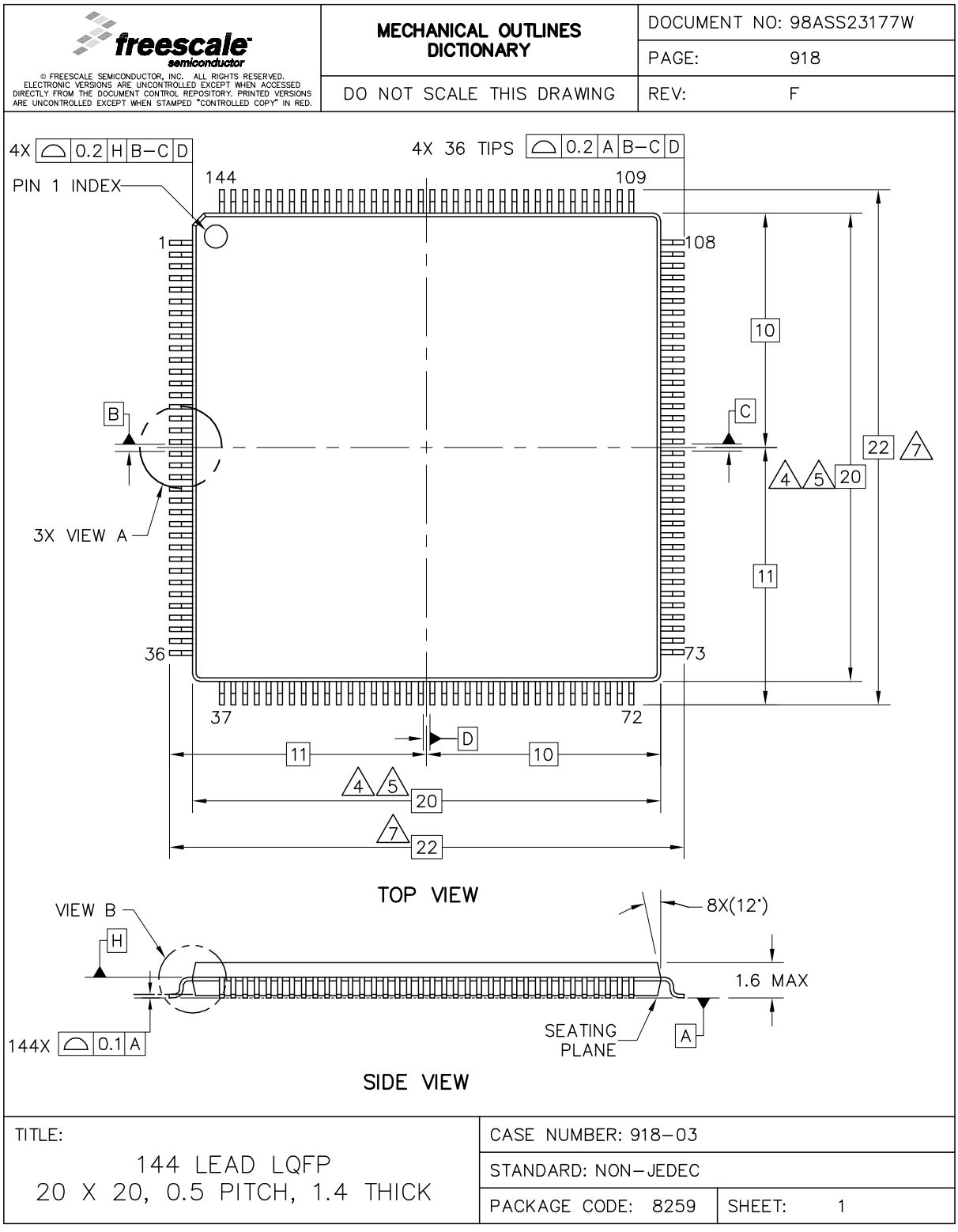


Figure 30. 144 LQFP package mechanical drawing (part 1)

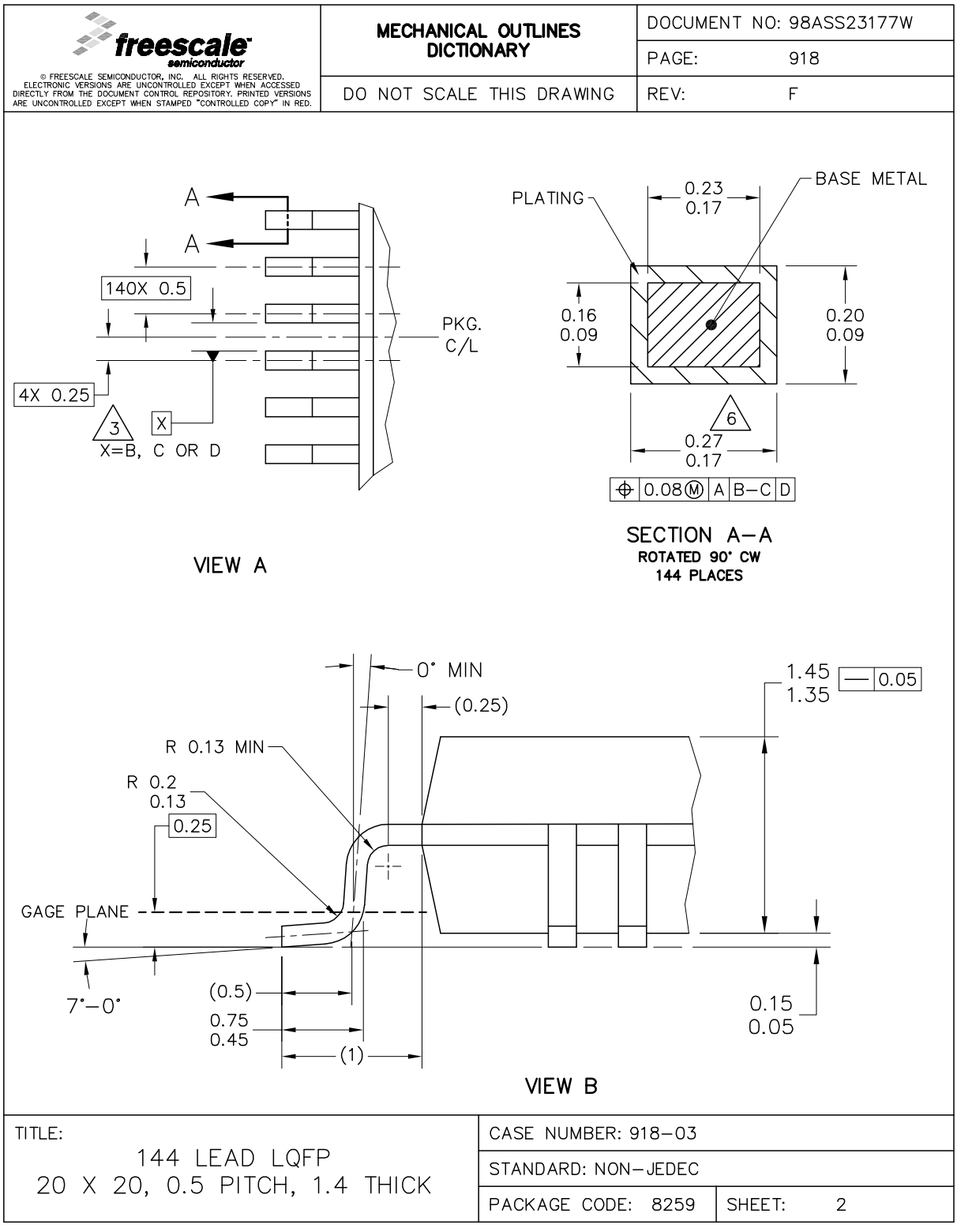


Figure 31. 144 LQFP package mechanical drawing (part 2)

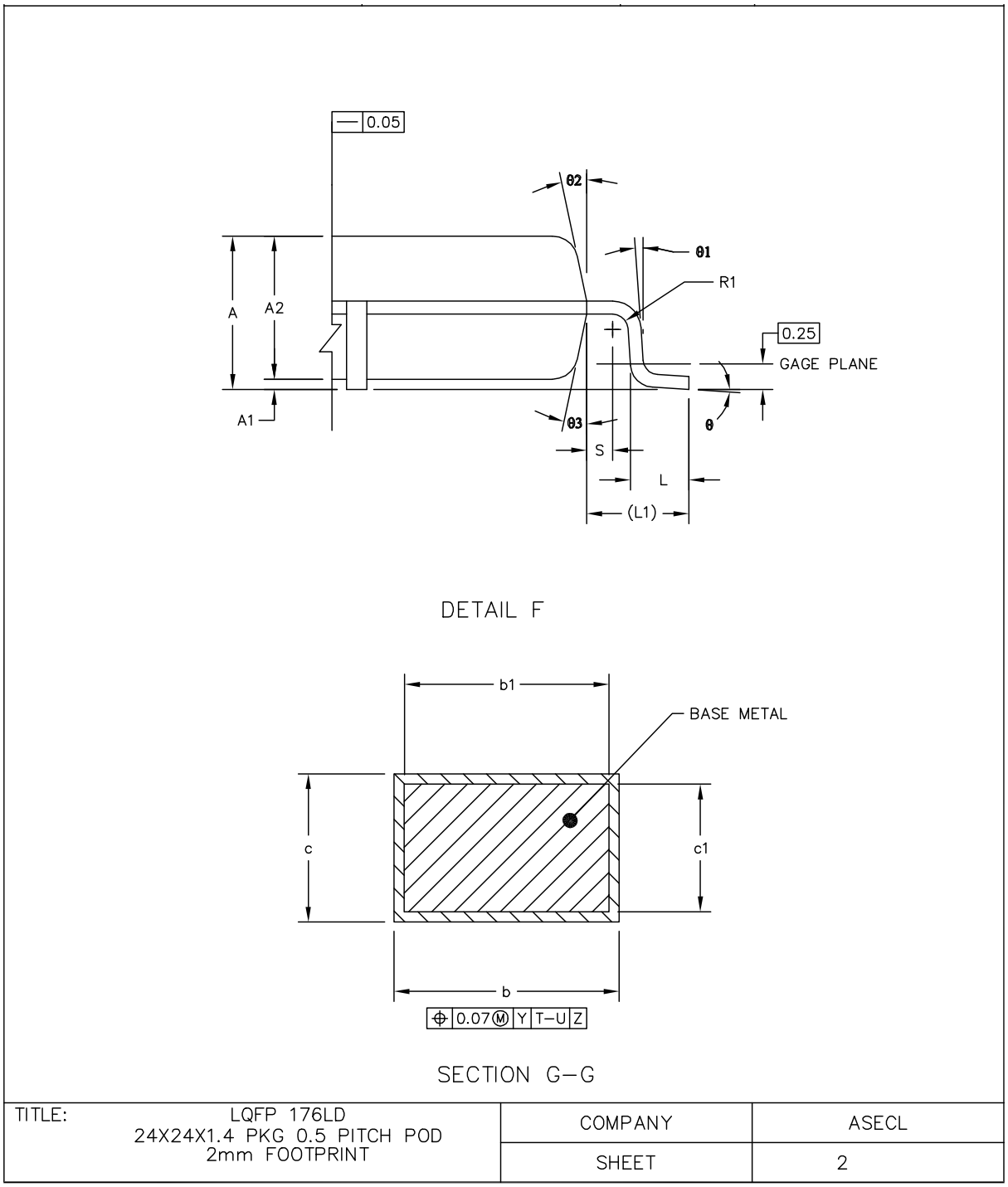


Figure 34. 176 LQFP package mechanical drawing (part 2)