Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.25V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5634mf2mlu80r

        - Allows selection of interrupt requests between external pins and DSPI
- Error correction status module (ECSM)
    - Configurable error-correcting codes (ECC) reporting
    - Single-bit error correction reporting
- On-chip flash memory
    - Up to 1.5 MB flash memory, accessed via a 64-bit wide bus interface
    - 16 KB shadow block
    - Fetch Accelerator
        - Provide single cycle flash access at 80 MHz
        - Quadruple 128-bit wide prefetch/burst buffers
        - Prefetch buffers can be configured to prefetch code or data or both
    - Censorship protection scheme to prevent flash content visibility
    - Flash divided into two independent arrays, allowing reading from one array while erasing/programming the other array (used for EEPROM emulation)
    - Memory block:
        - For MPC5634M: 18 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 10 × 128 KB)
        - For MPC5633M: 14 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 6 × 128 KB)
        - For MPC5632M: 12 blocks (4 × 16 KB, 2 × 32 KB, 2 × 64 KB, 4 × 128 KB)
    - Hardware programming state machine
- On-chip static RAM
    - For MPC5634M: 94 KB general purpose RAM of which 32 KB are on standby power supply
    - For MPC5633M: 64 KB general purpose RAM of which 32 KB are on standby power supply
    - For MPC5632M: 48 KB general purpose RAM of which 24 KB are on standby power supply
- Boot assist module (BAM)
    - Enables and manages the transition of MCU from reset to user code execution in the following configurations:
        - Execution from internal flash memory
        - Execution from external memory on the calibration bus
        - Download and execution of code via FlexCAN or eSCI
- Periodic interrupt timer (PIT)
    - 32-bit wide down counter with automatic reload
    - Four channels clocked by system clock
    - One channel clocked by crystal clock
    - Each channel can produce periodic software interrupt
    - Each channel can produce periodic triggers for eQADC queue triggering
    - One channel out of the five can be used as wake-up timer to wake device from low power stop mode
- System timer module (STM)
    - 32-bit up counter with 8-bit prescaler
    - Clocked from system clock
    - Four-channel timer compare hardware
    - Each channel can generate a unique interrupt request
    - Designed to address AUTOSAR task monitor function
- Software watchdog timer (SWT)
    - 32-bit timer
    - Clock by system clock or crystal clock
    - Can generate either system reset or non-maskable interrupt followed by system reset

- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8, 9, 12 or 13 bits
- Separately enabled transmitter and receiver
- LIN support
- DMA support
- Interrupt request support
- Programmable clock source: system clock or oscillator clock
- Support Microsecond Channel (Timed Serial Bus - TSB) upstream Version 1.0

- Two FlexCAN
  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    - Run-time access of entire memory map
    - Calibration
  - Support for data value breakpoints / watchpoints
    - Run-time access of entire memory map
    - Calibration

      Table constants calibrated using MMU and internal and external RAM

      Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation
  - On-chip regulator 5 V to 3.3 V for internal supplies
  - On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic
- Low-power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using Freescale protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the software watchdog timer

2.2.12 eMIOS

The eMIOS (Enhanced Modular Input Output System) module provides the functionality to generate or measure time events. The channels on this module provide a range of operating modes including the capability to perform dual input capture or dual output compare as well as PWM output.

The eMIOS provides the following features:

- 16 channels (24-bit timer resolution)
- For compatibility with other family members selected channels and timebases are implemented:
  - Channels 0 to 6, 8 to 15, and 23
  - Timebases A, B and C
- Channels 1, 3, 5 and 6 support modes:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
- Channels 2, 4, 11 and 13 support all the modes above plus:
  - Output Pulse Width Modulation Buffered (OPWMB)
- Channels 0, 8, 9, 10, 12, 14, 15, 23 support all the modes above plus:
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (set flag on both matches) (DAOC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width and Frequency Modulation Buffered (OPWFMB)
- Three 24-bit wide counter buses
  - Counter bus A can be driven by channel 23 or by the eTPU2 and all channels can use it as a reference
  - Counter bus B is driven by channel 0 and channels 0 to 6 can use it as a reference
  - Counter bus C is driven by channel 8 and channels 8 to 15 can use it as a reference
- Shared time bases with the eTPU2 through the counter buses
- Synchronization among internal and external time bases

2.2.13 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host

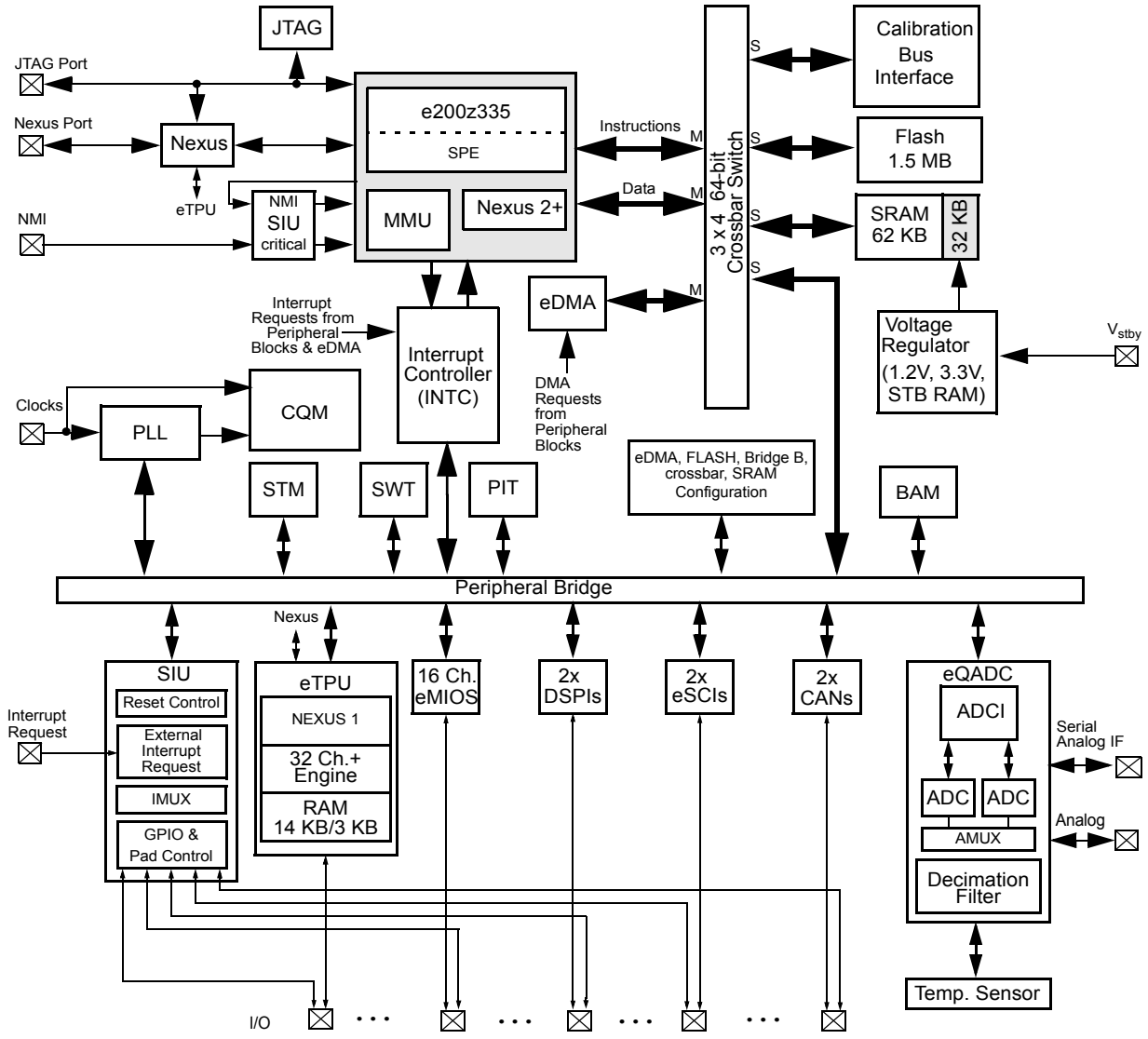


Figure 1. MPC5634M series block diagram

2.3.2 Block summary

Table 1 summarizes the functions of the blocks present on the MPC5634M series microcontrollers.

Table 1. MPC5634M series block summary

Block	Function
e200z3 core	Executes programs and interrupt handlers.
Flash memory	Provides storage for program code, constants, and variables
RAM (random-access memory)	Provides storage for program code, constants, and variables
Calibration bus	Transfers data across the crossbar switch to/from peripherals attached to the VertiCal connector

Table 1. MPC5634M series block summary (continued)

Block	Function
DMA (direct memory access)	Performs complex data movements with minimal intervention from the core
DSPI (deserial serial peripheral interface)	Provides a synchronous serial interface for communication with external devices
eMIOS (enhanced modular input-output system)	Provides the functionality to generate or measure events
eQADC (enhanced queued analog-to-digital converter)	Provides accurate and fast conversions for a wide range of applications
eSCI (serial communication interface)	Allows asynchronous serial communications with peripheral devices and other microcontroller units
eTPU (enhanced time processor unit)	Processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports the programmable frequency modulation of these clocks
INTC (interrupt controller)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
NPC (Nexus Port Controller)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
PIT (peripheral interrupt timer)	Produces periodic interrupts and triggers
Temperature sensor	Provides the temperature of the device as an analog value
SWT (Software Watchdog Timer)	Provides protection from runaway code
STM (System Timer Module)	Timer providing a set of output compare events to support AutoSAR and operating system tasks

3 Pinout and signal description

This section contains the pinouts for all production packages for the MPC5634M family of devices. Please note the following:

- Pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.
- Pins labeled “NIC” have no internal connection.

3.1 144 LQFP pinout

Figure 2 shows the pinout for the 144-pin LQFP.

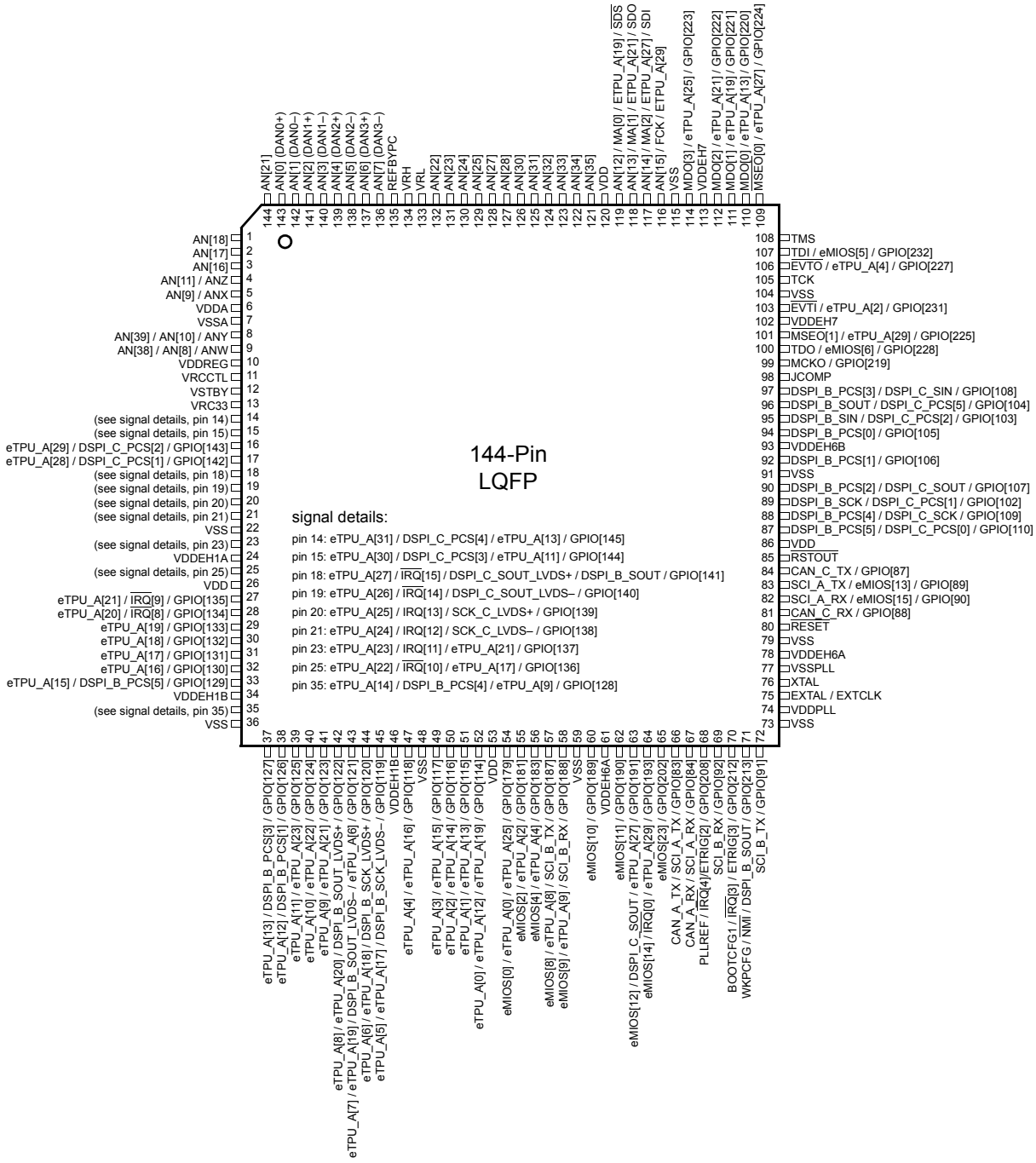
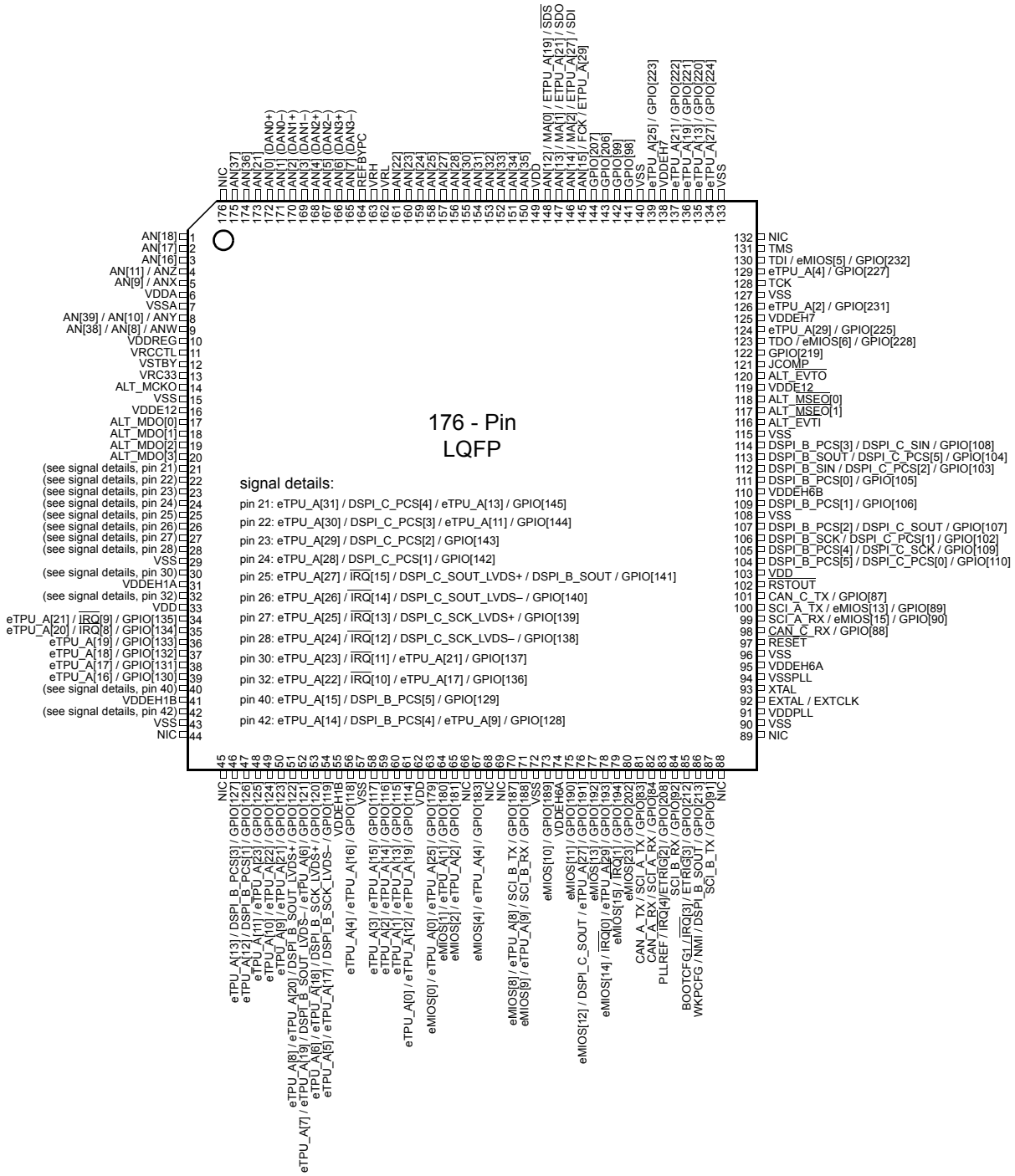


Figure 2. 144-pin LQFP pinout (top view; all 144-pin devices)

3.2 176 LQFP pinout (MPC5634M)

Figure 3 shows the 176-pin LQFP pinout for the MPC5634M (1536 KB flash memory).



Note: Pins marked “NIC” have no internal connection.

Figure 3. 176-pin LQFP pinout (MPC5634M; top view)

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
AN[13] MA[1] ETPU_A[21] SDO	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data Out	PCR[216]	011 010 100 000	I O O O	VDDEH7	I / –	AN[13] / –		118	147	B12
AN[14] MA[2] ETPU_A[27] SDI	Single Ended Analog Input Mux Address ETPU_A Ch. eQADC Serial Data In	PCR[217]	011 010 100 000	I O O I	VDDEH7	I / –	AN[14] / –		117	146	C12
AN[15] FCK ETPU_A[29]	Single Ended Analog Input eQADC Free Running Clock ETPU_A Ch.	PCR[218]	011 010 000	I O O	VDDEH7	I / –	AN[15] / –		116	145	C13
AN[16]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		3	3	C6
AN[17]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		2	2	C4
AN[18]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		1	1	D5
AN[21]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		144	173	B4
AN[22]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		132	161	B8
AN[23]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		131	160	C9
AN[24]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		130	159	D8
AN[25]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		129	158	B9
AN[27]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		128	157	A10
AN[28]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		127	156	B10
AN[30]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		126	155	D9
AN[31]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		125	154	D10
AN[32]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		124	153	C10
AN[33]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		123	152	C11
AN[34]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		122	151	C5
AN[35]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		121	150	D11
AN[36]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	174[7]	F4[8]
AN[37]	Single Ended Analog Input	—	—	I	VDDA	I / –	AN[x] / –		—	175[7]	E3[8]

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.			
									144 LQFP	176 LQFP	208 MAPBGA
eTPU_A[7] eTPU_A[19] DSPI_B_SOUT_LVDS- eTPU_A[6] GPIO[121]	eTPU_A Ch. eTPU_A Ch. DSPI_B Data Output LVDS- eTPU_A Ch. GPIO	PCR[121]	0001 0010 0100 1000 0000	I/O O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		43	52	K3
eTPU_A[8] eTPU_A[20] DSPI_B_SOUT_LVDS+ GPIO[122]	eTPU_A Ch. eTPU_A Ch. DSPI_B Data Output LVDS+ GPIO	PCR[122]	001 010 100 000	I/O O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		42	51	N1
eTPU_A[9] eTPU_A[21] GPIO[123]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[123]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		41	50	M2
eTPU_A[10] eTPU_A[22] GPIO[124]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[124]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		40	49	M1
eTPU_A[11] eTPU_A[23] GPIO[125]	eTPU_A Ch. eTPU_A Ch. GPIO	PCR[125]	01 10 00	I/O O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		39	48	L2
eTPU_A[12] DSPI_B_PCS[1] GPIO[126]	eTPU_A Ch. DSPI_B Periph Chip Select GPIO	PCR[126]	01 10 00	I/O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		38	47	L1
eTPU_A[13] DSPI_B_PCS[3] GPIO[127]	eTPU_A Ch. DSPI_B Periph Chip Select GPIO	PCR[127]	01 10 00	I/O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		37	46	J4
eTPU_A[14] DSPI_B_PCS[4] eTPU_A[9] GPIO[128]	eTPU_A Ch. DSPI_B Periph Chip Select eTPU_A Ch. GPIO	PCR[128]	001 010 100 000	I/O O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		35	42	J3
eTPU_A[15] DSPI_B_PCS[5] GPIO[129]	eTPU_A Ch. DSPI_B Periph Chip Select GPIO	PCR[129]	01 10 00	I/O O I/O	VDDEH1b Medium	– / WKPCFG	– / WKPCFG		33	40	K2
eTPU_A[16] GPIO[130]	eTPU_A Ch. GPIO	PCR[130]	01 00	I/O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		32	39	K1
eTPU_A[17] GPIO[131]	eTPU_A Ch. GPIO	PCR[131]	01 00	I/O I/O	VDDEH1b Slow	– / WKPCFG	– / WKPCFG		31	38	H3

Table 2. MPC563xM signal properties (continued)

Name	Function[1]	Pad Config. Register (PCR)[2]	PCR PA Field[3]	I/O Type	Voltage[4] / Pad Type	Reset State[5]	Function / State After Reset[6]	Pin No.		
								144 LQFP	176 LQFP	208 MAPBGA
VSS	Ground	—	—	–	VSS0	I / –	—	22, 36, 48, 59, 73, 79, 91, 104, 115	15, 29, 43, 57, 72, 90, 96, 108, 115[7], 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, N4, N13, P3, P14, R2, R15, T1, T16
VDDEH1A[36] VDDEH1B[36]	I/O Supply Input	—	—	I	VDDEH1[37] (3.3V – 5.0V)	I / –	—	24, 34, 46	31, 41 55	K4
VDDE5	I/O Supply Input	—	—	I	VDDE5	I / –	—	—	—	T13
VDDEH6a[38, 39] VDDEH6b[39]	I/O Supply Input	—	—	I	VDDEH6 (3.3V – 5.0V)	I / –	—	78, 93, 61	95, 110, 74	—
VDDEH6	I/O Supply Input	—	—	I	VDDEH6	I / –	—	—	—	F13
VDDEH7	I/O Supply Input	—	—	I	VDDEH7[40] (3.3V – 5.0V)	I / –	—	102, 113	125, 138	D12
VDDE7[41]	I/O Supply Input	—	—	I	VDDE7 (3.3V)	I / –	—	—	16, 119[7]	E13, P6

1 For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted.

2 Values in this column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.

3 The Pad Configuration Register (PCR) PA field is used by software to select pin function.

4 The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (–10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/– 10%).

5 Terminology is O — output, I — input, Up — weak pull up enabled, Down — weak pull down enabled, Low — output driven low, High — output driven high. A dash for the function in this column denotes that both the input and output buffer are turned off.

6 Function after reset of GPI is general purpose input. A dash for the function in this column denotes that both the input and output buffer are turned off.

7 Not available on 1 MB version of 176-pin package.

8 Not available on 1 MB version of 208-pin package.

[9] The GPIO functions on GPIO[206] and GPIO[207] can be selected as trigger functions in the SIU for the ADC by making the proper selections in the SIU_ETISR and SIU_ISEL3 registers in the SIU.

[10] Some signals in this section are available only on calibration package.

[11] These pins are only available in the 496 CSP/MAPBGA calibration/development package.

[12] On the calibration package, the Nexus function on this pin is enabled when the NEXUSCFG pin is high and Nexus is configured to full port mode. On the 176-pin and 208-pin packages, the Nexus function on this pin is enabled permanently. Do not connect the Nexus MDO or MSEO pins directly to a power supply or ground.

[13] In the calibration package, the I/O segment containing this pin is called VDDE12.

[14] 208-ball BGA package only

[15] When configured as Nexus (208-pin package or calibration package with NEXUSCFG=1), and JCOMP is asserted during reset, MDO[0] is driven high until the crystal oscillator becomes stable, at which time it is then negated.

[16] The function of this pin is Nexus when NEXUSCFG is high.

[17] High when the pin is configured to Nexus, low otherwise.

[18] O/Low for the calibration with NEXUSCFG=0; I/Up otherwise.

[19] ALT_ADDR/Low for the calibration package with NEXUSCFG=0; $\overline{\text{EVTI}}$/Up otherwise.

[20] In 176-pin and 208-pin packages, the Nexus function is disabled and the pin/ball has the secondary function

[21] This signal is not available in the 176-pin and 208-pin packages.

[22] The primary function is not selected via the PA field when the pin is a Nexus signal. Instead, it is activated by the Nexus controller.

[23] TDI and TDO are required for JTAG operation.

[24] The primary function is not selected via the PA field when the pin is a JTAG signal. Instead, it is activated by the JTAG controller.

[25] The function and state of the CAN_A and eSCI_A pins after execution of the BAM program is determined by the BOOTCFG1 pin.

[26] Connect an external 10K pull-up resistor to the SCI_A_RX pin to ensure that the pin is driven high during CAN serial boot.

[27] For pins AN[0:7], during and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

[28] ETPUA[24:29] are input and output. The input muxing is controlled by SIU_ISEL8 register.

[29] eTPU_A[25] is an output only function.

[30] Only the output channels of eTPU[8:9] are connected to pins.

[31] The function after reset of the XTAL pin is determined by the value of the signal on the PLLCFG[1] pin. When bypass mode is chosen XTAL has no function and should be grounded.

[32] The function after reset of the EXTAL_EXTCLK pin is determined by the value of the signal on the PLLCFG[1] pin. If the EXTCLK function is chosen, the valid operating voltage for the pin is 1.62 V to 3.6 V. If the EXTAL function is chosen, the valid operating voltage is 3.3 V.

[33] VSSPLL and VSSREG are connected to the same pin.

[34] This pin is shared by two pads: VDDA_AN, using pad_vdde_hv, and VDDA_DIG, using pad_vdde_int_hv.

[35] This pin is shared by two pads: VSSA_AN, using pad_vsse_hv, and VSSA_DIG, using pad_vsse_int_hv.

[36] VDDEH1A, VDDEH1B, and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[37] LVDS pins will not work at 3.3 V.

[38] The VDDEH6 segment may be powered from 3.0 V to 5.0 V for mux address or SSI functions, but must meet the VDDA specifications of 4.5 V to 5.25 V for analog input function.

Table 16. Network 1 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	4 x 2.35	4 x 4.7	4 x 6.35	µF	X7R, -50%/+35%
		1 x 5	1 x 10	1 x 13.5	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 50	4 x 100	4 x 135	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	6.12	6.8	7.48	Ω	±10%
Emitter resistor	R_E	0	0	0	Ω	Not required (short)

Table 17. Network 2 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	3 x 2.35	3 x 4.7	3 x 6.35	µF	X7R, -50%/+35%
		1 x 5	1 x 10	1 x 13.5	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 50	4 x 100	4 x 135	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	9	10	11	Ω	±10%
Emitter resistor	R_E	0.252	0.280	0.308	Ω	Not required (short)

The following component configuration is acceptable when using the BCP68 transistor, however, is not recommended for new designs. Either option 1 or option 2 should be used for new designs. This option should not be used with the NJD2873 transistor.

Table 18. Network 3 component values

Component	Symbol	Minimum	Typical	Maximum	Units	Comment
Transistor emitter bypass capacitance	C_E	4 x 3.4	4 x 6.8	4 x 9.18	µF	X7R, -50%/+35%
	R_{ESR}	5		50	mΩ	Equivalent ESR of C_E capacitors
MCU decoupling capacitor	C_D	4 x 110	4 x 220	4 x 297	nF	X7R, -50%/+35%
Base "snubber" capacitor	C_B	1.1	2.2	2.97	µF	X7R, -50%/+35%
Base "snubber" resistor	R_B	13.5	15	16.5	Ω	±10%
Emitter resistor	R_E	0	0	0	Ω	Not required (short)

4.8 DC electrical specifications

Table 22. DC electrical specifications[1]

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14	—	1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62	—	3.6[3]	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0	—	5.25	V
V_{RC33}	SR	—	3.3 V external voltage[4]	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75[5]	—	5.25	V
V_{INDC}	SR	—	Analog input voltage[6]	—	V_{SSA} – 0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	V_{RL} differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA} – 0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage [7]	—	1.14	—	1.32	V
V_{FLASH}[8]	SR	—	Flash read voltage	—	4.75	—	5.25	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
				Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	—	Voltage regulator supply voltage[9]	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDEH}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDEH}	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}–0.3	—	0.35*V_{DDE}	V
		P		hysteresis disabled	V_{SS}–0.3	—	0.40*V_{DDE}	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[10,11,12,13,17]	I_{OH_LS} = 0.5 mA Min V_{DDEH} = 4.75 V	2.1	—	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[17]	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	V
I_{DD}+I_{DDPLL}[19]	CC	P	Operating current 1.2 V supplies	V_{DD} = 1.32 V, 80 MHz	—	—	195	mA
	CC	P		V_{DD} = 1.32 V, 60 MHz	—	—	135	
	CC	P		V_{DD} = 1.32 V, 40 MHz	—	—	98	
I_{DDSTBY}	CC	T	Operating current 1 V supplies	T_J = 25 °C	—	—	80	µA
	CC	T		T_J = 55 °C	—	—	100	µA
$I_{DDSTBY150}$	CC	P	Operating current	T_J=150 °C	—	—	700	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current @ 1.32 V	Slow mode[20]	—	—	50	mA
		C		Stop mode[21]	—	—	50	
I_{DD33}	CC	T	Operating current 3.3 V supplies @ 80 MHz	V_{RC33}[4,22]	—	—	70	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies @ 80 MHz	V_{DDA}	—	—	30	mA
		P		Analog reference supply current	—	—	1.0	
		C		V_{DDREG}	—	—	70	

Table 22. DC electrical specifications[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					min	typ	max	
I_{DDH1} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[23] supplies @ 80 MHz	V_{DDEH1}	—	—	See note [23]	mA
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[24]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.25 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[24]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDEH}= 3.0–3.6 V[10], pad_multv_hv, all process corners, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[25]	—	–2.5	—	2.5	µA
I_{IC}	CC	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	CC	P	Analog input current, channel off, AN[0:7], AN38, AN39[26]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins (ANx)[26]	—	–150	—	150	

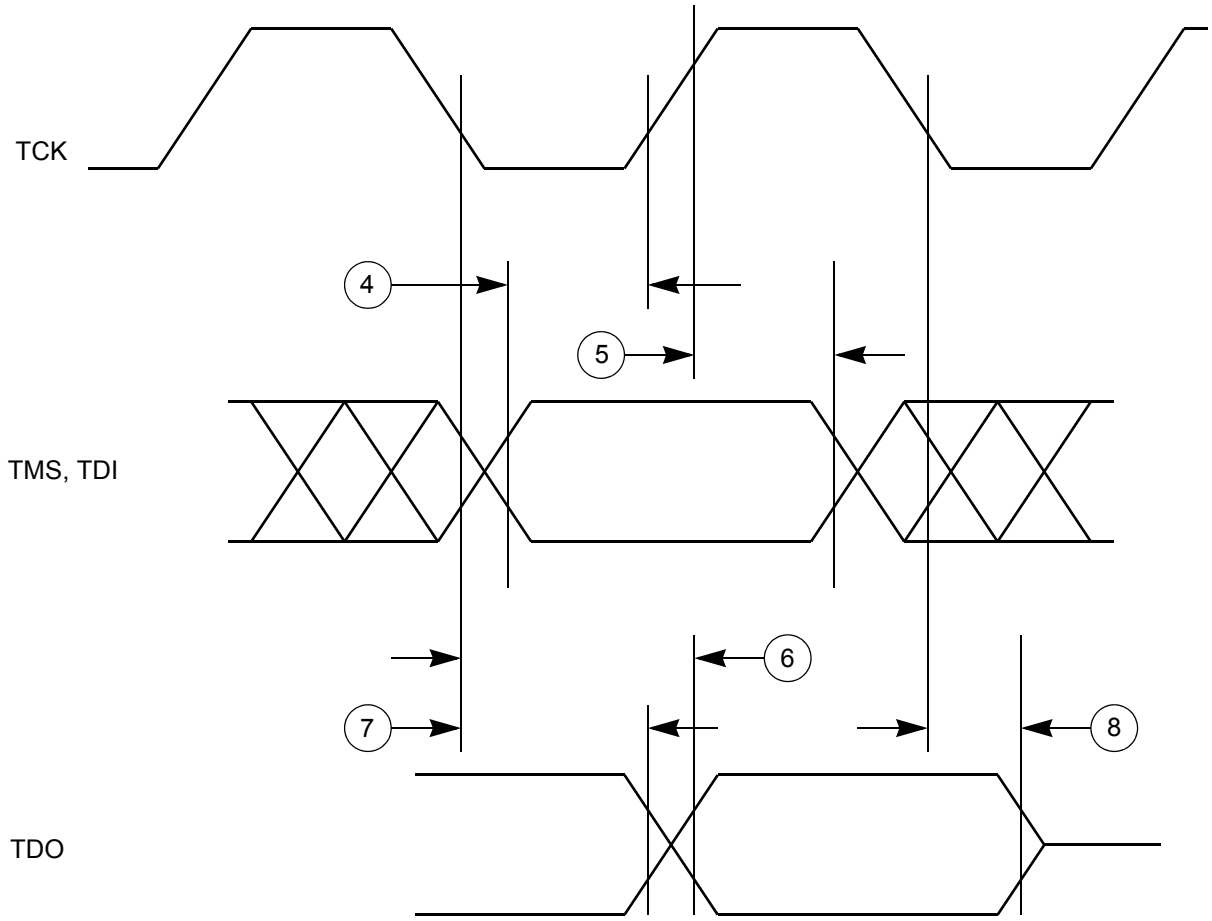


Figure 10. JTAG test access port timing

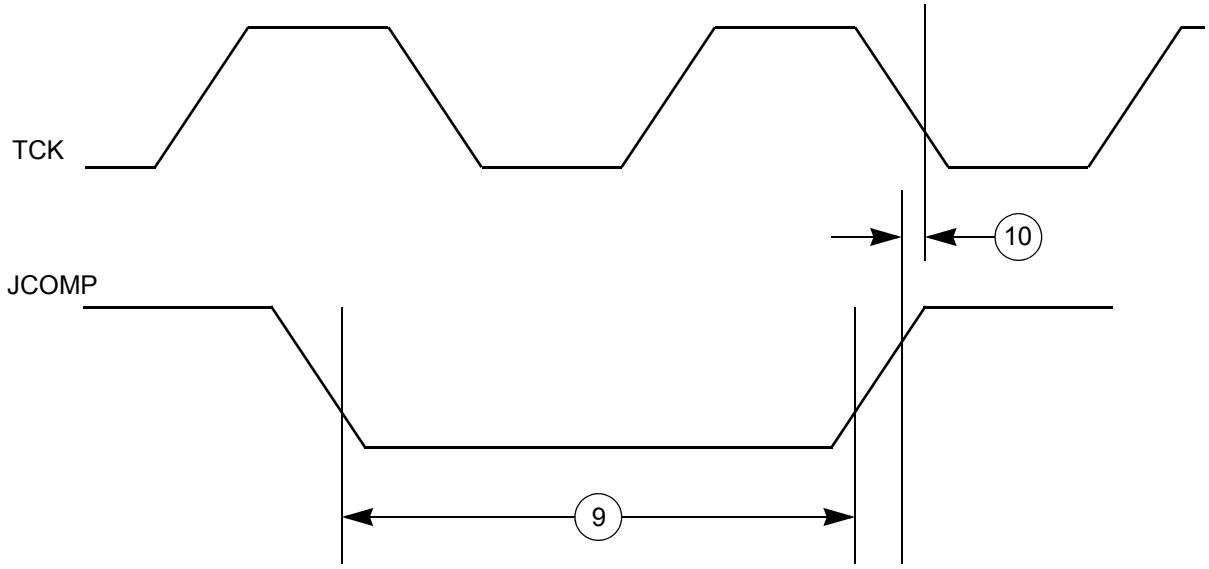


Figure 11. JTAG JCOMP timing

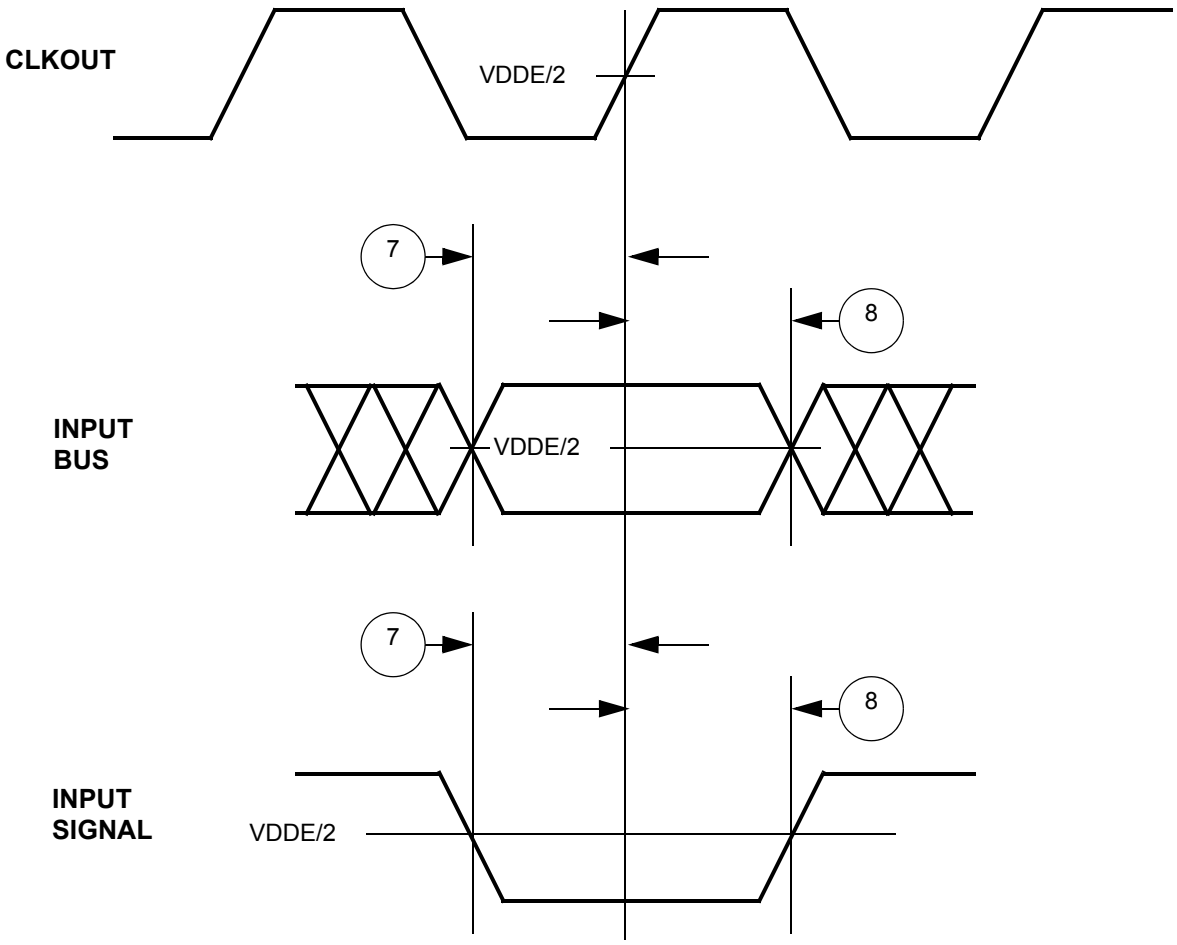


Figure 18. Synchronous input timing

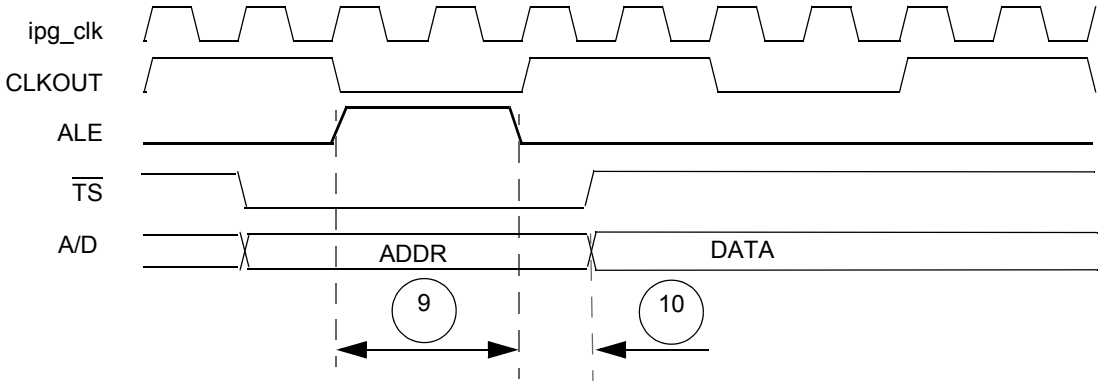


Figure 19. ALE signal timing

Table 40. DSPI timing[1,2] (continued)

#	Symbol		C	Characteristic	40 MHz		60 MHz		80 MHz		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{HI}	CC	Data Hold Time for Inputs								
			D	Master (MTFE = 0)	–4	—	–4	—	–4	—	ns
			D	Slave	7	—	7	—	7	—	
			D	Master (MTFE = 1, CPHA = 0)[7]	45	—	25	—	21	—	
			D	Master (MTFE = 1, CPHA = 1)	–4	—	–4	—	–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)								
			D	Master (MTFE = 0)	—	6	—	6	—	6	ns
			D	Slave	—	25	—	25	—	25	
			D	Master (MTFE = 1, CPHA=0)	—	45	—	25	—	21	
			D	Master (MTFE = 1, CPHA=1)	—	6	—	6	—	6	
12	t_{HO}	CC	Data Hold Time for Outputs								
			D	Master (MTFE = 0)	–5	—	–5	—	–5	—	ns
			D	Slave	5.5	—	5.5	—	5.5	—	
			D	Master (MTFE = 1, CPHA = 0)	8	—	4	—	3	—	
			D	Master (MTFE = 1, CPHA = 1)	–5	—	–5	—	–5	—	

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at VDDEH = 3.0–5.25 V, TA = TL to TH, and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 62 MHz parts allow for a 60 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two MPC5634M devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

Table 43. Revision history (continued)

Revision	Date	Description of Changes
Rev 9	05/2012	In Section 4.6.1, “Regulator example • Updated ,Figure 7 “Core voltage regulator controller external components preferred configuration” to show R_C, R_B, R_E, C_C, C_B, C_E, C_D and C_{REG}. • Added Table 15 “Required external PMC component values”, Table 16 “Network 1 component values”, Table 17 “Network 2 component values” and Table 18 “Network 3 component values”. Updated Table 1: Number of eMIOS channels changed from ‘8’ to ‘16’ for MPC5632M. In Section 4.2, “Maximum ratings, Table 7 • V_{FLASH} maximum value changed from 3.6V to 5.5V and changed table note3 to: “The V_{FLASH} supply is connected to V_{DDEH}” • Removed table note 4, “Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V +10%” In Section 4.12, “eQADC electrical characteristics: • Added note. • In Table 29, additional five parameters added (SNR, THD, SFDR, SINAD and ENOB) and added footnotes # 9,10 and 11.