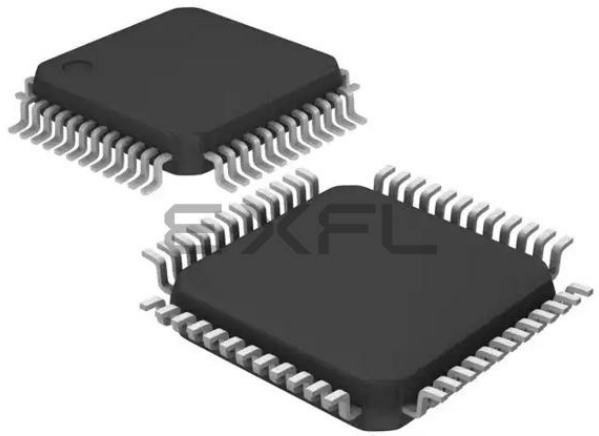

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1517jbd48e

- Single power supply 2.4 V to 3.6 V.
- Temperature range −40 °C to +105 °C.
- Available as LQFP100, LQFP64, and LQFP48 packages.

3. Applications

- Motor control
- Motion drives
- Digital power supplies
- Industrial and medical
- Solar inverters
- Home appliances
- Building and factory automation

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1549JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1549JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1549JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1548JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1548JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1519JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1519JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1518JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1518JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

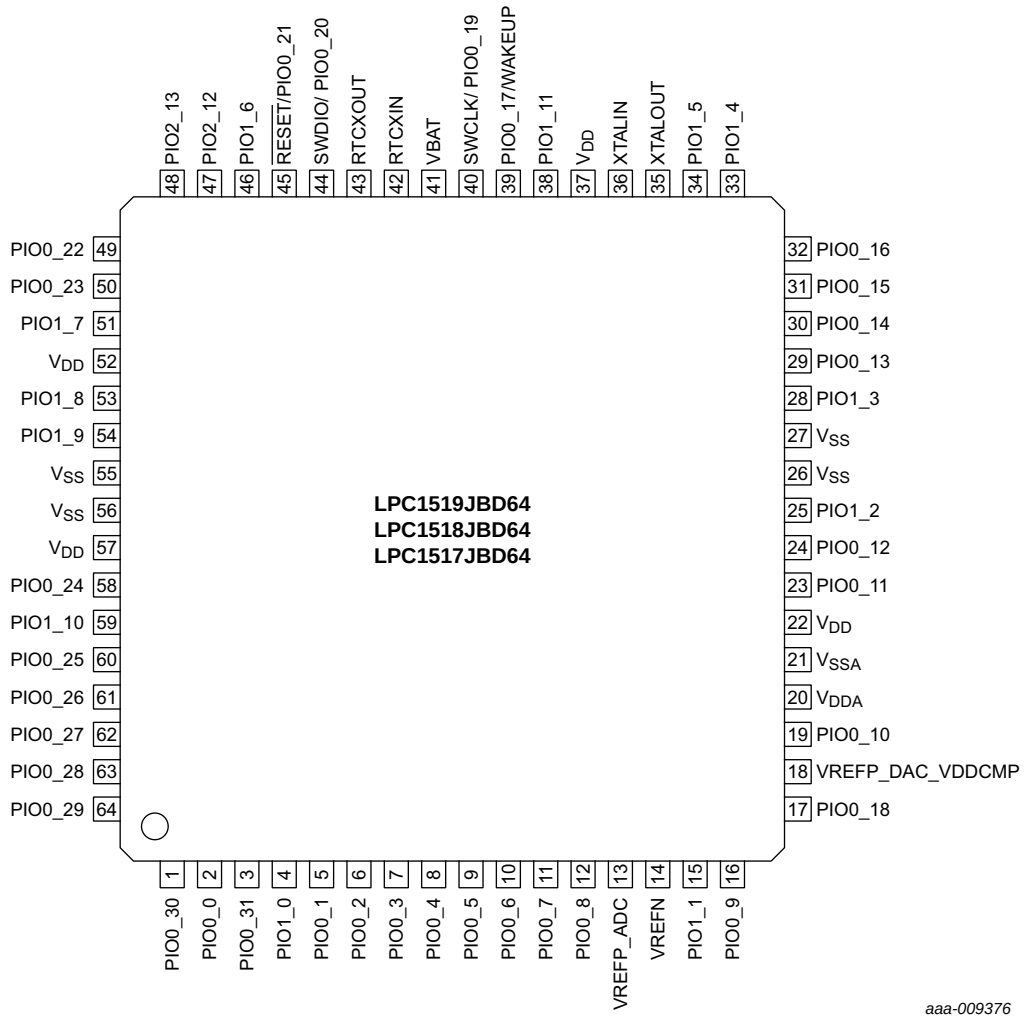


Fig 7. LQFP64 pin configuration (without USB)

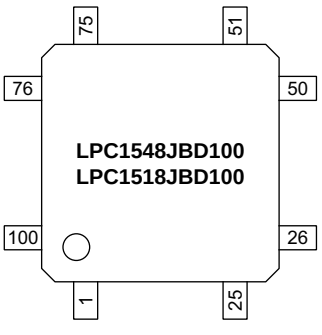


Fig 8. LQFP100 pin configuration

8.9 Nested Vectored Interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.9.1 Features

- Nested Vectored Interrupt Controller that is an integral part of the ARM Cortex-M3.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- The NVIC supports 47 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Support for NMI.
- ARM Cortex-M3 Vector table offset register VTOR implemented.

8.9.2 Interrupt sources

Typically, each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.10 IOCON block

The IOCON block configures the electrical properties of the pins such as pull-up and pull-down resistors, hysteresis, open-drain modes and input filters.

Remark: The pin function and whether the pin operates in digital or analog mode are entirely under the control of the switch matrix.

Enabling an analog function through the switch matrix disables the digital pad. However, the internal pull-up and pull-down resistors as well as the pin hysteresis must be disabled to obtain an accurate reading of the analog input.

8.10.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All pins (except PIO0_22 and PIO0_23) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable (on/off) 10 ns glitch filter on 36 pins (PIO0_0 to PIO0_17, PIO0_25 to PIO0_31, PIO1_0 to PIO1_10). The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.
- Digital filter with programmable filter constant on all pins.

8.10.2 Standard I/O pad configuration

Figure 11 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter configurable on all pins
- Digital input: Input glitch filter enabled/disabled on select pins
- Analog input

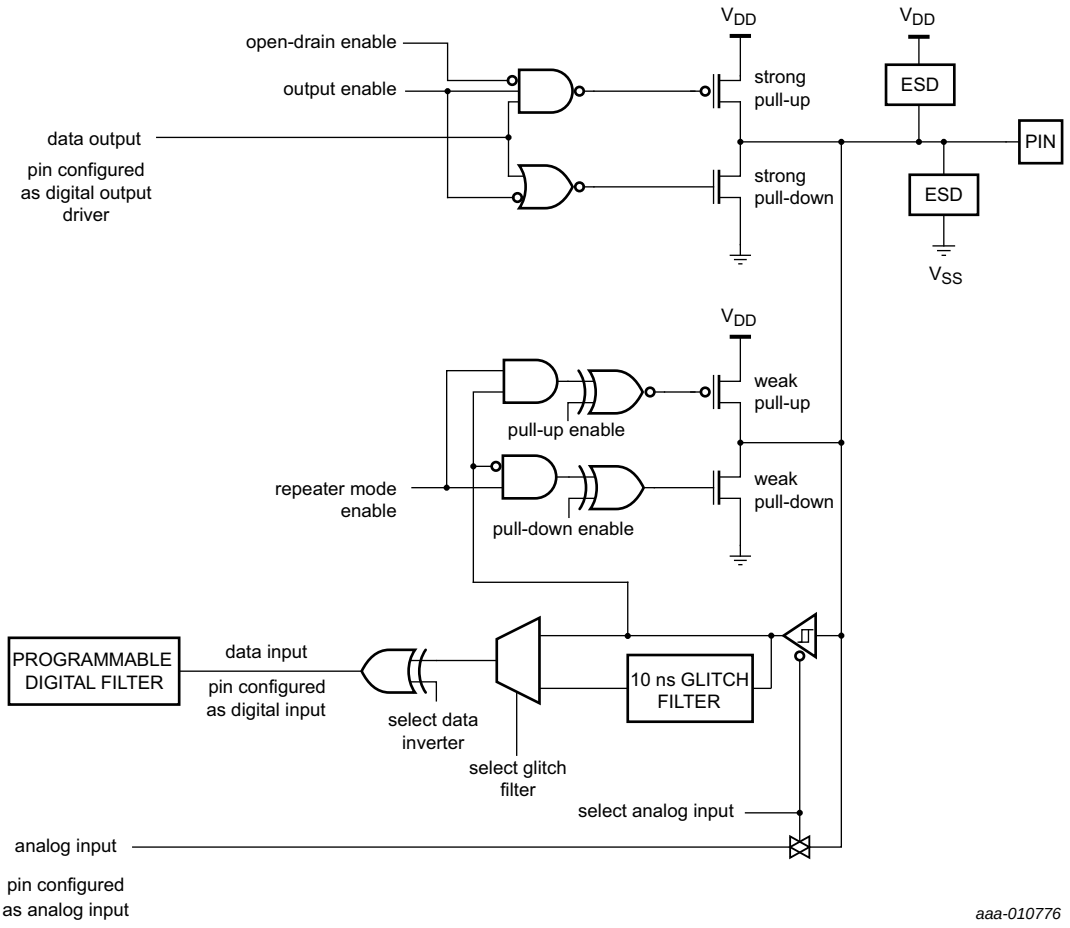


Fig 11. Standard I/O pin configuration

8.11 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the ADC or analog comparator inputs can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.12 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function through the switch matrix are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC15xx use accelerated GPIO functions.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.12.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.13 Pin interrupt/pattern match engine (PINT)

The pin interrupt block configures up to eight pins from the digital pins on ports 1 and 2 for providing eight external interrupts connected to the NVIC. The input multiplexer block is used to select the pins.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin on ports 0 and 1 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.13.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU.
  - The pattern match engine does not facilitate wake-up.

8.18 USART0/1/2

Remark: All USART functions are movable functions and are assigned to pins through the switch matrix. Do not connect USART functions to the open-drain pins PIO0_22 and PIO0_23.

Interrupts generated by the USART peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled.

8.18.1 Features

- Maximum bit rates of 4.5 Mbit/s in asynchronous mode, 15 Mbit/s in synchronous mode master mode, and 18 Mbit/s in synchronous slave mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep and power-down modes.
- Special operating mode allows operation at up to 9600 baud using the 32 kHz RTC oscillator as the UART clock. This mode can be used while the device is in Deep-sleep or Power-down mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

8.19 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix. Do not connect SPI functions to the open-drain pins PIO0_22 and PIO0_23.

- When the ADC is accurately calibrated, the internal voltage reference can be used to measure the power supply voltage. This requires calibration by recording the ADC code of the internal voltage reference at different power supply levels yielding a different ADC code value for each supply voltage level. In a particular application, the internal voltage reference can be measured and the actual power supply voltage can be determined from the stored calibration values. The calibration values can be stored in the EEPROM for easy access.

After power-up, the internal voltage reference must be allowed to settle to its stable value before it can be used as an ADC reference voltage input.

For an accurate measurement of the internal voltage reference by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.29 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.29.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

8.30 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.30.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WWDT is clocked by the dedicated watchdog oscillator (WDOsc) running at a fixed frequency.

8.34 Clock generation

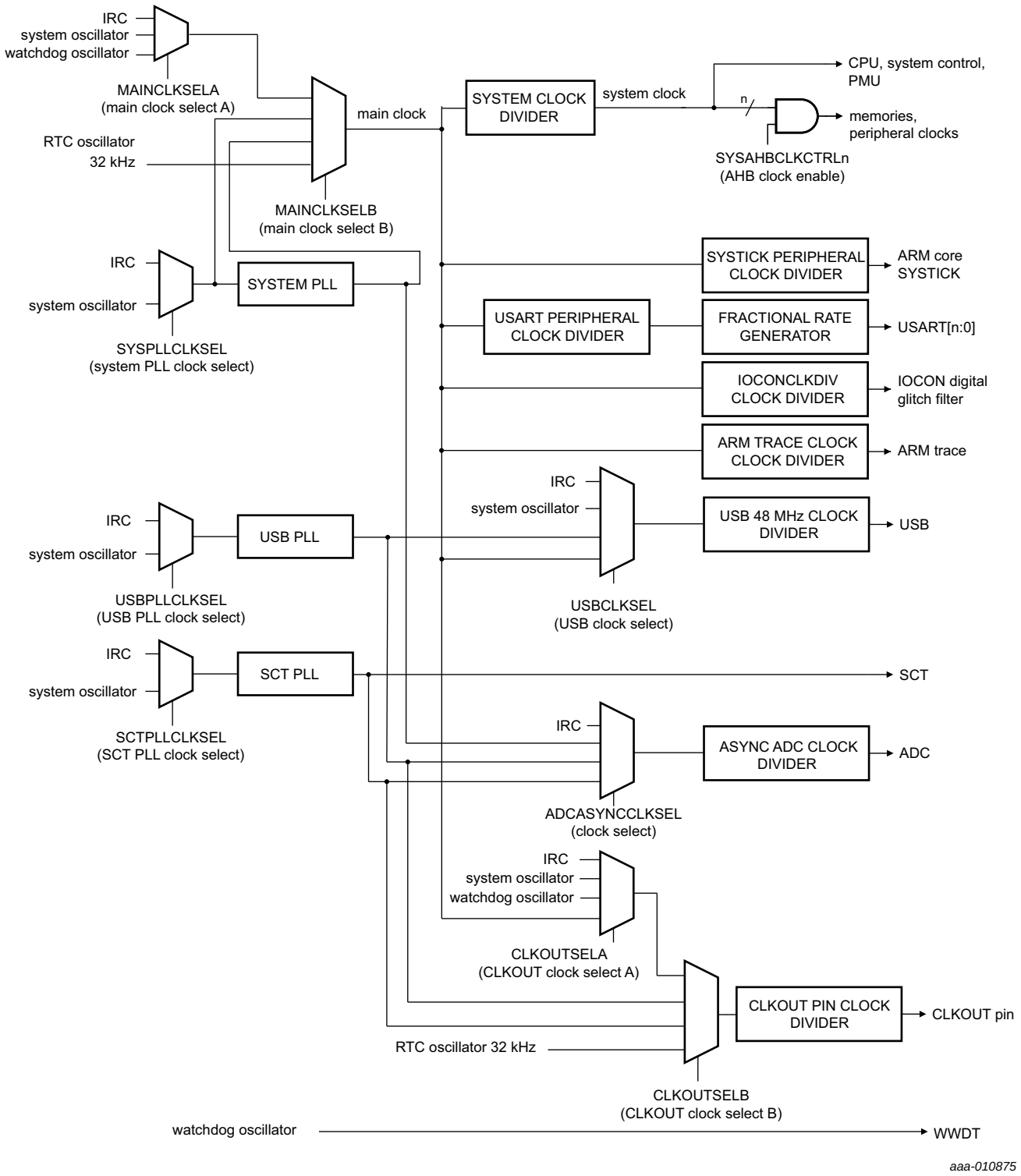


Fig 14. Clock generation

8.41 System control

8.41.1 Reset

Reset has four sources on the LPC15xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

The $\overline{\text{RESET}}$ pin is operational in active, sleep, deep-sleep, and power-down modes if the $\overline{\text{RESET}}$ function is selected through the switch matrix for pin PIO0_21 (this is the default). A LOW-going pulse as short as 50 ns executes the reset and thereby wakes up the part to its active state. The $\overline{\text{RESET}}$ pin is not functional in Deep power-down mode and must be pulled HIGH externally while the part is in Deep power-down mode.

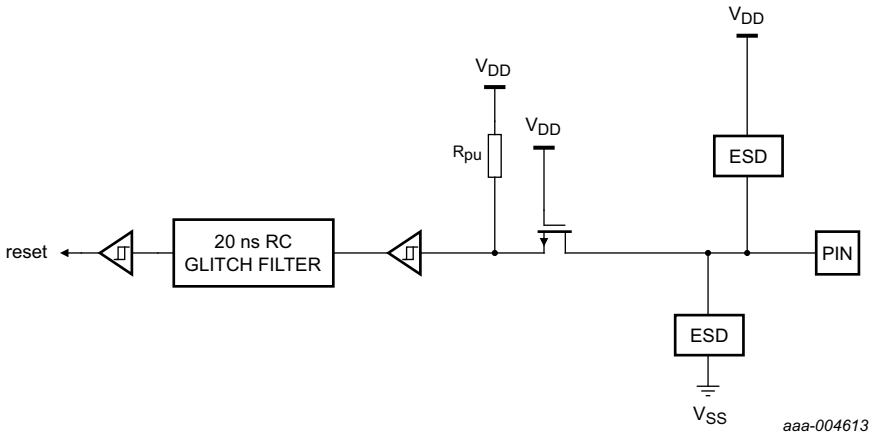


Fig 16. $\overline{\text{RESET}}$ pin configuration

8.41.2 Brownout detection

The LPC15xx includes brown-out detection (BOD) with two levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of two selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels can be selected to cause a forced reset of the chip.

8.41.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

8.42 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M3 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC15xx is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage (3.3 V)	[2]	–0.5	V_{DDA}	V
V_{DDA}	analog supply voltage		–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP_DAC_VDDCMP	–0.5	V_{DDA}	V
		on pin VREFP_ADC	–0.5	V_{DDA}	V
V_{BAT}	battery supply voltage		–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present [3][4]	–0.5	+5.5	V
		on I2C open-drain pins PIO0_22, PIO0_23 [5]	–0.5	+5.5	V
		3 V tolerant I/O pin without over-voltage protection. Applies to PIO0_12. [6]	–0.5	V_{DDA}	V
		USB_DM, USB_DP pins	–0.5	V_{DD} + 0.5	V
V_{IA}	analog input voltage	[7][8][9]	–0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage	[2]	–0.5	+2.5	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	[2]	–0.5	+4.6	V
I_{DD}	supply current	per supply pin	-	100	mA
I_{SS}	ground current	per ground pin	-	100	mA

Table 9. Limiting values *...continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C	-	100	mA
T_{stg}	storage temperature	[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins [11]	-	5	kV

[1] The following applies to the limiting values:
  a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
  b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 11) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_22 and PIO0_23 and except the 3 V tolerant pin PIO0_12.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

[6] Applies to 3 V tolerant pin PIO0_12.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
High-drive output pin configured as digital pin (PIO0_24); see Figure 17						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10[14]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10[14]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10[14]	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V [16] [18]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage	2.4 V <= V_{DD} < 3.0 V	0.30	-	-	V
		3.0 V <= V_{DD} <= 3.6 V	0.35	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.7 V <= V_{DD} < 3.6 V	$V_{DD} - 0.4$	-	-	V
		I_{OH} = 12 mA; 2.4 V <= V_{DD} < 2.7 V	$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.7 V <= V_{DD} < 3.6 V	20	-	-	mA
		$V_{OH} = V_{DD} - 0.4$ V; 2.4 V <= V_{DD} < 2.7 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [19]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [20]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V [20]	−10	−50	−85	µA
		$V_{DD} < V_I < 5$ V	0	0	0	µA
I^2C-bus pins (PIO0_22 and PIO0_23); see Figure 17						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins	3.5	-	-	mA

14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 24:

- The ADC input trace must be short and as close as possible to the LPC15xx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 44) or bus-powered device (see Figure 45).

On the LPC15xx, the PIO0_3/USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always greater than 0 V while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

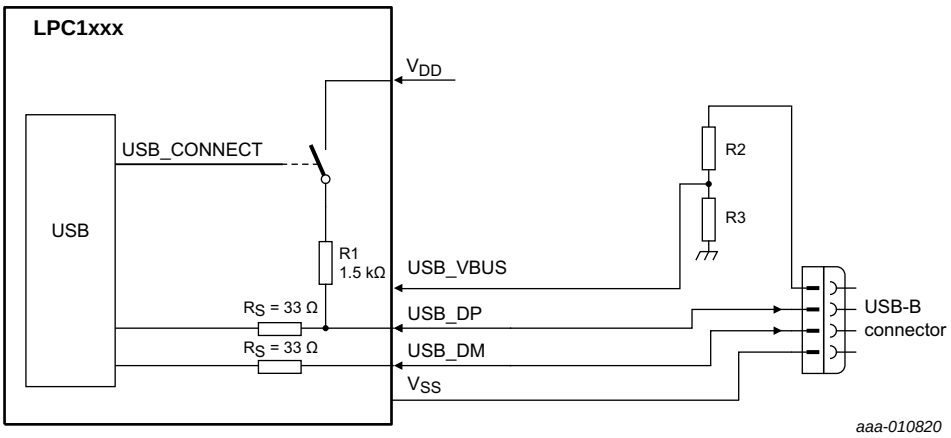


Fig 44. USB interface on a self-powered device where USB_VBUS = 5 V

For a bus-powered device, the VBUS signal does not need to be connected to the USB_VBUS pin (see Figure 45). The USB_CONNECT function can additionally be enabled internally by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required for the USB_CONNECT functionality.

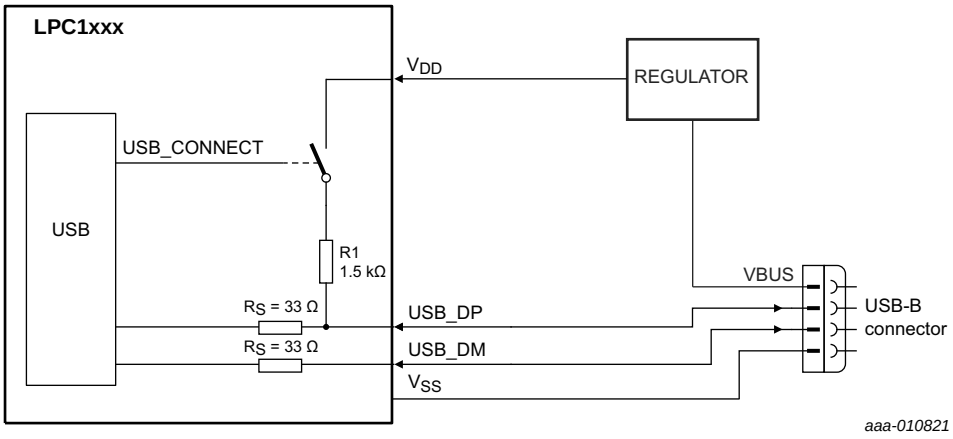


Fig 45. USB interface on a bus-powered device

Remark: When a bus-powered circuit as shown in Figure 45 is used or, for a self-powered device, when the VBUS pin is not connected, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) in the IOCON block. This ties the VBUS signal HIGH internally.

14.2.1 USB Low-speed operation

The USB device controller can be used in low-speed mode supporting 1.5 Mbit/s data exchange with a USB host controller.

Remark: To operate in low-speed mode, change the board connections as follows:

1. Connect USB_DP to the D- pin of the connector.
2. Connect USB_DM to the D+ pin of the connector.

14.5 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 48. If the RTC is not used, the RTCXIN pin can be grounded.

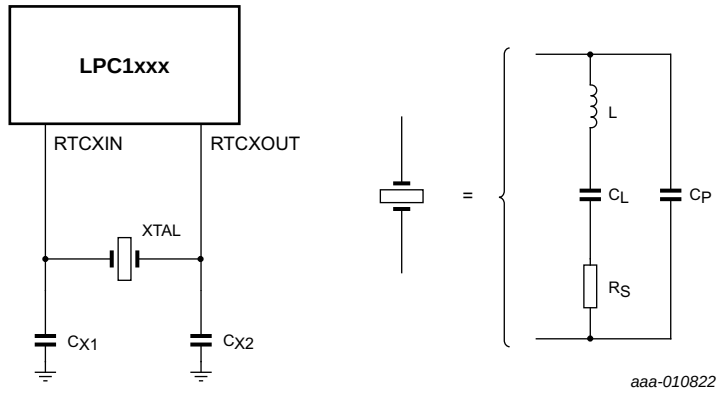


Fig 48. RTC oscillator components

Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry.The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If the external crystal's load capacitance is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$C_{x1} = C_{x2} = 2 \times C_L - C_P$

14.6 Connecting power, clocks, and debug functions

Figure 49 shows the basic board connections used to power the LPC15xx, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

14.9 ElectroMagnetic Compatibility (EMC)

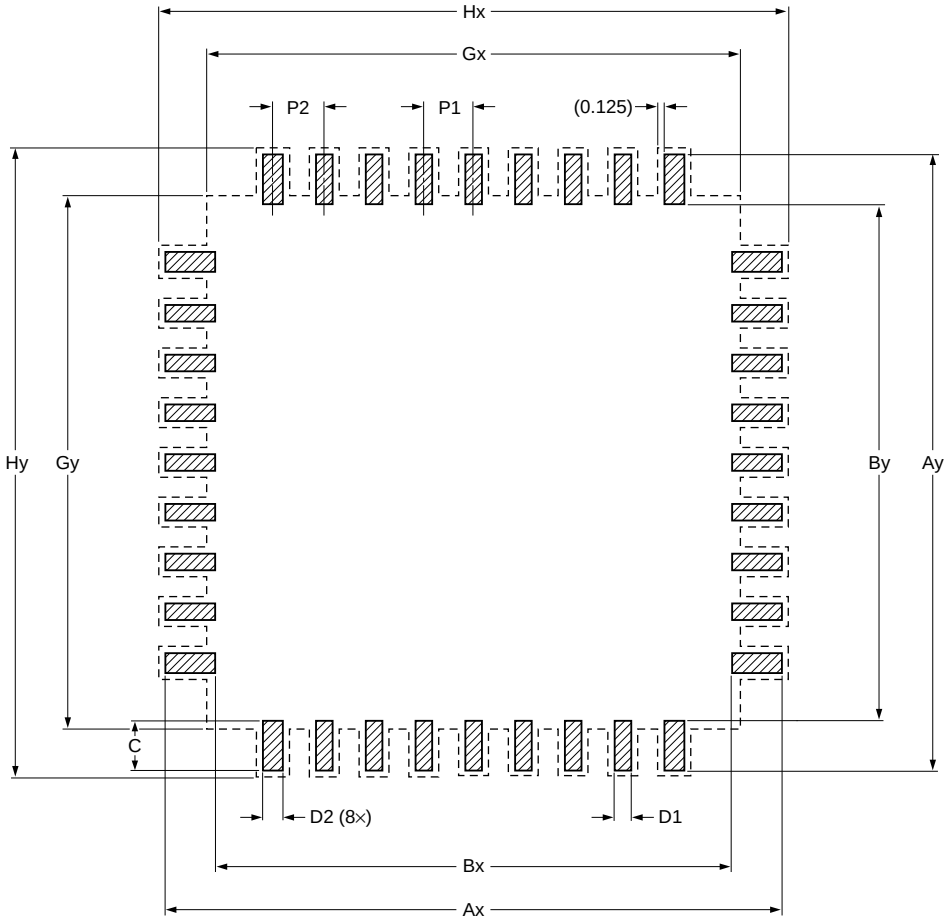
Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1549JBD100.

Table 36. ElectroMagnetic Compatibility (EMC) for part LPC1549 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =						Unit
		12 MHz	24 MHz	36 MHz	48 MHz	60 MHz	72 MHz	
Input clock: IRC (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-5	-1	-5	-4	-3	0	dBμV
	30 MHz to 150 MHz	-1	+3	+6	+8	+11	+14	dBμV
	150 MHz to 1 GHz	-1	+2	+5	+10	+9	+11	dBμV
IEC level[1]	-	O	O	O	N	N	M	-
Input clock: crystal oscillator (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-2	0	-5	-2	-2	2	dBμV
	30 MHz to 150 MHz	0	+3	+6	+8	+12	+14	dBμV
	150 MHz to 1 GHz	-1	+3	+5	+10	+10	+11	dBμV
IEC level[1]	-	O	O	O	N	N	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 54. Reflow soldering for the LQFP64 package

17. References

[1] LPC15xx User manual UM10736:
http://www.nxp.com/documents/user_manual/UM10736.pdf

[2] LPC15xx Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC15XX.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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