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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1517jbd64e

4.1 Ordering options

Table 2. Ordering options for LPC15xx

Type number	Flash/ kB	EEPROM/ kB	Total SRAM/ kB	USB	USART	I^2C	SPI	C_CAN	SCTimer/ PWM	12-bit ADC0/1 channels	DAC	GPIO
LPC1549JBD100	256	4	36	yes	3	1	2	1	4	12/12	1	76
LPC1549JBD64	256	4	36	yes	3	1	2	1	4	12/12	1	44
LPC1549JBD48	256	4	36	yes	3	1	2	1	4	9/7	1	30
LPC1548JBD100	128	4	20	yes	3	1	2	1	4	12/12	1	76
LPC1548JBD64	128	4	20	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD64	64	4	12	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD48	64	4	12	yes	3	1	2	1	4	9/7	1	30
LPC1519JBD100	256	4	36	no	3	1	2	1	4	12/12	1	78
LPC1519JBD64	256	4	36	no	3	1	2	1	4	12/12	1	46
LPC1518JBD100	128	4	20	no	3	1	2	1	4	12/12	1	78
LPC1518JBD64	128	4	20	no	3	1	2	1	4	12/12	1	46
LPC1517JBD64	64	4	12	no	3	1	2	1	4	12/12	1	46
LPC1517JBD48	64	4	12	no	3	1	2	1	4	9/7	1	32

7. Pinning information

7.1 Pinning

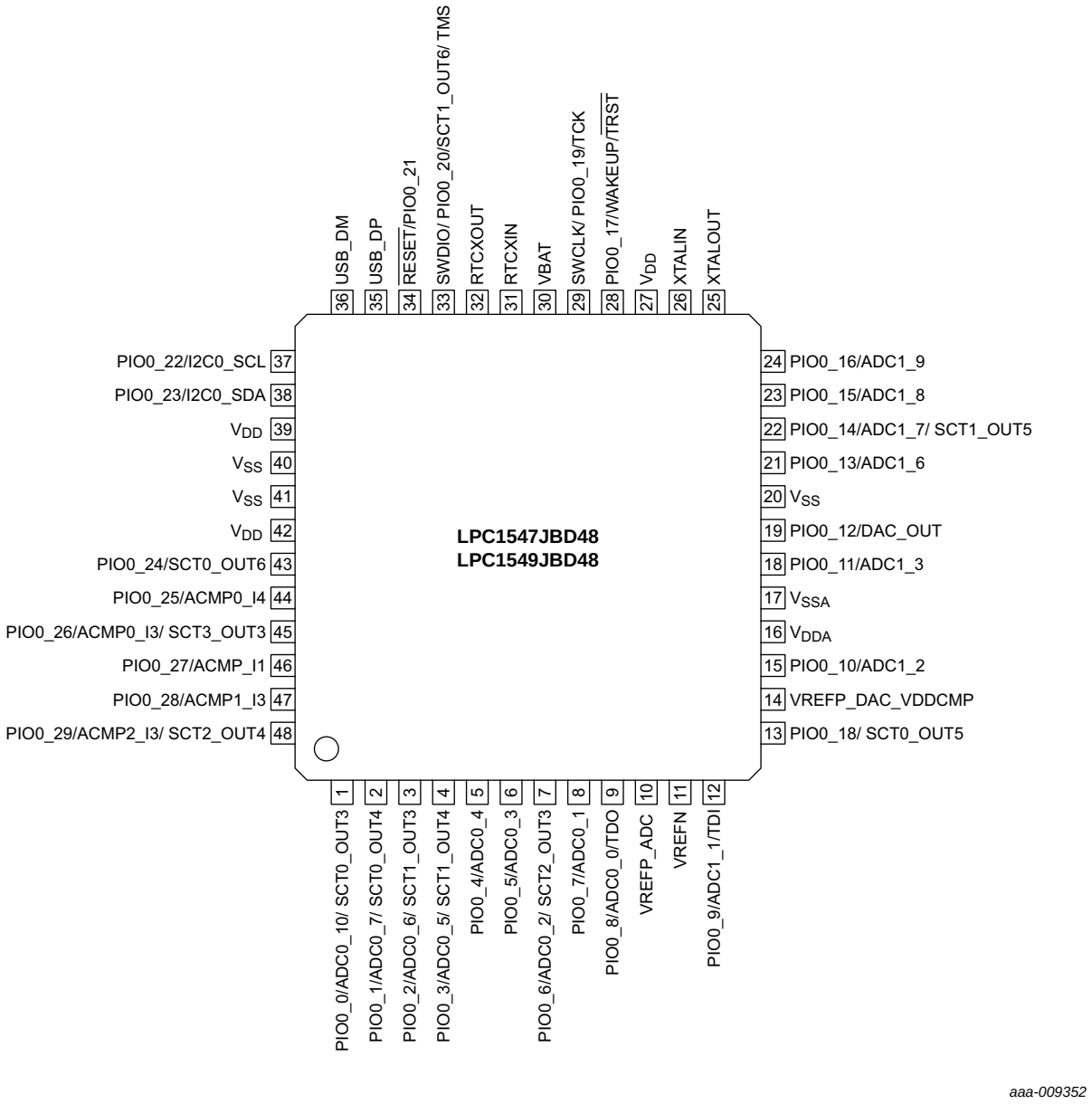


Fig 4. LQFP48 pin configuration (with USB)

Table 4. Movable functions *…continued*

Function name	Type	Description
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
$\overline{\text{U1\_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U1\_CTS}}$	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL0	I/O	Slave select 0 for SPI0.
SPI0_SSEL1	I/O	Slave select 1 for SPI0.
SPI0_SSEL2	I/O	Slave select 2 for SPI0.
SPI0_SSEL3	I/O	Slave select 3 for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL0	I/O	Slave select 0 for SPI1.
SPI1_SSEL1	I/O	Slave select 1 for SPI1.
CAN0_TD	O	CAN0 transmit.
CAN0_RD	I	CAN0 receive.
USB_VBUS	I	USB VBUS.
SCT0_OUT0	O	SCTimer0/PWM output 0.
SCT0_OUT1	O	SCTimer0/PWM output 1.
SCT0_OUT2	O	SCTimer0/PWM output 2.
SCT1_OUT0	O	SCTimer1/PWM output 0.
SCT1_OUT1	O	SCTimer1/PWM output 1.
SCT1_OUT2	O	SCTimer1/PWM output 2.
SCT2_OUT0	O	SCTimer2/PWM output 0.
SCT2_OUT1	O	SCTimer2/PWM output 1.
SCT2_OUT2	O	SCTimer2/PWM output 2.
SCT3_OUT0	O	SCTimer3/PWM output 0.
SCT3_OUT1	O	SCTimer3/PWM output 1.
SCT3_OUT2	O	SCTimer3/PWM output 2.
SCT_ABORT0	I	SCT abort 0.
SCT_ABORT1	I	SCT abort 1.
ADC0_PINTRIG0	I	ADC0 external pin trigger input 0.
ADC0_PINTRIG1	I	ADC0 external pin trigger input 1.
ADC1_PINTRIG0	I	ADC1 external pin trigger input 1.
ADC1_PINTRIG1	I	ADC1 external pin trigger input 1.

8.18 USART0/1/2

Remark: All USART functions are movable functions and are assigned to pins through the switch matrix. Do not connect USART functions to the open-drain pins PIO0_22 and PIO0_23.

Interrupts generated by the USART peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled.

8.18.1 Features

- Maximum bit rates of 4.5 Mbit/s in asynchronous mode, 15 Mbit/s in synchronous mode master mode, and 18 Mbit/s in synchronous slave mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep and power-down modes.
- Special operating mode allows operation at up to 9600 baud using the 32 kHz RTC oscillator as the UART clock. This mode can be used while the device is in Deep-sleep or Power-down mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

8.19 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix. Do not connect SPI functions to the open-drain pins PIO0_22 and PIO0_23.

- 8 inputs and 10 outputs
- DMA support

- Counter/timer features:
  - Configurable as two 16-bit counters or one 32-bit counter.
  - Counters clocked by system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to 16 match and capture registers total.
  - Upon match create the following events: stop, halt, limit counter or change counter direction; toggle outputs; create an interrupt; change the state.
  - Counter value can be loaded into capture register triggered by match or input/output toggle.
- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to eight single-edge or dual-edge controlled PWM outputs with up to eight independent duty cycles when configured as 32-bit timers.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as an rising or falling edge or level, a combination of match and/or input/output condition.
  - Events can only have an effect while the counter is running.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by the set of events that are allowed to happen in the state.
  - A state changes into another state as result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- Dither engine.
- Integrated with an input pre-processing unit (SCTIPU) to combine or delay input events.

Inputs and outputs on the SCTimer0/PWM and SCTimer1/PWM are configured as follows:

- 8 inputs
  - 7 inputs. Each input except input 7 can select one of 23 sources from an input multiplexer.
  - One input connected directly to the SCT PLL for a high-speed dedicated clock input.

- 10 outputs (some outputs are connected to multiple locations)
  - Three outputs connected to external pins through the switch matrix as movable functions.
  - Five outputs connected to external pins through the switch matrix as fixed-pin functions.
  - Two outputs connected to the SCTIPU to sample or latch input events.
  - One output connected to the other large SCT
  - Four outputs connected to one small SCT
  - Two outputs connected to each ADC trigger input

8.22.4 State-Configurable Timers in the small configuration (SCT2/3)

Remark: For applications that require exact timing of the SCT outputs (for example PWM), assign the outputs only to fixed-pin functions to ensure that the output skew is nearly the same for all outputs.

8.22.4.1 Features

The following feature list summarizes the configuration for the two small SCTs. Each small SCT has a companion large SCT (see Section 8.22.3) with more inputs and outputs and a dither engine.

- Each SCT supports:
  - 8 match/capture registers
  - 10 events
  - 10 states
  - 3 inputs and 6 outputs
  - DMA support
- Counter/timer features:
  - Configurable as two 16-bit counters or one 32-bit counter.
  - Counters clocked by bus clock or selected input.
  - Up counters or up-down counters.
  - Configurable number of match and capture registers. Up to 16 match and capture registers total.
  - Upon match create the following events: interrupt, stop, limit timer or change direction; toggle outputs; change state.
  - Counter value can be loaded into capture register triggered by match or input/output toggle.
- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge controlled PWM outputs with independent duty cycles if configured as 32-bit timers.
- Event creation features:

- When the ADC is accurately calibrated, the internal voltage reference can be used to measure the power supply voltage. This requires calibration by recording the ADC code of the internal voltage reference at different power supply levels yielding a different ADC code value for each supply voltage level. In a particular application, the internal voltage reference can be measured and the actual power supply voltage can be determined from the stored calibration values. The calibration values can be stored in the EEPROM for easy access.

After power-up, the internal voltage reference must be allowed to settle to its stable value before it can be used as an ADC reference voltage input.

For an accurate measurement of the internal voltage reference by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.29 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.29.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

8.30 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.30.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WWDT is clocked by the dedicated watchdog oscillator (WDOsc) running at a fixed frequency.

8.36.1 Internal RC oscillator

The IRC can be used as the clock that drives the system PLL and then the CPU. In addition, the IRC can be selected as input to various clock dividers and as the clock source for the USB PLL and the SCT PLL (see Figure 14). The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC15xx use the IRC as the clock source. Software can later switch to one of the other available clock sources.

8.36.2 System oscillator

The system oscillator can be used as a stable and accurate clock source for the CPU, with or without using the PLL. For USB applications, use the system oscillator to provide the clock source to USB PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

The system oscillator has a wake-up time of approximately 500 μs.

8.36.3 Watchdog oscillator

The low-power watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is fixed at 503 kHz. The frequency spread over processing and temperature is ±40 %.

8.36.4 RTC oscillator

The low-power RTC oscillator provides a 1 Hz clock and a 1 kHz clock to the RTC and a 32 kHz clock output that can be used to obtain the main clock (see Figure 14).The 32 kHz oscillator output can be observed on the CLKOUT pin to allow trimming the RTC oscillator without interference from a probe.

8.37 System PLL, USB PLL, and SCT PLL

The LPC15xx contain a three identical PLLs for generating the system clock, the 48 MHz USB clock, and an asynchronous clock for the ADCs and SCTs. The system PLL is used to create the main clock. The SCT and USB PLLs create dedicated clocks for the asynchronous ADC, the asynchronous SCT clock input, and the USB.

Remark: The USB PLL is available on parts LPC1549/48/47 only.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

8.40.3 Deep-sleep mode

In Deep-sleep mode, the LPC15xx is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC15xx can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, an interrupt generating USB port activity, an RTC interrupt, or any interrupts that the USART, SPI, or I2C interfaces can create in Deep-sleep mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Deep-sleep mode saves power and allows for short wake-up times.

8.40.4 Power-down mode

In Power-down mode, the LPC15xx is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC15xx can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, an interrupt generating USB port activity, an RTC interrupt, or any interrupts that the USART, SPI, or I2C interfaces can create in Power-down mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.40.5 Deep power-down mode

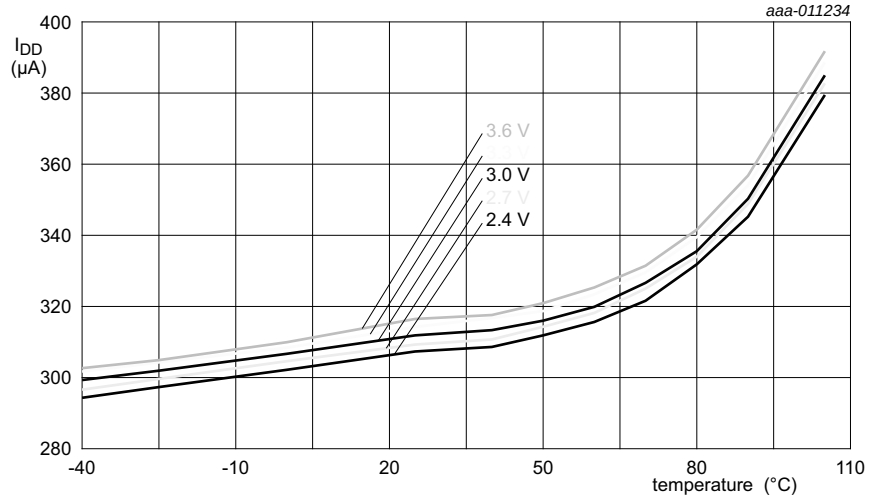
In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the always-on RTC power-domain. The LPC15xx can wake up from Deep power-down mode via the WAKEUP pin or a wake-up signal generated by the RTC interrupt.

The LPC15xx can be blocked from entering Deep power-down mode by setting a lock bit in the PMU block. Blocking the Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the WAKEUP pin is used in the application, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH while the part is in deep power-down mode. Pulling the WAKEUP pin LOW wakes up the part from deep power-down mode. In addition, pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

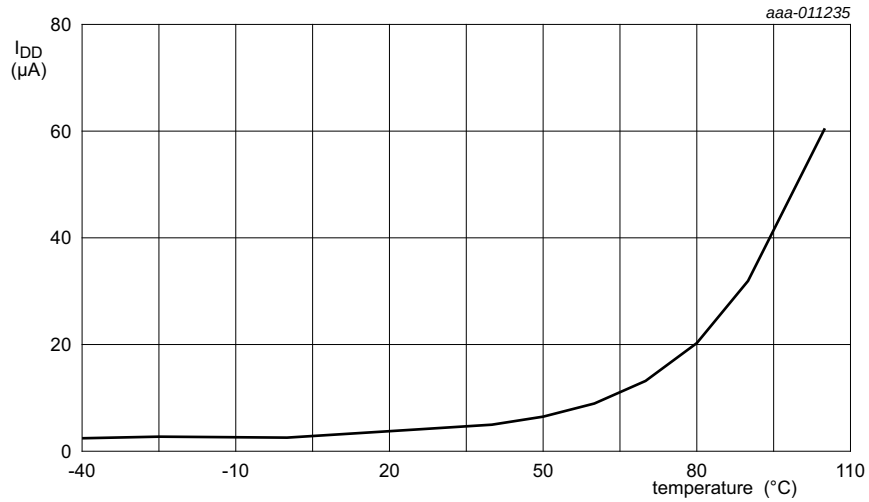
Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; VBAT = 0 or VBAT = 3.0 V [3][12][13]				
		RTC oscillator running				
		T_{amb} = 25 °C	-	1.1	1.3[14]	µA
		T_{amb} = 105 °C	-	-	15	µA
		RTC oscillator input grounded; T_{amb} = 25 °C [3][12]	-	560	-	nA
I_{BAT}	battery supply current	Deep power-down mode; V_{DD} = V_{DDA} = 3.3 V; VBAT = 3.0 V [13]		0	-	nA
		V_{DD} and V_{DDA} tied to ground; VBAT = 3.0 V [13]		1	-	µA
Standard port pins configured as digital pins, $\overline{\text{RESET}}$; see Figure 17						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10[14]	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10[14]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10[14]	nA
V_I	input voltage	$V_{DD} \geq$ 2.4 V; 5 V tolerant pins except PIO0_12 [16] [18]	0	-	5	V
		$V_{DD} \geq$ 2.4 V; on 3 V tolerant pin PIO0_12	0	-	V_{DDA}	
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage	2.4 V <= V_{DD} < 3.0 V	0.30	-	-	V
		3.0 V <= V_{DD} <= 3.6 V	0.35	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V	4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [19]	-	-	-45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [19]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V;	−10	−50	−85	µA
		V_{DD} < V_I < 5 V	0	0	0	µA



Conditions: BOD disabled; all oscillators and analog blocks disabled. Use API power_mode_configure() with mode parameter set to DEEP_SLEEP and peripheral parameter set to 0xFF.

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



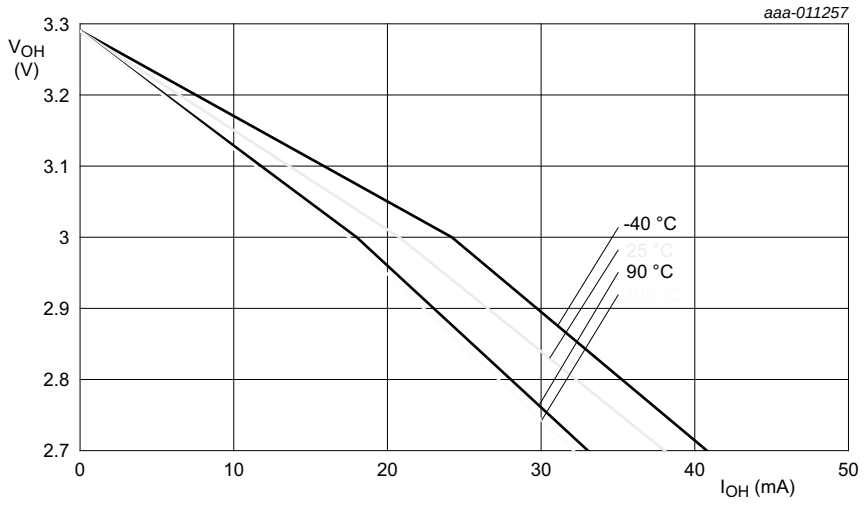
Conditions: BOD disabled; all oscillators and analog blocks disabled; V_{DD} = 2.4 V to 3.6 V. Use API power_mode_configure() with mode parameter set to POWER_DOWN and peripheral parameter set to 0xFF.

Fig 22. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 12. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	72 MHz	
USART0	-	0.02	0.15	-
USART1	-	0.02	0.16	-
USART2	-	0.02	0.15	-
C_CAN	-	0.50	3.00	
USB	-	0.10	0.50	
Comparator ACMP0/1/2/3	-	0.01	0.03	-
ADC0	-	0.05	0.33	-
ADC1	-	0.04	0.33	-
temperature sensor	-	0.03	0.03	
internal voltage reference/band gap	-	0.03	0.04	
DAC	-	0.02	0.09	-
DMA	-	0.36	1.5	
CRC	-	0.01	0.08	-

11.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_24.

Fig 27. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

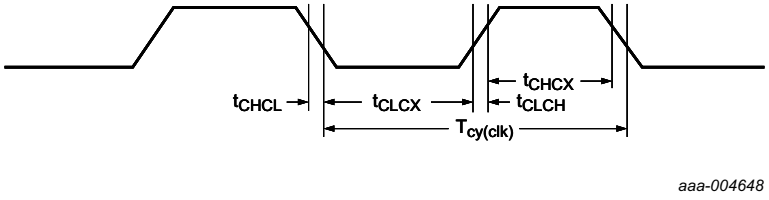


Fig 33. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

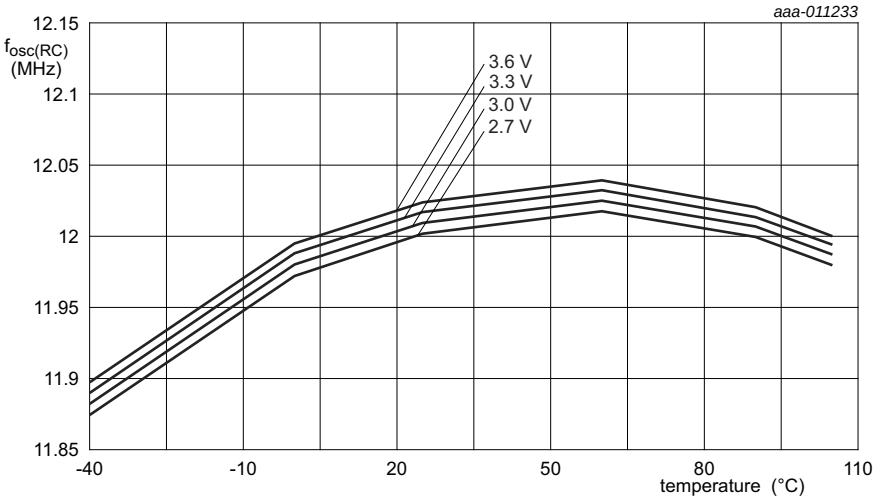
Table 16. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1%	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2%	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 34. Typical Internal RC oscillator frequency versus temperature

Table 17. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	- [2]	-	503	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

12.4 I/O pins

Table 18. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.5 I²C-bus

Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0.26	-	µs
$t_{HD;DAT}$	data hold time [3][4][8]	Standard-mode	0	-	µs
		Fast-mode	0	-	µs
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0	-	µs

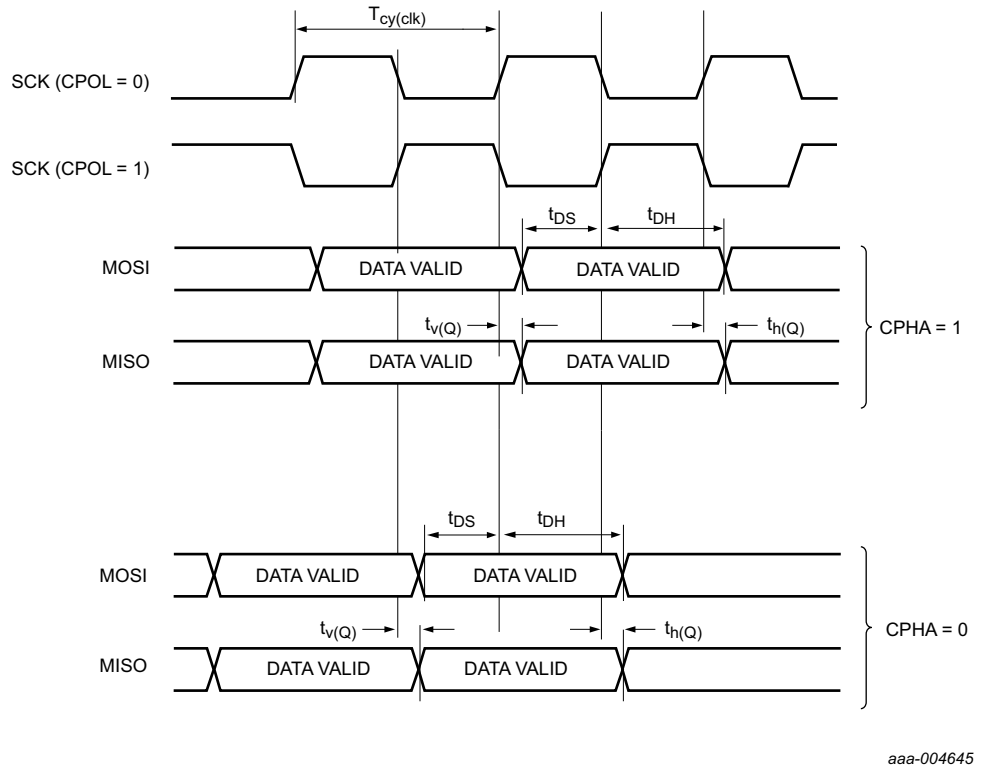


Fig 37. SPI slave timing

14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 24:

- The ADC input trace must be short and as close as possible to the LPC15xx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 44) or bus-powered device (see Figure 45).

On the LPC15xx, the PIO0_3/USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always greater than 0 V while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

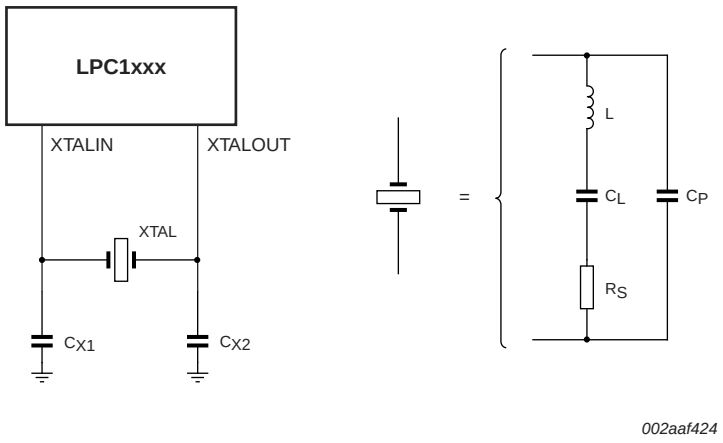


Fig 47. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 32. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 33. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.4 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in

14.5 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 48. If the RTC is not used, the RTCXIN pin can be grounded.

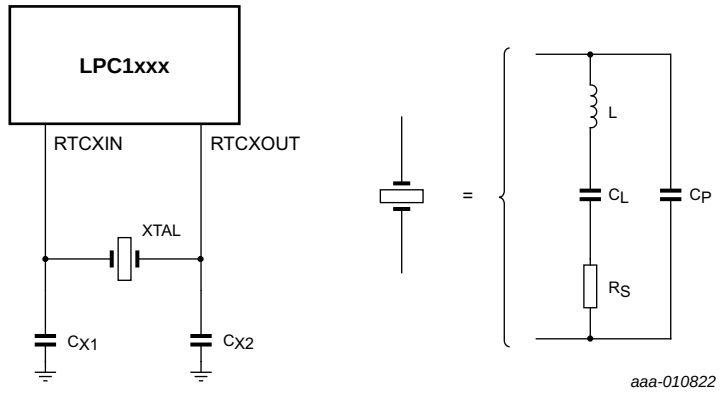


Fig 48. RTC oscillator components

Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry.The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If the external crystal's load capacitance is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$C_{x1} = C_{x2} = 2 \times C_L - C_P$

14.6 Connecting power, clocks, and debug functions

Figure 49 shows the basic board connections used to power the LPC15xx, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

17. References

[1] LPC15xx User manual UM10736:
http://www.nxp.com/documents/user_manual/UM10736.pdf

[2] LPC15xx Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC15XX.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

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