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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1517jbd64y

- Analog peripherals:
  - Two 12-bit ADC with up to 12 input channels per ADC and with multiple internal and external trigger inputs and sample rates of up to 2 Msamples/s. Each ADC supports two independent conversion sequences. ADC conversion clock can be the system clock or an asynchronous clock derived from one of the three PLLs.
  - One 12-bit DAC.
  - Integrated temperature sensor and band gap internal reference voltage.
  - Four comparators with external and internal voltage references (ACMP0 to 3). Comparator outputs are internally connected to the SCTimer/PWMs and ADCs and externally to pins. Each comparator output contains a programmable glitch filter.
- Serial interfaces:
  - Three USART interfaces with DMA, RS-485 support, autobaud, and with synchronous mode and 32 kHz mode for wake-up from Deep-sleep and Power-down modes. The USARTs share a fractional baud-rate generator.
  - Two SPI controllers.
  - One I^2C-bus interface supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode.
  - One C_CAN controller.
  - One USB 2.0 full-speed device controller with on-chip PHY.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Watchdog oscillator with a frequency range of 503 kHz.
  - 32 kHz low-power RTC oscillator with 32 kHz, 1 kHz, and 1 Hz outputs.
  - System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Two additional PLLs for generating the USB and SCTimer/PWM clocks.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - APIs provided for optimizing power consumption in active and sleep modes and for configuring Deep-sleep, Power-down, and Deep power-down modes.
  - Wake-up from Deep-sleep and Power-down modes on activity on USB, USART, SPI, and I2C peripherals.
  - Wake-up from Sleep, Deep-sleep, Power-down, and Deep power-down modes from the RTC alarm or wake-up interrupts.
  - Timer-controlled self wake-up from Deep power-down mode using the RTC high-resolution/wake-up 1 kHz timer.
  - Power-On Reset (POR).
  - BrownOut Detect BOD).
- JTAG boundary scan modes supported.
- Unique device serial number for identification.

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4.1 Ordering options

Table 2. Ordering options for LPC15xx

Type number	Flash/ kB	EEPROM/ kB	Total SRAM/ kB	USB	USART	I^2C	SPI	C_CAN	SCTimer/ PWM	12-bit ADC0/1 channels	DAC	GPIO
LPC1549JBD100	256	4	36	yes	3	1	2	1	4	12/12	1	76
LPC1549JBD64	256	4	36	yes	3	1	2	1	4	12/12	1	44
LPC1549JBD48	256	4	36	yes	3	1	2	1	4	9/7	1	30
LPC1548JBD100	128	4	20	yes	3	1	2	1	4	12/12	1	76
LPC1548JBD64	128	4	20	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD64	64	4	12	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD48	64	4	12	yes	3	1	2	1	4	9/7	1	30
LPC1519JBD100	256	4	36	no	3	1	2	1	4	12/12	1	78
LPC1519JBD64	256	4	36	no	3	1	2	1	4	12/12	1	46
LPC1518JBD100	128	4	20	no	3	1	2	1	4	12/12	1	78
LPC1518JBD64	128	4	20	no	3	1	2	1	4	12/12	1	46
LPC1517JBD64	64	4	12	no	3	1	2	1	4	12/12	1	46
LPC1517JBD48	64	4	12	no	3	1	2	1	4	9/7	1	32

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_27/ACMP_I1	46	62	97	[2]	I; PU	IO	**PIO0_27 —** General purpose port 0 input/output 27.
						A	**ACMP_I1 —** Analog comparator common input 1.
PIO0_28/ACMP1_I3	47	63	98	[2]	I; PU	IO	**PIO0_28 —** General purpose port 0 input/output 28.
						A	**ACMP1_I3 —** Analog comparator 1 input 3.
PIO0_29/ACMP2_I3/ SCT2_OUT4	48	64	100	[2]	I; PU	IO	**PIO0_29 —** General purpose port 0 input/output 29.
						A	**ACMP2_I3 —** Analog comparator 2 input 3.
						O	**SCT2_OUT4 —** SCTimer2/PWM output 4.
PIO0_30/ADC0_11	-	1	1	[2]	I; PU	IO	**PIO0_30 —** General purpose port 0 input/output 30.
						A	**ADC0_11 —** ADC0 input 11.
PIO0_31/ADC0_9	-	3	3	[2]	I; PU	IO	**PIO0_31 —** General purpose port 0 input/output 31. On the LQFP64 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						A	**ADC0_9 —** ADC0 input 9.
PIO1_0/ADC0_8	-	4	5	[2]	I; PU	IO	**PIO1_0 —** General purpose port 1 input/output 0.
						A	**ADC0_8 —** ADC0 input 8.
PIO1_1/ADC1_0	-	15	23	[2]	I; PU	IO	**PIO1_1 —** General purpose port 1 input/output 1.
						A	**ADC1_0 —** ADC1 input 0.
PIO1_2/ADC1_4	-	25	36	[2]	I; PU	IO	**PIO1_2 —** General purpose port 1 input/output 2.
						A	**ADC1_4 —** ADC1 input 4.
PIO1_3/ADC1_5	-	28	41	[2]	I; PU	IO	**PIO1_3 —** General purpose port 1 input/output 3.
						A	**ADC1_5 —** ADC1 input 5.
PIO1_4/ADC1_10	-	33	51	[2]	I; PU	IO	**PIO1_4 —** General purpose port 1 input/output 4.
						A	**ADC1_10 —** ADC1 input 10.
PIO1_5/ADC1_11	-	34	52	[2]	I; PU	IO	**PIO1_5 —** General purpose port 1 input/output 5.
						A	**ADC1_11 —** ADC1 input 11.
PIO1_6/ACMP_I2	-	46	73	[2]	I; PU	IO	**PIO1_6 —** General purpose port 1 input/output 6.
						A	**ACMP_I2 —** Analog comparator common input 2.
PIO1_7/ACMP3_I4	-	51	81	[2]	I; PU	IO	**PIO1_7 —** General purpose port 1 input/output 7.
						A	**ACMP3_I4 —** Analog comparator 3 input 4.
PIO1_8/ACMP3_I3/ SCT3_OUT4	-	53	84	[2]	I; PU	IO	**PIO1_8 —** General purpose port 1 input/output 8.
						A	**ACMP3_I3 —** Analog comparator 3 input 3.
						O	**SCT3_OUT4 —** SCTimer3/PWM output 4.
PIO1_9/ACMP2_I4	-	54	85	[2]	I; PU	IO	**PIO1_9 —** General purpose port 1 input/output 9. On the LQFP64 package, this is the ISP_0 boot pin.
						A	**ACMP2_I4 —** Analog comparator 2 input 4.
PIO1_10/ACMP1_I4	-	59	91	[2]	I; PU	IO	**PIO1_10 —** General purpose port 1 input/output 10.
						A	**ACMP1_I4 —** Analog comparator 1 input 4.
PIO1_11	-	38	58	[5]	I; PU	IO	**PIO1_11 —** General purpose port 1 input/output 11. On the LQFP64 package, this is the ISP_1 boot pin.

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO1_12	-	-	9	[5]	I; PU	IO	**PIO1_12 —** General purpose port 1 input/output 12.
PIO1_13	-	-	11	[5]	I; PU	IO	**PIO1_13 —** General purpose port 1 input/output 13.
PIO1_14/SCT0_OUT7	-	-	12	[5]	I; PU	IO	**PIO1_14 —** General purpose port 1 input/output 14.
						O	**SCT0_OUT7 —** SCTimer0/PWM output 7.
PIO1_15	-	-	15	[5]	I; PU	IO	**PIO1_15 —** General purpose port 1 input/output 15.
PIO1_16	-	-	18	[5]	I; PU	IO	**PIO1_16 —** General purpose port 1 input/output 16.
PIO1_17/SCT1_OUT7	-	-	20	[5]	I; PU	IO	**PIO1_17 —** General purpose port 1 input/output 17.
						O	**SCT1_OUT7 —** SCTimer1/PWM output 7.
PIO1_18	-	-	25	[5]	I; PU	IO	**PIO1_18 —** General purpose port 1 input/output 18.
PIO1_19	-	-	29	[5]	I; PU	IO	**PIO1_19 —** General purpose port 1 input/output 19.
PIO1_20/SCT2_OUT5	-	-	34	[5]	I; PU	IO	**PIO1_20 —** General purpose port 1 input/output 20.
						O	**SCT2_OUT5 —** SCTimer2/PWM output 5.
PIO1_21	-	-	37	[5]	I; PU	IO	**PIO1_21 —** General purpose port 1 input/output 21.
PIO1_22	-	-	38	[5]	I; PU	IO	**PIO1_22 —** General purpose port 1 input/output 22.
PIO1_23	-	-	42	[5]	I; PU	IO	**PIO1_23 —** General purpose port 1 input/output 23.
PIO1_24/SCT3_OUT5	-	-	44	[5]	I; PU	IO	**PIO1_24 —** General purpose port 1 input/output 24.
						O	**SCT3_OUT5 —** SCTimer3/PWM output 5.
PIO1_25	-	-	46	[5]	I; PU	IO	**PIO1_25 —** General purpose port 1 input/output 25.
PIO1_26	-	-	48	[5]	I; PU	IO	**PIO1_26 —** General purpose port 1 input/output 26.
PIO1_27	-	-	50	[5]	I; PU	IO	**PIO1_27 —** General purpose port 1 input/output 27.
PIO1_28	-	-	55	[5]	I; PU	IO	**PIO1_28 —** General purpose port 1 input/output 28.
PIO1_29	-	-	56	[5]	I; PU	IO	**PIO1_29 —** General purpose port 1 input/output 29.
PIO1_30	-	-	59	[5]	I; PU	IO	**PIO1_30 —** General purpose port 1 input/output 30.
PIO1_31	-	-	60	[5]	I; PU	IO	**PIO1_31 —** General purpose port 1 input/output 31.
PIO2_0	-	-	62	[5]	I; PU	IO	**PIO2_0 —** General purpose port 2 input/output 0.
PIO2_1	-	-	64	[5]	I; PU	IO	**PIO2_1 —** General purpose port 2 input/output 1.
PIO2_2	-	-	72	[5]	I; PU	IO	**PIO2_2 —** General purpose port 2 input/output 2.
PIO2_3	-	-	76	[5]	I; PU	IO	**PIO2_3 —** General purpose port 2 input/output 3.
PIO2_4	-	-	77	[5]	I; PU	IO	**PIO2_4 —** General purpose port 2 input/output 4. On the LQFP100 package, this is the ISP_1 boot pin.
PIO2_5	-	-	80	[5]	I; PU	IO	**PIO2_5 —** General purpose port 2 input/output 5. On the LQFP100 package, this is the ISP_0 boot pin.
PIO2_6	-	-	82	[5]	I; PU	IO	**PIO2_6 —** General purpose port 2 input/output 6. On the LQFP100 package, this pin is assigned to U0_TXD in ISP USART mode.
PIO2_7	-	-	86	[5]	I; PU	IO	**PIO2_7 —** General purpose port 2 input/output 7. On the LQFP100 package, this pin is assigned to U0_RXD in ISP USART mode.

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The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

8.3 On-chip flash programming memory

The LPC15xx contain up to 256 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software. Flash updates via USB are supported as well.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.3.1 ISP pin configuration

The LPC15xx supports ISP via the USART0, C_CAN, or USB interfaces. The ISP mode is determined by the state of two pins (ISP_0 and ISP_1) at boot time:

Table 6. ISP modes

Boot mode	ISP_0	ISP_1	Description
No ISP	HIGH	HIGH	ISP bypassed. Part attempts to boot from flash. If the user code in flash is not valid, then enters ISP via USB.
C_CAN	HIGH	LOW	Part enters ISP via C_CAN.
USB	LOW	HIGH	Part enters ISP via USB.
USART0	LOW	LOW	Part enters ISP via USART0.

The ISP pin assignment is different for each package, so that the fewest functions possible are blocked. No more than four pins must be set aside for entering ISP in any ISP mode. The boot code assigns two ISP pins for each package, which are probed when the part boots to determine whether or not to enter ISP mode. Once the ISP mode has been determined, the boot loader configures the necessary serial pins for each package.

Pins which are not configured by the boot loader for the selected boot mode (for example CAN0_RD and CAN0_TD in USART mode) can be assigned to any function through the switch matrix.

Table 7. Pin assignments for ISP modes

Boot pin	LQFP48	LQFP64	LQFP100
ISP_0	PIO0_4	PIO1_9	PIO2_5
ISP_1	PIO0_16	PIO1_11	PIO2_4
USART mode			
U0_TXD	PIO0_15	PIO0_18	PIO2_6
U0_RXD	PIO0_14	PIO0_13	PIO2_7
C_CAN mode			
CAN0_TD	PIO0_18	PIO0_31	PIO2_8
CAN0_RD	PIO0_13	PIO0_11	PIO2_9
USB mode			
USB_VBUS (same as ISP_1)	PIO0_16	PIO1_11	PIO2_4

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8.19.1 Features

- Maximum data rates of 17 Mbit/s in master mode and slave mode for SPI functions connected to all digital pins except PIO0_22 and PIO0_23.
- Data transmits of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Up to four Slave Select input/outputs with selectable polarity and flexible usage.
- Supports DMA transfers: SPIn transmit and receive functions work with the system DMA controller.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.20 I2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are fixed-pin functions and must be enabled through the switch matrix on the open-drain pins PIO0_22 and PIO0_23.

8.20.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.
- Supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Fail-safe operation: When the power to an I^2C-bus device is switched off, the SDA and SCL pins connected to the I^2C-bus are floating and do not disturb the bus.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Supported by on-chip ROM API.

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8.21 C_CAN

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller can build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

The C_CAN functions are movable functions and are assigned to pins through the switch matrix. Do not connect C_CAN functions to the open-drain pins PIO0_22 and PIO0_23.

8.21.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

8.22 PWM/timer/motor control subsystem

The SCTimer/PWMs (State Configurable Timer/Pulse Width Modulators) and the analog peripherals support multiple ways of interconnecting their inputs and outputs and of interfacing to the pins and the DMA controller. Using the highly flexible and programmable connection scheme makes it easy to configure various subsystems for motor control and complex timing and tracking applications. Specifically, the inputs to the SCTs and the trigger inputs of the ADCs and DMA are selected through the input multiplexer which offers a choice of many possible sources for each input or trigger. SCT outputs are assigned to pins through the switch matrix allowing for many pinout solutions.

8.22.1 SCtimer/PWM subsystem

The SCTimer/PWMs can be configured to build a PWM controller with multiple outputs by programming the MATCH and MATCHRELOAD registers to control the base frequency and the duty cycle of each SCTimer/PWM output. More complex waveforms that span multiple counter cycles or change behavior across or within counter cycles can be generated using the state capability built into the SCTimer/PWMs.

Combining the PWM functions with the analog functions, the PWM output can react to control signals like comparator outputs or the ADC interrupts. The SCT IPU adds emergency shut-down functions and pre-processing of controlling events. For an overview of the PWM subsystem, see Figure 12 “PWM-Analog subsystem”.

For high-speed PWM functionality, use only outputs that are fixed-pin functions to minimize pin-to-pin differences in output skew. See also Table 22 “SCTimer/PWM output dynamic characteristics”. This reduces the number of PWM outputs to five for each large SCT.

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- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Selected events can limit, halt, start, or stop a counter.
- Events control state changes, outputs, interrupts, and DMA requests.
- Match register 0 can be used as an automatic limit.
- In bi-directional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can take place in the state while the counter is running.
  - A state changes into another state as result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- Integrated with an input pre-processing unit (SCTIPU) to combine or delay input events.

Inputs and outputs on the SCTimer2/PWM and SCTimer3/PWM are configured as follows:

- 3 inputs. Each input selects one of 21 sources from a pin multiplexer.
- 6 outputs (some outputs are connected to multiple locations)
  - Three outputs connected to external pins through the switch matrix as movable functions.
  - Three outputs connected to external pins through the switch matrix as fixed-pin functions.
  - Two outputs connected to the SCT IPU to sample or latch input events.
  - Four outputs connected to the accompanying large SCT
  - Two outputs connected to each ADC trigger input

8.22.5 SCT Input processing unit (SCTIPU)

The SCTIPU allows to block or propagate signals to inputs of the SCT under the control of an SCT output. Using the SCTIPU in this way, allows signals to be blocked from entering the SCT inputs for a certain amount of time, for example while they are known to be invalid.

In addition, the SCTIPU can generate a common signal from several combined input sources that can be selected on all SCT inputs. Such a mechanism can be useful to create an abort signal that stops all timers.

8.22.5.1 Features

The SCTIPU pre-processes inputs to the State-Configurable Timers (SCT).

- Four outputs created from a selection of input transitions. Each output can be used as abort input to the SCTs or for any other application which requires a collection of multiple SCT inputs to trigger an identical SCT response.

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8.26.1 Features

- Seven selectable inputs. Fully configurable on either the positive side or the negative input channel.
- 32-stage voltage ladder internal reference for selectable voltages on each comparator; configurable on either positive or negative comparator input.
- Voltage ladder source voltage is selectable from an external pin or the 3.3 V analog voltage supply.
- 0.9 V internal band gap reference voltage selectable as either positive or negative input on each comparator.
- Temperature sensor voltage selectable as either positive or negative input on each comparator.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Individual comparator outputs can be connected internally to the SCT and ADC trigger inputs or the external pins.
- Separate interrupt for each comparator.
- Pin filter included on each comparator output.
- Three propagation delay values are programmable to optimize between speed and power consumption.
- Relaxation oscillator circuitry output for a 555 style timer operation using comparator blocks 0 and 1.

8.27 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.28 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.905 V. The internal voltage reference can be used in the following applications:

- When the supply voltage V_{DD} is known accurately, the internal voltage reference can be used to reduce the offset error E_O of the ADC code output. The ADC error correction then increases the accuracy of temperature sensor voltage output measurements.

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- When the ADC is accurately calibrated, the internal voltage reference can be used to measure the power supply voltage. This requires calibration by recording the ADC code of the internal voltage reference at different power supply levels yielding a different ADC code value for each supply voltage level. In a particular application, the internal voltage reference can be measured and the actual power supply voltage can be determined from the stored calibration values. The calibration values can be stored in the EEPROM for easy access.

After power-up, the internal voltage reference must be allowed to settle to its stable value before it can be used as an ADC reference voltage input.

For an accurate measurement of the internal voltage reference by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.29 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.29.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

8.30 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.30.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WWDT is clocked by the dedicated watchdog oscillator (WDOsc) running at a fixed frequency.

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8.34 Clock generation

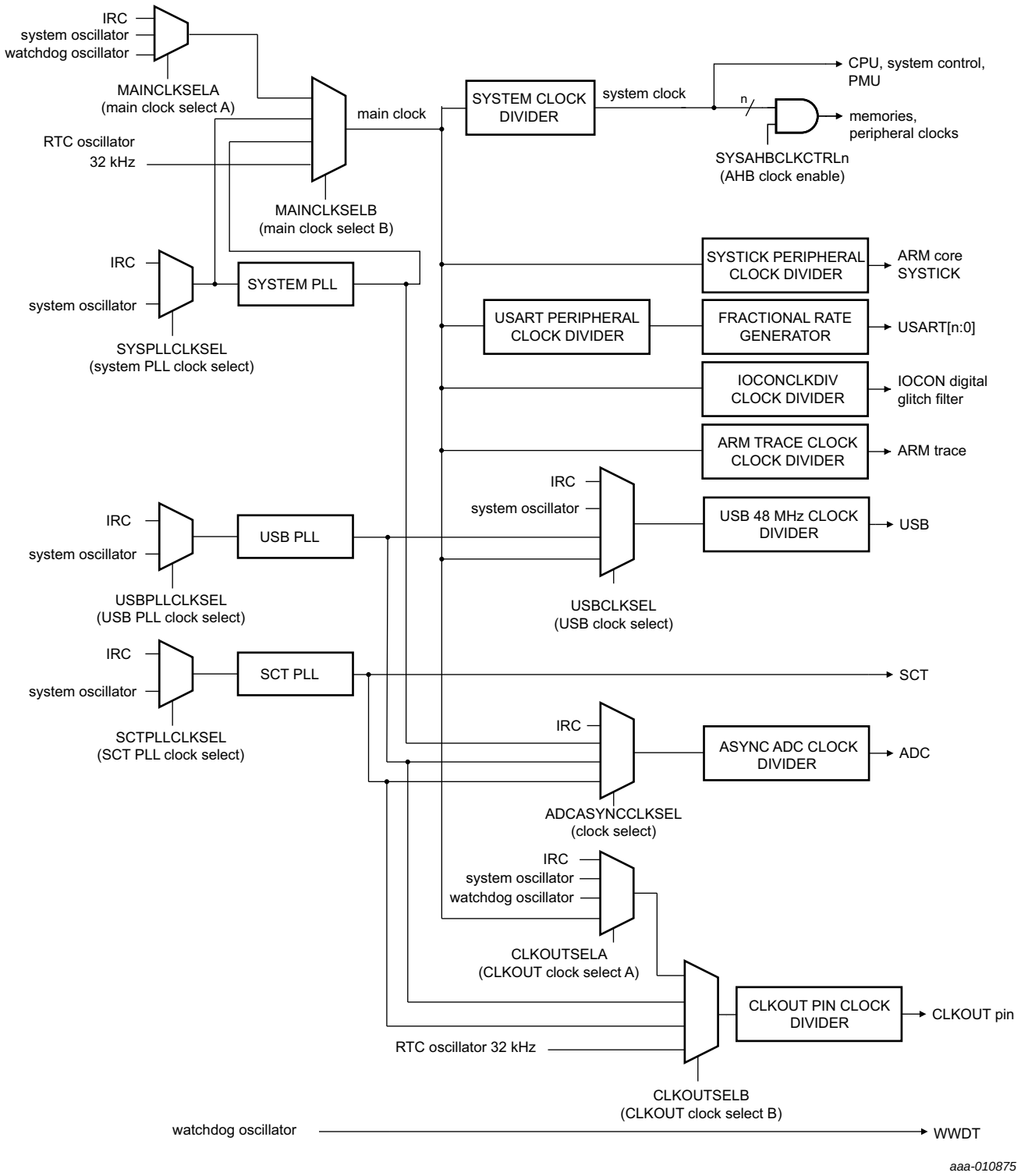

Fig 14. Clock generation

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8.42 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M3 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC15xx is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage (3.3 V)	[2]	–0.5	V_{DDA}	V
V_{DDA}	analog supply voltage		–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP_DAC_VDDCMP	–0.5	V_{DDA}	V
		on pin VREFP_ADC	–0.5	V_{DDA}	V
V_{BAT}	battery supply voltage		–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present [3][4]	–0.5	+5.5	V
		on I2C open-drain pins PIO0_22, PIO0_23 [5]	–0.5	+5.5	V
		3 V tolerant I/O pin without over-voltage protection. Applies to PIO0_12. [6]	–0.5	V_{DDA}	V
		USB_DM, USB_DP pins	–0.5	V_{DD} + 0.5	V
V_{IA}	analog input voltage	[7][8][9]	–0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage	[2]	–0.5	+2.5	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	[2]	–0.5	+4.6	V
I_{DD}	supply current	per supply pin	-	100	mA
I_{SS}	ground current	per ground pin	-	100	mA

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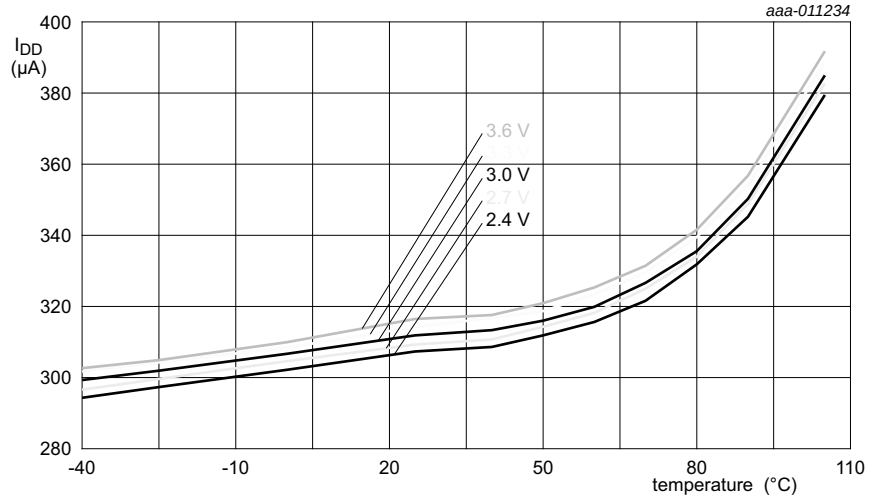
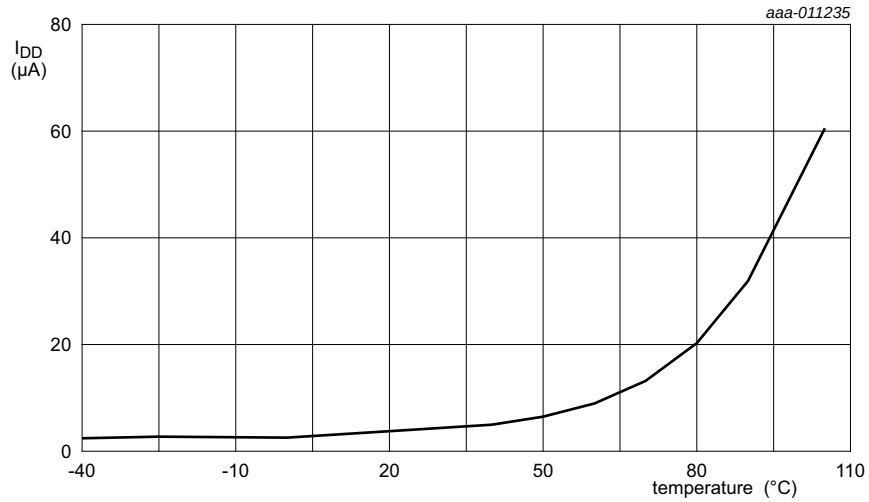


Conditions: BOD disabled; all oscillators and analog blocks disabled. Use API power_mode_configure() with mode parameter set to DEEP_SLEEP and peripheral parameter set to 0xFF.

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled; V_{DD} = 2.4 V to 3.6 V. Use API power_mode_configure() with mode parameter set to POWER_DOWN and peripheral parameter set to 0xFF.

Fig 22. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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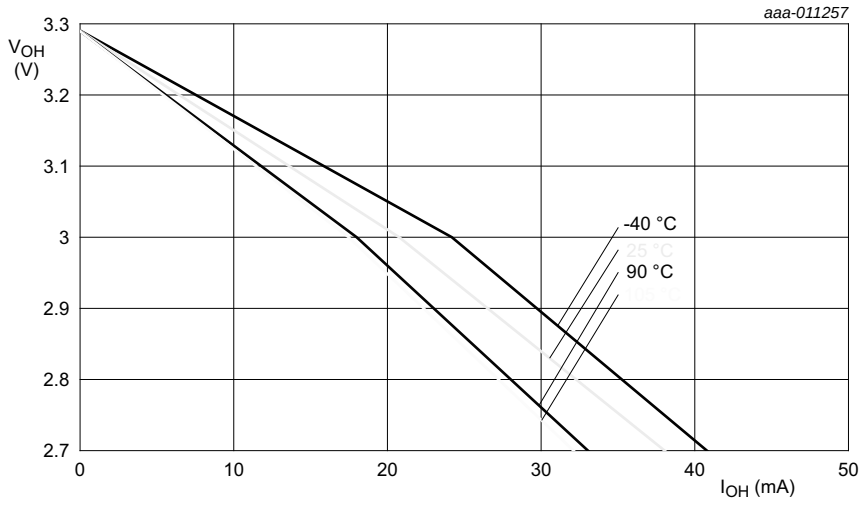
Table 12. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	72 MHz	
USART0	-	0.02	0.15	-
USART1	-	0.02	0.16	-
USART2	-	0.02	0.15	-
C_CAN	-	0.50	3.00	
USB	-	0.10	0.50	
Comparator ACMP0/1/2/3	-	0.01	0.03	-
ADC0	-	0.05	0.33	-
ADC1	-	0.04	0.33	-
temperature sensor	-	0.03	0.03	
internal voltage reference/band gap	-	0.03	0.04	
DAC	-	0.02	0.09	-
DMA	-	0.36	1.5	
CRC	-	0.01	0.08	-

11.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_24.

Fig 27. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

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Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

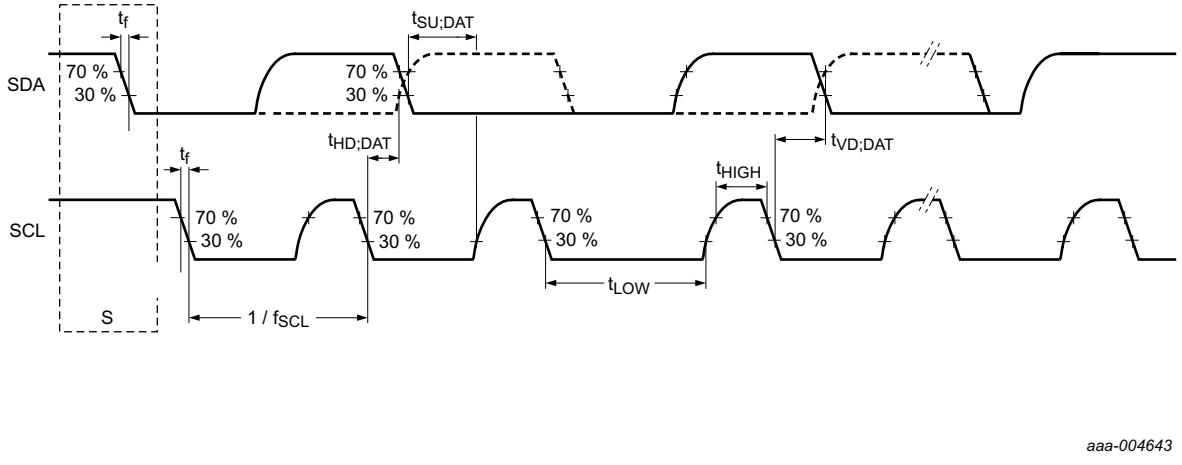

Fig 35. I²C-bus pins clock timing

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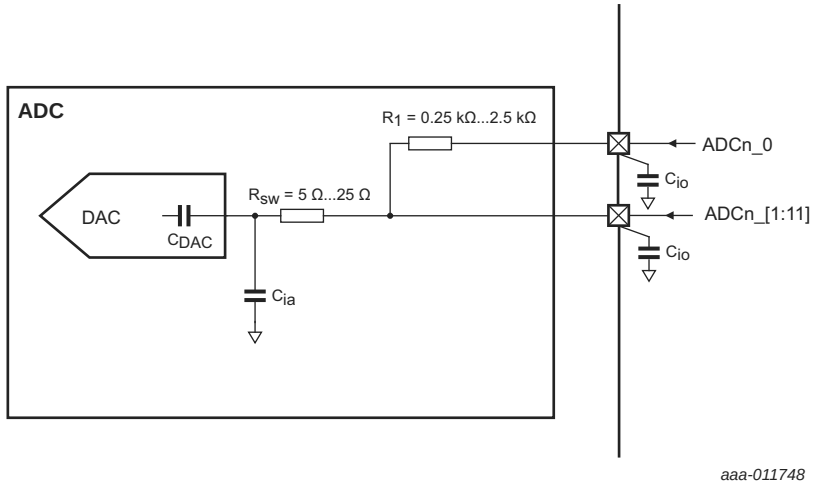

Fig 39. ADC input impedance

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14.7 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as GPIO (switch matrix default) and setto outputs driving LOW with their internal pull-up disabled. To drive the output LOW, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_21	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether Deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
USB_DP/USB_DM	F	Can be left unconnected. When the USP PHY is disabled, the pins are LOW.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP_DAC_VDDCMP	-	Tie to VDD.
VREFP_ADC		Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VBAT	-	Tie to VDD if no external battery connected.
VSSA	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

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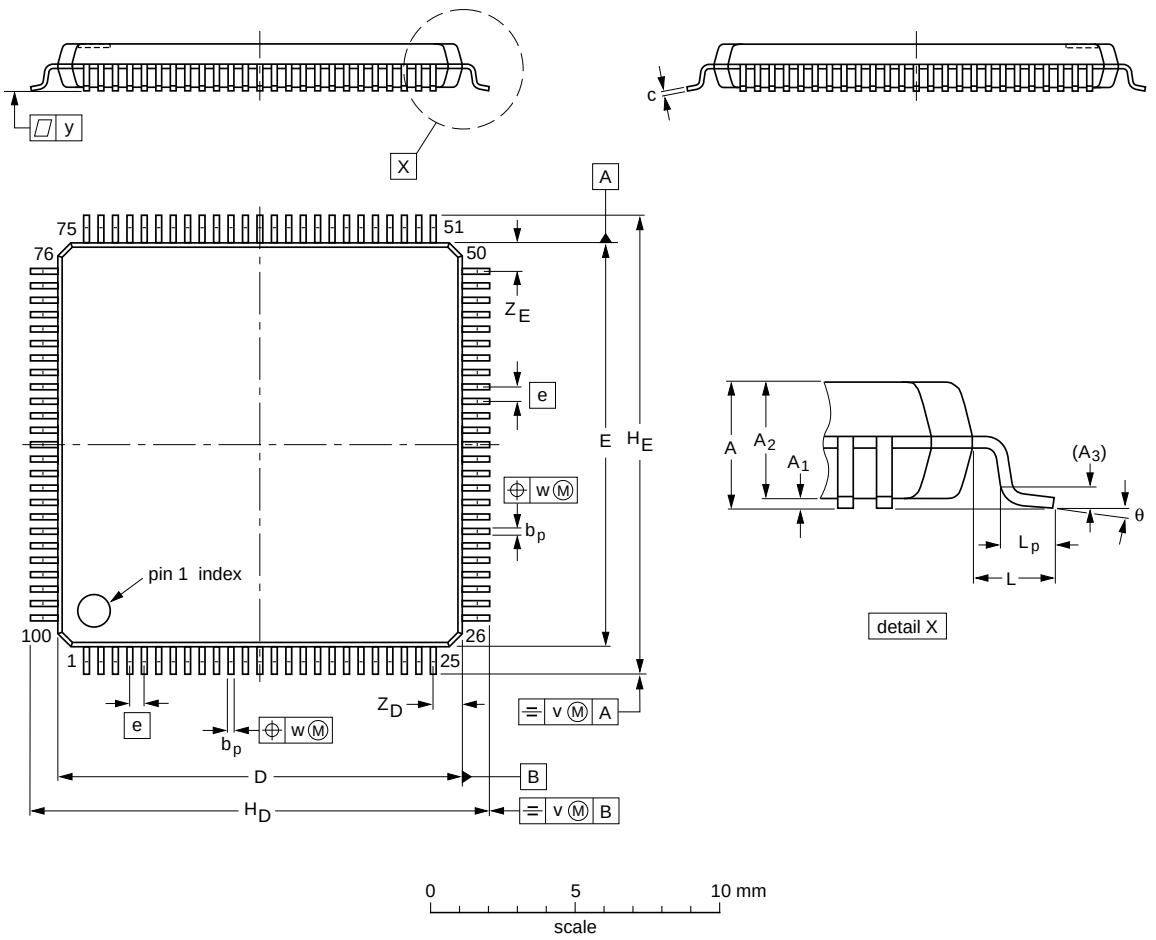
LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 52. Package outline LQFP100 (SOT407-1)

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17. References

[1] LPC15xx User manual UM10736:
http://www.nxp.com/documents/user_manual/UM10736.pdf

[2] LPC15xx Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC15XX.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

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