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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1518jbd100e

- ROM API support:
  - Boot loader with boot options from flash or external source via USART, C_CAN, or USB
  - USB drivers
  - ADC drivers
  - SPI drivers
  - USART drivers
  - I2C drivers
  - Power profiles and power mode configuration with low-power mode configuration option
  - DMA drivers
  - C_CAN drivers
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - Simple DMA engine with 18 channels and 20 programmable input triggers.
  - High-speed GPIO interface with up to 76 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, open-drain mode, input inverter, and programmable digital glitch filter.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight external inputs.
  - Two GPIO grouped port interrupts.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - Quadrature Encoder Interface (QEI).
- Configurable PWM/timer/motor control subsystem:
  - Up to four 32-bit counter/timers or up to eight 16-bit counter/timers or combinations of 16-bit and 32-bit timers.
  - Up to 28 match outputs and 22 configurable capture inputs with input multiplexer.
  - Up to 28 PWM outputs total.
  - Dither engine for improved average resolution of pulse edges.
  - Four State Configurable Timers (SCTimers) for highly flexible, event-driven timing and PWM applications.
  - SCT Input Pre-processor Unit (SCTIPU) for processing timer inputs and immediate handling of abort situations.
  - Integrated with ADC threshold compare interrupts, temperature sensor, and analog comparator outputs for motor control feedback using analog signals.
- Special-application and simple timers:
  - 24-bit, four-channel, multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Repetitive interrupt timer for general purpose use.
  - Windowed Watchdog timer (WWDT).
  - High-resolution 32-bit Real-time clock (RTC) with selectable 1 s or 1 ms time resolution running in the always-on power domain. RTC can be used for wake-up from all low power modes including Deep power-down.

4.1 Ordering options

Table 2. Ordering options for LPC15xx

Type number	Flash/ kB	EEPROM/ kB	Total SRAM/ kB	USB	USART	I^2C	SPI	C_CAN	SCTimer/ PWM	12-bit ADC0/1 channels	DAC	GPIO
LPC1549JBD100	256	4	36	yes	3	1	2	1	4	12/12	1	76
LPC1549JBD64	256	4	36	yes	3	1	2	1	4	12/12	1	44
LPC1549JBD48	256	4	36	yes	3	1	2	1	4	9/7	1	30
LPC1548JBD100	128	4	20	yes	3	1	2	1	4	12/12	1	76
LPC1548JBD64	128	4	20	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD64	64	4	12	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD48	64	4	12	yes	3	1	2	1	4	9/7	1	30
LPC1519JBD100	256	4	36	no	3	1	2	1	4	12/12	1	78
LPC1519JBD64	256	4	36	no	3	1	2	1	4	12/12	1	46
LPC1518JBD100	128	4	20	no	3	1	2	1	4	12/12	1	78
LPC1518JBD64	128	4	20	no	3	1	2	1	4	12/12	1	46
LPC1517JBD64	64	4	12	no	3	1	2	1	4	12/12	1	46
LPC1517JBD48	64	4	12	no	3	1	2	1	4	9/7	1	32

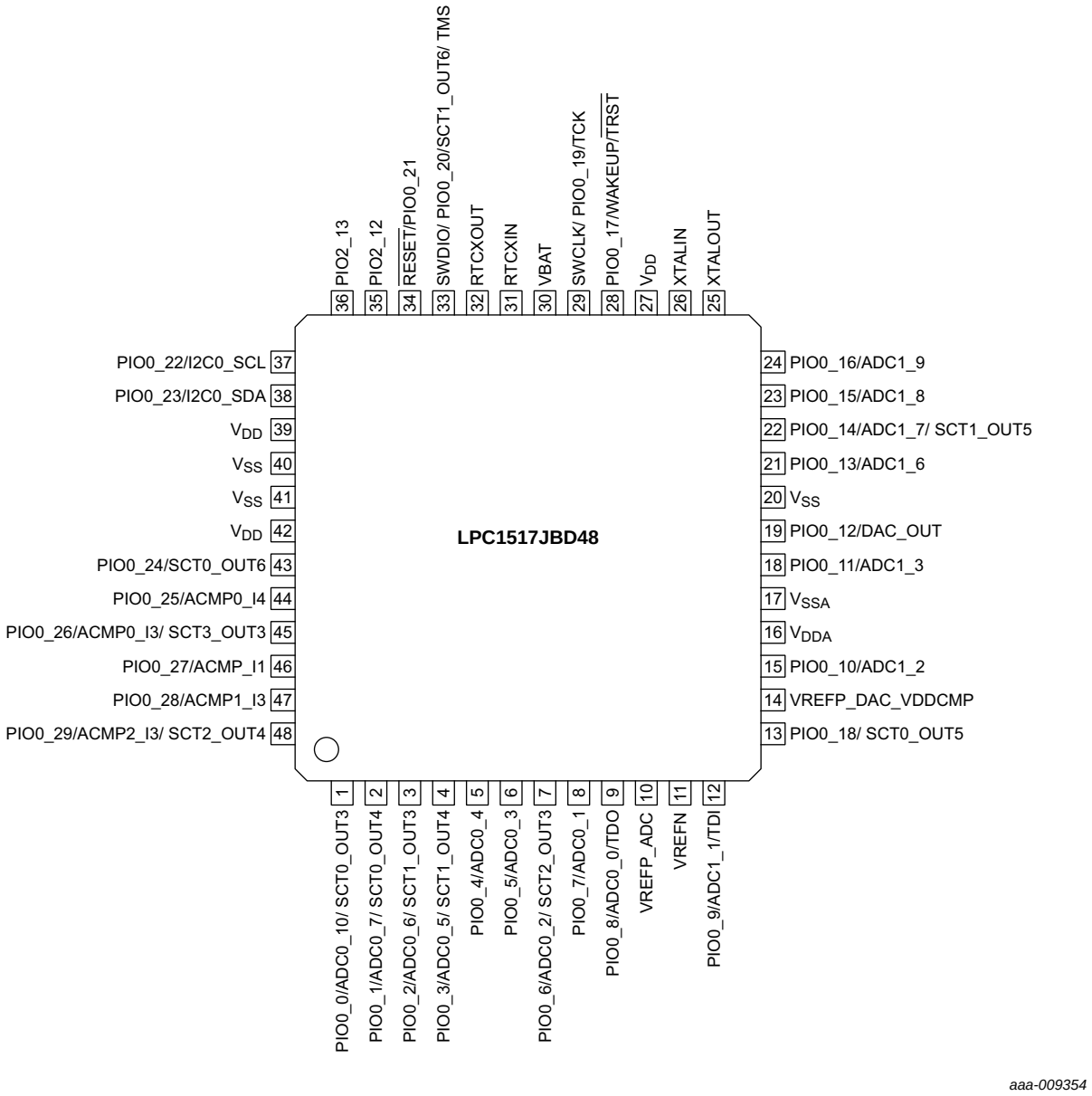


Fig 5. LQFP48 pin configuration (without USB)

7.2 Pin description

Most pins are configurable for multiple functions, which can be analog or digital. Digital inputs can be connected to several peripherals at once, however only one digital output or one analog function can be assigned to any on pin. The pin's connections to internal peripheral blocks are configured by the switch matrix (SWM), the input multiplexer (INPUT MUX), and the SCT Input Pre-processor Unit (SCTIPU).

The switch matrix enables certain fixed-pin functions that can only reside on specific pins (see Table 3) and assigns all other pin functions (movable functions) to any available pin (see Table 4), so that the pinout can be optimized for a given application.

The input multiplexer provides many choices (pins and internal signals) for selecting the inputs of the SCTimer/PWMs and the frequency measure block. Pins that are connected to the input multiplexer are listed in Table 5. If a pin is selected in the input multiplexer, it is directly connected to the peripheral input without being routed through the switch matrix. Independently of being selected in the input multiplexer, the same pin can also be assigned by the switch matrix to another peripheral input.

Four pins can also be connected directly to the SCTIPU and at the same time be inputs to the input multiplexer and the switch matrix (see Table 5).

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_0/ADC0_10/ SCT0_OUT3	1	2	2	[2]	I; PU	IO	**PIO0_0 —** General purpose port 0 input/output 0.
						A	**ADC0_10 —** ADC0 input 10.
						O	**SCT0_OUT3 —** SCTimer0/PWM output 3.
PIO0_1/ADC0_7/ SCT0_OUT4	2	5	6	[2]	I; PU	IO	**PIO0_1 —** General purpose port 0 input/output 1.
						A	**ADC0_7 —** ADC0 input 7.
						O	**SCT0_OUT4 —** SCTimer0/PWM output 4.
PIO0_2/ADC0_6/ SCT1_OUT3	3	6	8	[2]	I; PU	IO	**PIO0_2 —** General purpose port 0 input/output 2.
							ADC0_6 — ADC0 input 6.
						O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO0_3/ADC0_5/ SCT1_OUT4	4	7	10	[2]	I; PU	IO	**PIO0_3 —** General purpose port 0 input/output 3.
						A	**ADC0_5 —** ADC0 input 5.
						O	**SCT1_OUT4 —** SCTimer1/PWM output 4.
PIO0_4/ADC0_4	5	8	13	[2]	I; PU	IO	**PIO0_4 —** General purpose port 0 input/output 4. This is the ISP_0 boot pin for the LQFP48 package.
						A	**ADC0_4 —** ADC0 input 4.
PIO0_5/ADC0_3	6	9	14	[2]	I; PU	IO	**PIO0_5 —** General purpose port 0 input/output 5.
						A	**ADC0_3 —** ADC0 input 3.
PIO0_6/ADC0_2/ SCT2_OUT3	7	10	16	[2]	I; PU	IO	**PIO0_6 —** General purpose port 0 input/output 6.
						A	**ADC0_2 —** ADC0 input 2.
						O	**SCT2_OUT3 —** SCTimer2/PWM output 3.
PIO0_7/ADC0_1	8	11	17	[2]	I; PU	IO	**PIO0_7 —** General purpose port 0 input/output 7.
						A	**ADC0_1 —** ADC0 input 1.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_18/ SCT0_OUT5	13	17	26	[5]	I; PU	IO	**PIO0_18 —** General purpose port 0 input/output 18. On the LQFP64 package, this pin is assigned to U0_TXD in ISP USART mode. On the LQFP48 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						O	**SCT0_OUT5 —** SCTimer0/PWM output 5.
SWCLK/ PIO0_19/TCK	29	40	63	[5]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						IO	**PIO0_19 —** General purpose port 0 input/output 19.
SWDIO/ PIO0_20/SCT1_OUT6/ TMS	33	44	69	[5]	I; PU	I/O	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						I/O	**PIO0_20 —** General purpose port 0 input/output 20.
						O	**SCT1_OUT6 —** SCTimer1/PWM output 6.
$\overline{\text{RESET}}$/PIO0_21	34	45	71	[6]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed and the Deep power-down mode is not used.
						I/O	**PIO0_21 —** General purpose port 0 input/output 21.
PIO0_22/I2C0_SCL	37	49	78	[7]	IA	IO	**PIO0_22 —** General purpose port 0 input/output 22 (open-drain)
						I/O	**I2C0_SCL —** Open-drain I^2C-bus clock input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_23/I2C0_SDA	38	50	79	[7]	IA	IO	**PIO0_23 —** General purpose port 0 input/output 23 (open-drain).
						I/O	**I2C0_SDA —** I^2C-bus data input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_24/SCT0_OUT6	43	58	90	[8]	I; PU	IO	**PIO0_24 —** General purpose port 0 input/output 24. High-current output driver.
						O	**SCT0_OUT6 —** SCTimer0/PWM output 6.
PIO0_25/ACMP0_I4	44	60	93	[2]	I; PU	IO	**PIO0_25 —** General purpose port 0 input/output 25.
						A	**ACMP0_I4 —** Analog comparator 0 input 4.
PIO0_26/ACMP0_I3/ SCT3_OUT3	45	61	95	[2]	I; PU	IO	**PIO0_26 —** General purpose port 0 input/output 26.
						A	**ACMP0_I3 —** Analog comparator 0 input 3.
						O	**SCT3_OUT3 —** SCTimer3/PWM output 3.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO1_12	-	-	9	[5]	I; PU	IO	**PIO1_12 —** General purpose port 1 input/output 12.
PIO1_13	-	-	11	[5]	I; PU	IO	**PIO1_13 —** General purpose port 1 input/output 13.
PIO1_14/SCT0_OUT7	-	-	12	[5]	I; PU	IO	**PIO1_14 —** General purpose port 1 input/output 14.
						O	**SCT0_OUT7 —** SCTimer0/PWM output 7.
PIO1_15	-	-	15	[5]	I; PU	IO	**PIO1_15 —** General purpose port 1 input/output 15.
PIO1_16	-	-	18	[5]	I; PU	IO	**PIO1_16 —** General purpose port 1 input/output 16.
PIO1_17/SCT1_OUT7	-	-	20	[5]	I; PU	IO	**PIO1_17 —** General purpose port 1 input/output 17.
						O	**SCT1_OUT7 —** SCTimer1/PWM output 7.
PIO1_18	-	-	25	[5]	I; PU	IO	**PIO1_18 —** General purpose port 1 input/output 18.
PIO1_19	-	-	29	[5]	I; PU	IO	**PIO1_19 —** General purpose port 1 input/output 19.
PIO1_20/SCT2_OUT5	-	-	34	[5]	I; PU	IO	**PIO1_20 —** General purpose port 1 input/output 20.
						O	**SCT2_OUT5 —** SCTimer2/PWM output 5.
PIO1_21	-	-	37	[5]	I; PU	IO	**PIO1_21 —** General purpose port 1 input/output 21.
PIO1_22	-	-	38	[5]	I; PU	IO	**PIO1_22 —** General purpose port 1 input/output 22.
PIO1_23	-	-	42	[5]	I; PU	IO	**PIO1_23 —** General purpose port 1 input/output 23.
PIO1_24/SCT3_OUT5	-	-	44	[5]	I; PU	IO	**PIO1_24 —** General purpose port 1 input/output 24.
						O	**SCT3_OUT5 —** SCTimer3/PWM output 5.
PIO1_25	-	-	46	[5]	I; PU	IO	**PIO1_25 —** General purpose port 1 input/output 25.
PIO1_26	-	-	48	[5]	I; PU	IO	**PIO1_26 —** General purpose port 1 input/output 26.
PIO1_27	-	-	50	[5]	I; PU	IO	**PIO1_27 —** General purpose port 1 input/output 27.
PIO1_28	-	-	55	[5]	I; PU	IO	**PIO1_28 —** General purpose port 1 input/output 28.
PIO1_29	-	-	56	[5]	I; PU	IO	**PIO1_29 —** General purpose port 1 input/output 29.
PIO1_30	-	-	59	[5]	I; PU	IO	**PIO1_30 —** General purpose port 1 input/output 30.
PIO1_31	-	-	60	[5]	I; PU	IO	**PIO1_31 —** General purpose port 1 input/output 31.
PIO2_0	-	-	62	[5]	I; PU	IO	**PIO2_0 —** General purpose port 2 input/output 0.
PIO2_1	-	-	64	[5]	I; PU	IO	**PIO2_1 —** General purpose port 2 input/output 1.
PIO2_2	-	-	72	[5]	I; PU	IO	**PIO2_2 —** General purpose port 2 input/output 2.
PIO2_3	-	-	76	[5]	I; PU	IO	**PIO2_3 —** General purpose port 2 input/output 3.
PIO2_4	-	-	77	[5]	I; PU	IO	**PIO2_4 —** General purpose port 2 input/output 4. On the LQFP100 package, this is the ISP_1 boot pin.
PIO2_5	-	-	80	[5]	I; PU	IO	**PIO2_5 —** General purpose port 2 input/output 5. On the LQFP100 package, this is the ISP_0 boot pin.
PIO2_6	-	-	82	[5]	I; PU	IO	**PIO2_6 —** General purpose port 2 input/output 6. On the LQFP100 package, this pin is assigned to U0_TXD in ISP USART mode.
PIO2_7	-	-	86	[5]	I; PU	IO	**PIO2_7 —** General purpose port 2 input/output 7. On the LQFP100 package, this pin is assigned to U0_RXD in ISP USART mode.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

8.3 On-chip flash programming memory

The LPC15xx contain up to 256 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software. Flash updates via USB are supported as well.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.3.1 ISP pin configuration

The LPC15xx supports ISP via the USART0, C_CAN, or USB interfaces. The ISP mode is determined by the state of two pins (ISP_0 and ISP_1) at boot time:

Table 6. ISP modes

Boot mode	ISP_0	ISP_1	Description
No ISP	HIGH	HIGH	ISP bypassed. Part attempts to boot from flash. If the user code in flash is not valid, then enters ISP via USB.
C_CAN	HIGH	LOW	Part enters ISP via C_CAN.
USB	LOW	HIGH	Part enters ISP via USB.
USART0	LOW	LOW	Part enters ISP via USART0.

The ISP pin assignment is different for each package, so that the fewest functions possible are blocked. No more than four pins must be set aside for entering ISP in any ISP mode. The boot code assigns two ISP pins for each package, which are probed when the part boots to determine whether or not to enter ISP mode. Once the ISP mode has been determined, the boot loader configures the necessary serial pins for each package.

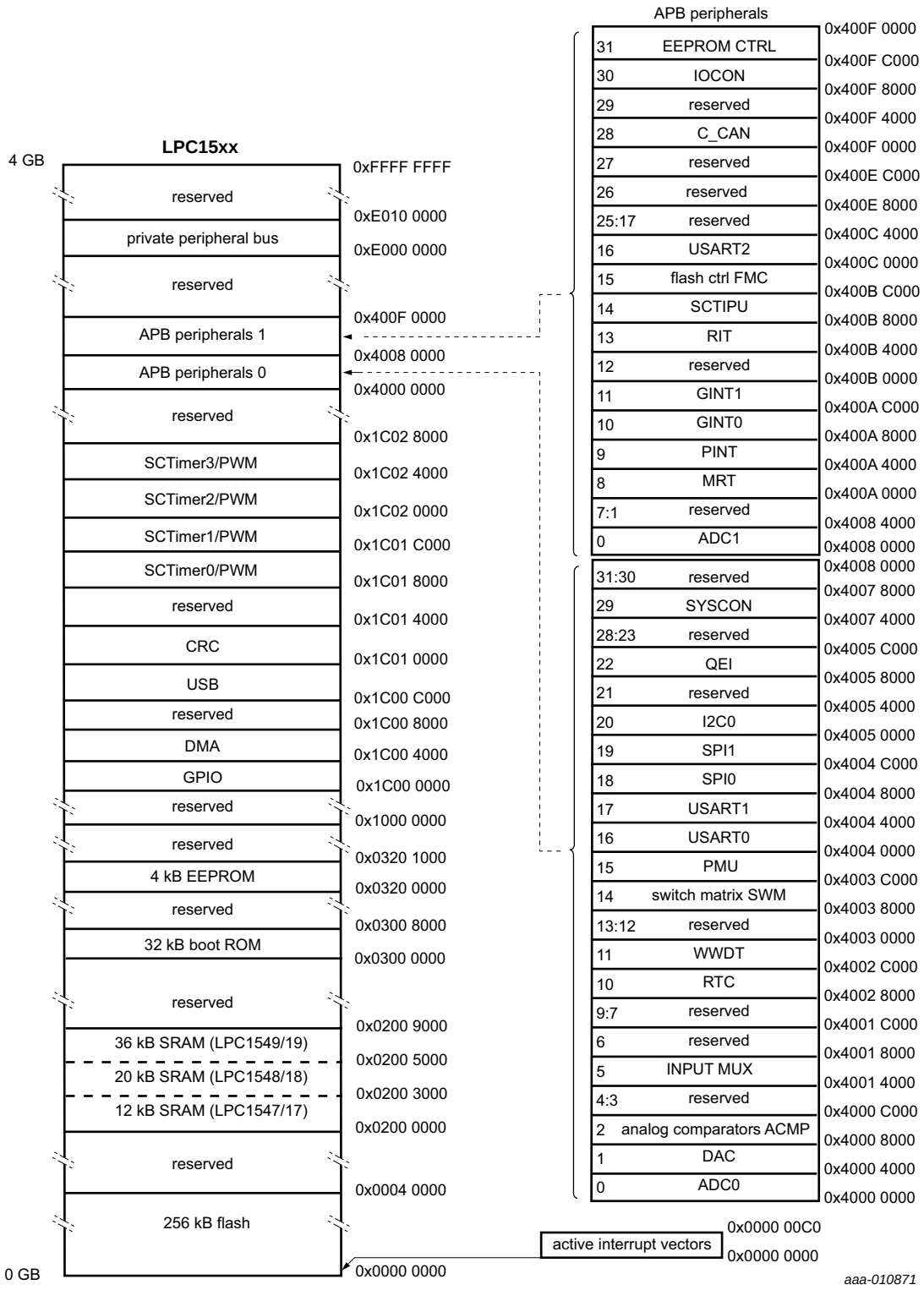
Pins which are not configured by the boot loader for the selected boot mode (for example CAN0_RD and CAN0_TD in USART mode) can be assigned to any function through the switch matrix.

Table 7. Pin assignments for ISP modes

Boot pin	LQFP48	LQFP64	LQFP100
ISP_0	PIO0_4	PIO1_9	PIO2_5
ISP_1	PIO0_16	PIO1_11	PIO2_4
USART mode			
U0_TXD	PIO0_15	PIO0_18	PIO2_6
U0_RXD	PIO0_14	PIO0_13	PIO2_7
C_CAN mode			
CAN0_TD	PIO0_18	PIO0_31	PIO2_8
CAN0_RD	PIO0_13	PIO0_11	PIO2_9
USB mode			
USB_VBUS (same as ISP_1)	PIO0_16	PIO1_11	PIO2_4

- Power mode configuration for configuring deep-sleep, power-down, and deep power-down modes.
- ADC drivers for analog-to-digital conversion and ADC calibration.

8.8 Memory map



See Section 8.5 “SRAM” for SRAM configuration.

Fig 10. Memory map

- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Selected events can limit, halt, start, or stop a counter.
- Events control state changes, outputs, interrupts, and DMA requests.
- Match register 0 can be used as an automatic limit.
- In bi-directional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can take place in the state while the counter is running.
  - A state changes into another state as result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- Integrated with an input pre-processing unit (SCTIPU) to combine or delay input events.

Inputs and outputs on the SCTimer2/PWM and SCTimer3/PWM are configured as follows:

- 3 inputs. Each input selects one of 21 sources from a pin multiplexer.
- 6 outputs (some outputs are connected to multiple locations)
  - Three outputs connected to external pins through the switch matrix as movable functions.
  - Three outputs connected to external pins through the switch matrix as fixed-pin functions.
  - Two outputs connected to the SCT IPU to sample or latch input events.
  - Four outputs connected to the accompanying large SCT
  - Two outputs connected to each ADC trigger input

8.22.5 SCT Input processing unit (SCTIPU)

The SCTIPU allows to block or propagate signals to inputs of the SCT under the control of an SCT output. Using the SCTIPU in this way, allows signals to be blocked from entering the SCT inputs for a certain amount of time, for example while they are known to be invalid.

In addition, the SCTIPU can generate a common signal from several combined input sources that can be selected on all SCT inputs. Such a mechanism can be useful to create an abort signal that stops all timers.

8.22.5.1 Features

The SCTIPU pre-processes inputs to the State-Configurable Timers (SCT).

- Four outputs created from a selection of input transitions. Each output can be used as abort input to the SCTs or for any other application which requires a collection of multiple SCT inputs to trigger an identical SCT response.

8.24.1 Features

- 12-bit successive approximation analog-to-digital converter.
- 12-bit conversion rate of 2 MHz.
- Input multiplexing among 12 pins and up to 4 internal sources.
- Internal sources are the temperature sensor voltage, internal reference voltage, core voltage regulator output, and VDDA/2.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

8.25 Digital-to-Analog Converter (DAC)

The DAC supports a resolution of 12 bits. Conversions can be triggered by an external pin input or an internal timer.

The DAC includes an optional automatic hardware shut-off feature which forces the DAC output voltage to zero while a HIGH level on the external DAC_SHUTOFF pin is detected.

8.25.1 Features

- 12-bit digital-to-analog converter.
- Supports DMA.
- Internal timer or pin external trigger for staged, jitter-free DAC conversion sequencing.
- Automatic hardware shut-off triggered by an external pin.

8.26 Analog comparator (ACMP)

The LPC15xx include four analog comparators with seven selectable inputs each for each positive or negative input channel. Two analog inputs are common to all four comparators. Internal voltage inputs include a voltage ladder reference with selectable voltage supply source, the temperature sensor or the internal voltage reference.

The analog inputs to the comparators are fixed-pin functions and must be enabled through the switch matrix.

The outputs of each analog comparator are internally connected to the ADC trigger inputs and to the SCT inputs, so that the result of a voltage comparison can trigger a timer operation or an analog-to-digital conversion.

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; VBAT = 0 or VBAT = 3.0 V [3][12][13]				
		RTC oscillator running				
		T_{amb} = 25 °C	-	1.1	1.3[14]	µA
		T_{amb} = 105 °C	-	-	15	µA
		RTC oscillator input grounded; T_{amb} = 25 °C [3][12]	-	560	-	nA
I_{BAT}	battery supply current	Deep power-down mode; V_{DD} = V_{DDA} = 3.3 V; VBAT = 3.0 V [13]		0	-	nA
		V_{DD} and V_{DDA} tied to ground; VBAT = 3.0 V [13]		1	-	µA
Standard port pins configured as digital pins, $\overline{\text{RESET}}$; see Figure 17						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10[14]	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10[14]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10[14]	nA
V_I	input voltage	$V_{DD} \geq$ 2.4 V; 5 V tolerant pins except PIO0_12 [16] [18]	0	-	5	V
		$V_{DD} \geq$ 2.4 V; on 3 V tolerant pin PIO0_12	0	-	V_{DDA}	
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage	2.4 V <= V_{DD} < 3.0 V	0.30	-	-	V
		3.0 V <= V_{DD} <= 3.6 V	0.35	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V	4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [19]	-	-	-45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [19]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V;	−10	−50	−85	µA
		V_{DD} < V_I < 5 V	0	0	0	µA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

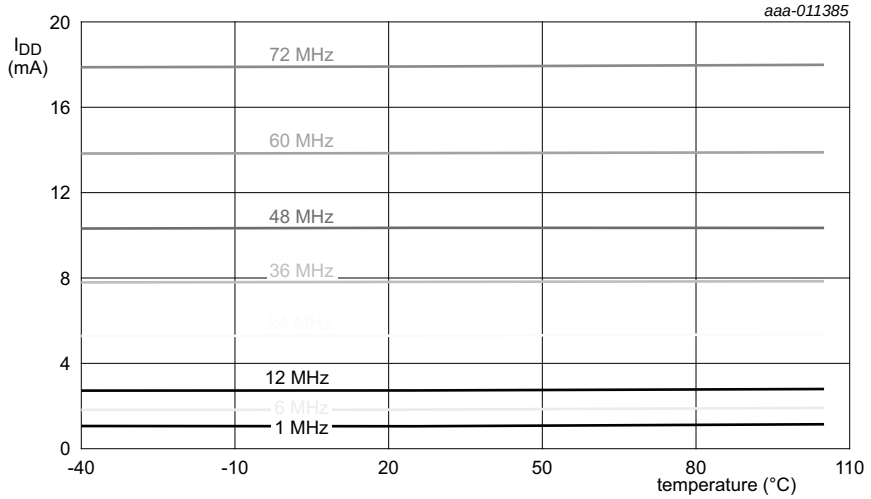
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.7 V <= V_{DD} < 3.6 V	20	-	-	mA
		V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.4 V <= V_{DD} < 2.7 V	16	-	-	mA
I_{LI}	input leakage current	V_I = V_{DD} [21]	-	2	4	µA
		V_I = 5 V	-	10	22	µA
USB_DM and USB_DP pins						
V_I	input voltage	[2]	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		1.8	-	-	V
V_{IL}	LOW-level input voltage		-	-	1.0	V
V_{hys}	hysteresis voltage		0.32	-	-	V
Z_{out}	output impedance		28	-	44	Ω
V_{OH}	HIGH-level output voltage		2.9	-	-	V
V_{OL}	LOW-level output voltage		-	-	0.18	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.3 V [22]	4.8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.3 V [22]	5.0	-	-	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; pad connected to ground	-	-	125	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; pad connected to ground	-	-	125	mA
Oscillator pins						
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN	−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT	−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN [23]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT [23]	−0.5	-	3.6	V
Pin capacitance						
C_{io}	input/output capacitance	pins with analog and digital functions [24]	-	-	7.1	pF
		I^2C-bus pins (PIO0_22 and PIO0_23) [24]	-	-	2.5	pF
		pins with digital functions only [24]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] For USB operation: 3.0 V ≤ V_{DD} ≤ 3.6 V.

[3] T_{amb} = 25 °C.

[4] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.



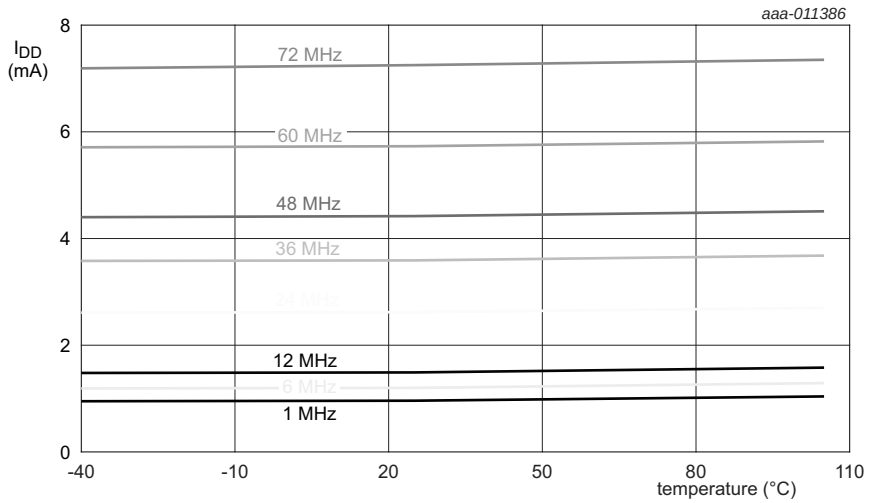
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 19. Active mode: Typical supply current I_{DD} versus temperature



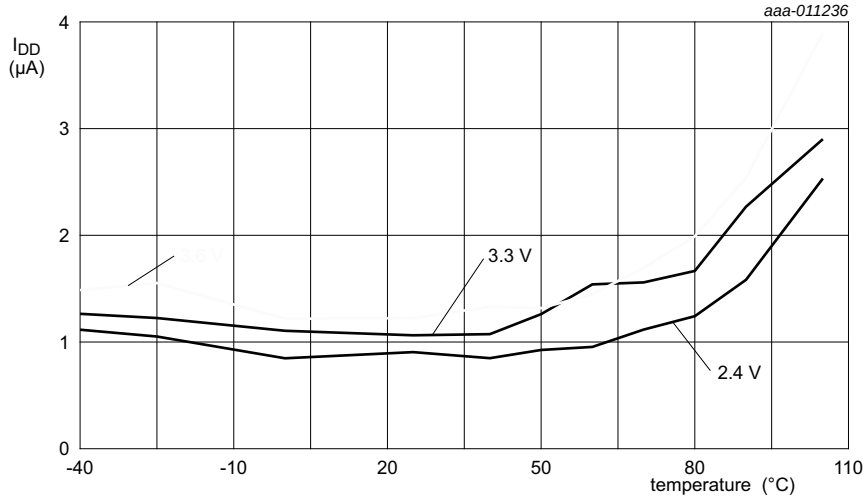
Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

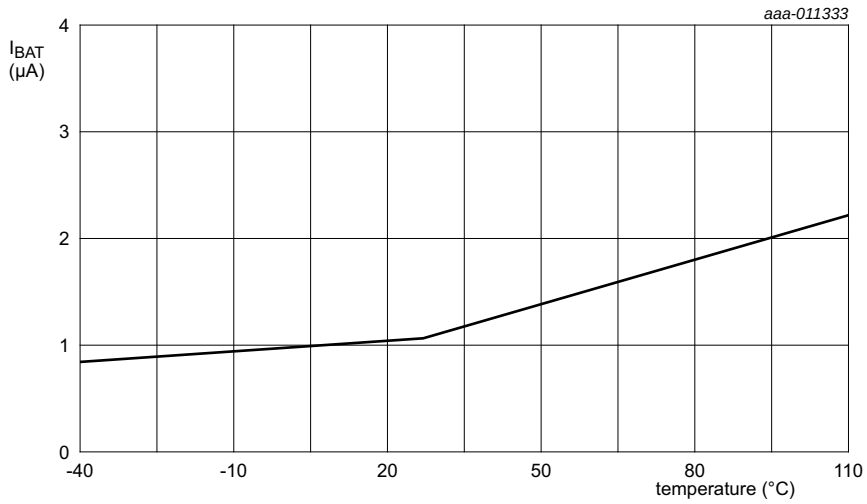
24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 20. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



VBAT = 0 V.

Fig 23. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



VBAT = 3.3 V; V_{DD} floating.

Fig 24. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

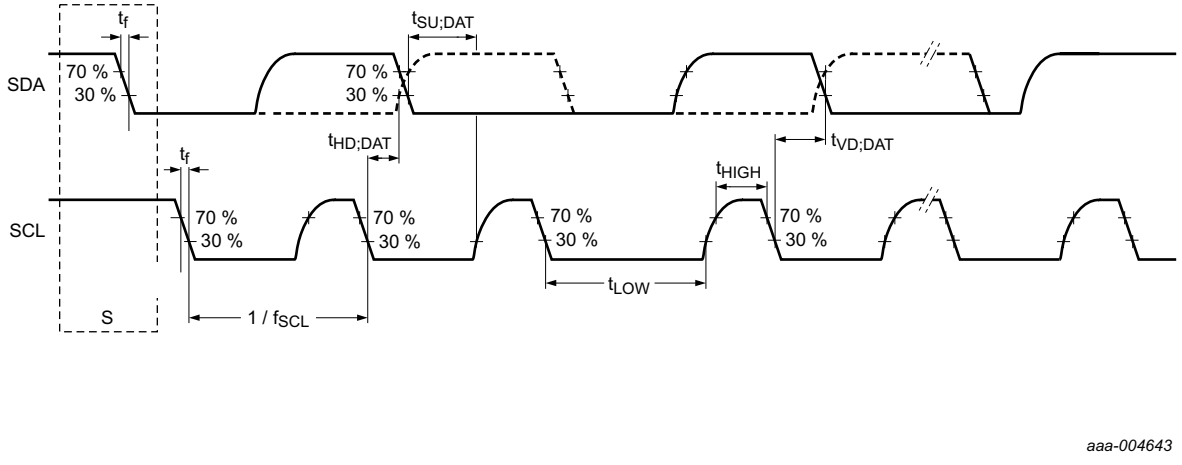


Fig 35. I²C-bus pins clock timing

14.8 Pin states in different power modes

Table 35. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_22, PIO0_23 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$/PIO0_21	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, addan external pull-up to the $\overline{\text{RESET}}$ pin to reduce power consumption.
PIO0_17/ WAKEUP/$\overline{\text{TRST}}$	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

14.9 ElectroMagnetic Compatibility (EMC)

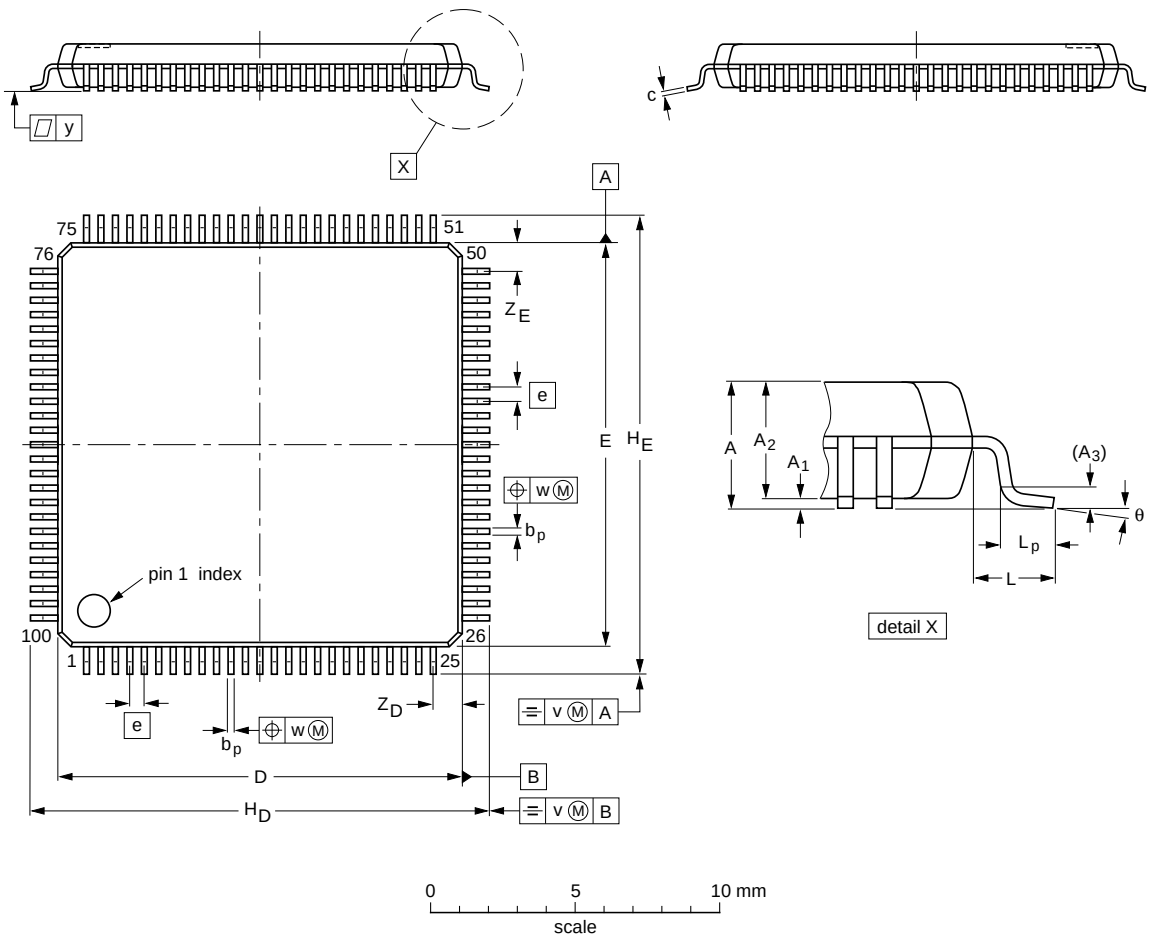
Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1549JBD100.

Table 36. ElectroMagnetic Compatibility (EMC) for part LPC1549 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =						Unit
		12 MHz	24 MHz	36 MHz	48 MHz	60 MHz	72 MHz	
Input clock: IRC (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-5	-1	-5	-4	-3	0	dBμV
	30 MHz to 150 MHz	-1	+3	+6	+8	+11	+14	dBμV
	150 MHz to 1 GHz	-1	+2	+5	+10	+9	+11	dBμV
IEC level[1]	-	O	O	O	N	N	M	-
Input clock: crystal oscillator (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-2	0	-5	-2	-2	2	dBμV
	30 MHz to 150 MHz	0	+3	+6	+8	+12	+14	dBμV
	150 MHz to 1 GHz	-1	+3	+5	+10	+10	+11	dBμV
IEC level[1]	-	O	O	O	N	N	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 52. Package outline LQFP100 (SOT407-1)

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