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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1518jbd64e

- ROM API support:
  - Boot loader with boot options from flash or external source via USART, C_CAN, or USB
  - USB drivers
  - ADC drivers
  - SPI drivers
  - USART drivers
  - I2C drivers
  - Power profiles and power mode configuration with low-power mode configuration option
  - DMA drivers
  - C_CAN drivers
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - Simple DMA engine with 18 channels and 20 programmable input triggers.
  - High-speed GPIO interface with up to 76 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, open-drain mode, input inverter, and programmable digital glitch filter.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight external inputs.
  - Two GPIO grouped port interrupts.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - Quadrature Encoder Interface (QEI).
- Configurable PWM/timer/motor control subsystem:
  - Up to four 32-bit counter/timers or up to eight 16-bit counter/timers or combinations of 16-bit and 32-bit timers.
  - Up to 28 match outputs and 22 configurable capture inputs with input multiplexer.
  - Up to 28 PWM outputs total.
  - Dither engine for improved average resolution of pulse edges.
  - Four State Configurable Timers (SCTimers) for highly flexible, event-driven timing and PWM applications.
  - SCT Input Pre-processor Unit (SCTIPU) for processing timer inputs and immediate handling of abort situations.
  - Integrated with ADC threshold compare interrupts, temperature sensor, and analog comparator outputs for motor control feedback using analog signals.
- Special-application and simple timers:
  - 24-bit, four-channel, multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Repetitive interrupt timer for general purpose use.
  - Windowed Watchdog timer (WWDT).
  - High-resolution 32-bit Real-time clock (RTC) with selectable 1 s or 1 ms time resolution running in the always-on power domain. RTC can be used for wake-up from all low power modes including Deep power-down.

- Single power supply 2.4 V to 3.6 V.
- Temperature range −40 °C to +105 °C.
- Available as LQFP100, LQFP64, and LQFP48 packages.

3. Applications

- Motor control
- Motion drives
- Digital power supplies
- Industrial and medical
- Solar inverters
- Home appliances
- Building and factory automation

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1549JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1549JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1549JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1548JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1548JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1519JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1519JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1518JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1518JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_27/ACMP_I1	46	62	97	[2]	I; PU	IO	**PIO0_27 —** General purpose port 0 input/output 27.
						A	**ACMP_I1 —** Analog comparator common input 1.
PIO0_28/ACMP1_I3	47	63	98	[2]	I; PU	IO	**PIO0_28 —** General purpose port 0 input/output 28.
						A	**ACMP1_I3 —** Analog comparator 1 input 3.
PIO0_29/ACMP2_I3/ SCT2_OUT4	48	64	100	[2]	I; PU	IO	**PIO0_29 —** General purpose port 0 input/output 29.
						A	**ACMP2_I3 —** Analog comparator 2 input 3.
						O	**SCT2_OUT4 —** SCTimer2/PWM output 4.
PIO0_30/ADC0_11	-	1	1	[2]	I; PU	IO	**PIO0_30 —** General purpose port 0 input/output 30.
						A	**ADC0_11 —** ADC0 input 11.
PIO0_31/ADC0_9	-	3	3	[2]	I; PU	IO	**PIO0_31 —** General purpose port 0 input/output 31. On the LQFP64 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						A	**ADC0_9 —** ADC0 input 9.
PIO1_0/ADC0_8	-	4	5	[2]	I; PU	IO	**PIO1_0 —** General purpose port 1 input/output 0.
						A	**ADC0_8 —** ADC0 input 8.
PIO1_1/ADC1_0	-	15	23	[2]	I; PU	IO	**PIO1_1 —** General purpose port 1 input/output 1.
						A	**ADC1_0 —** ADC1 input 0.
PIO1_2/ADC1_4	-	25	36	[2]	I; PU	IO	**PIO1_2 —** General purpose port 1 input/output 2.
						A	**ADC1_4 —** ADC1 input 4.
PIO1_3/ADC1_5	-	28	41	[2]	I; PU	IO	**PIO1_3 —** General purpose port 1 input/output 3.
						A	**ADC1_5 —** ADC1 input 5.
PIO1_4/ADC1_10	-	33	51	[2]	I; PU	IO	**PIO1_4 —** General purpose port 1 input/output 4.
						A	**ADC1_10 —** ADC1 input 10.
PIO1_5/ADC1_11	-	34	52	[2]	I; PU	IO	**PIO1_5 —** General purpose port 1 input/output 5.
						A	**ADC1_11 —** ADC1 input 11.
PIO1_6/ACMP_I2	-	46	73	[2]	I; PU	IO	**PIO1_6 —** General purpose port 1 input/output 6.
						A	**ACMP_I2 —** Analog comparator common input 2.
PIO1_7/ACMP3_I4	-	51	81	[2]	I; PU	IO	**PIO1_7 —** General purpose port 1 input/output 7.
						A	**ACMP3_I4 —** Analog comparator 3 input 4.
PIO1_8/ACMP3_I3/ SCT3_OUT4	-	53	84	[2]	I; PU	IO	**PIO1_8 —** General purpose port 1 input/output 8.
						A	**ACMP3_I3 —** Analog comparator 3 input 3.
						O	**SCT3_OUT4 —** SCTimer3/PWM output 4.
PIO1_9/ACMP2_I4	-	54	85	[2]	I; PU	IO	**PIO1_9 —** General purpose port 1 input/output 9. On the LQFP64 package, this is the ISP_0 boot pin.
						A	**ACMP2_I4 —** Analog comparator 2 input 4.
PIO1_10/ACMP1_I4	-	59	91	[2]	I; PU	IO	**PIO1_10 —** General purpose port 1 input/output 10.
						A	**ACMP1_I4 —** Analog comparator 1 input 4.
PIO1_11	-	38	58	[5]	I; PU	IO	**PIO1_11 —** General purpose port 1 input/output 11. On the LQFP64 package, this is the ISP_1 boot pin.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

8.3 On-chip flash programming memory

The LPC15xx contain up to 256 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software. Flash updates via USB are supported as well.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.3.1 ISP pin configuration

The LPC15xx supports ISP via the USART0, C_CAN, or USB interfaces. The ISP mode is determined by the state of two pins (ISP_0 and ISP_1) at boot time:

Table 6. ISP modes

Boot mode	ISP_0	ISP_1	Description
No ISP	HIGH	HIGH	ISP bypassed. Part attempts to boot from flash. If the user code in flash is not valid, then enters ISP via USB.
C_CAN	HIGH	LOW	Part enters ISP via C_CAN.
USB	LOW	HIGH	Part enters ISP via USB.
USART0	LOW	LOW	Part enters ISP via USART0.

The ISP pin assignment is different for each package, so that the fewest functions possible are blocked. No more than four pins must be set aside for entering ISP in any ISP mode. The boot code assigns two ISP pins for each package, which are probed when the part boots to determine whether or not to enter ISP mode. Once the ISP mode has been determined, the boot loader configures the necessary serial pins for each package.

Pins which are not configured by the boot loader for the selected boot mode (for example CAN0_RD and CAN0_TD in USART mode) can be assigned to any function through the switch matrix.

Table 7. Pin assignments for ISP modes

Boot pin	LQFP48	LQFP64	LQFP100
ISP_0	PIO0_4	PIO1_9	PIO2_5
ISP_1	PIO0_16	PIO1_11	PIO2_4
USART mode			
U0_TXD	PIO0_15	PIO0_18	PIO2_6
U0_RXD	PIO0_14	PIO0_13	PIO2_7
C_CAN mode			
CAN0_TD	PIO0_18	PIO0_31	PIO2_8
CAN0_RD	PIO0_13	PIO0_11	PIO2_9
USB mode			
USB_VBUS (same as ISP_1)	PIO0_16	PIO1_11	PIO2_4

8.4 EEPROM

The LPC15xx contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

8.5 SRAM

The LPC15xx contain a total 36 kB, 20 kB or 12 kB of contiguous, on-chip static RAM memory. For each SRAM configuration, the SRAM is divided into three blocks: 2 x 16 kB + 4 kB for 36 kB SRAM, 2 x 8 kB + 4 kB for 20 kB SRAM, and 2 x 4 kB + 4 kB for 12 kB SRAM. The bottom 16 kB, 8 kB, or 4 kB are enabled by the bootloader and cannot be disabled. The next two SRAM blocks in each configuration can be disabled or enabled individually in the SYSCON block to save power.

Table 8. LPC15xx SRAM configurations

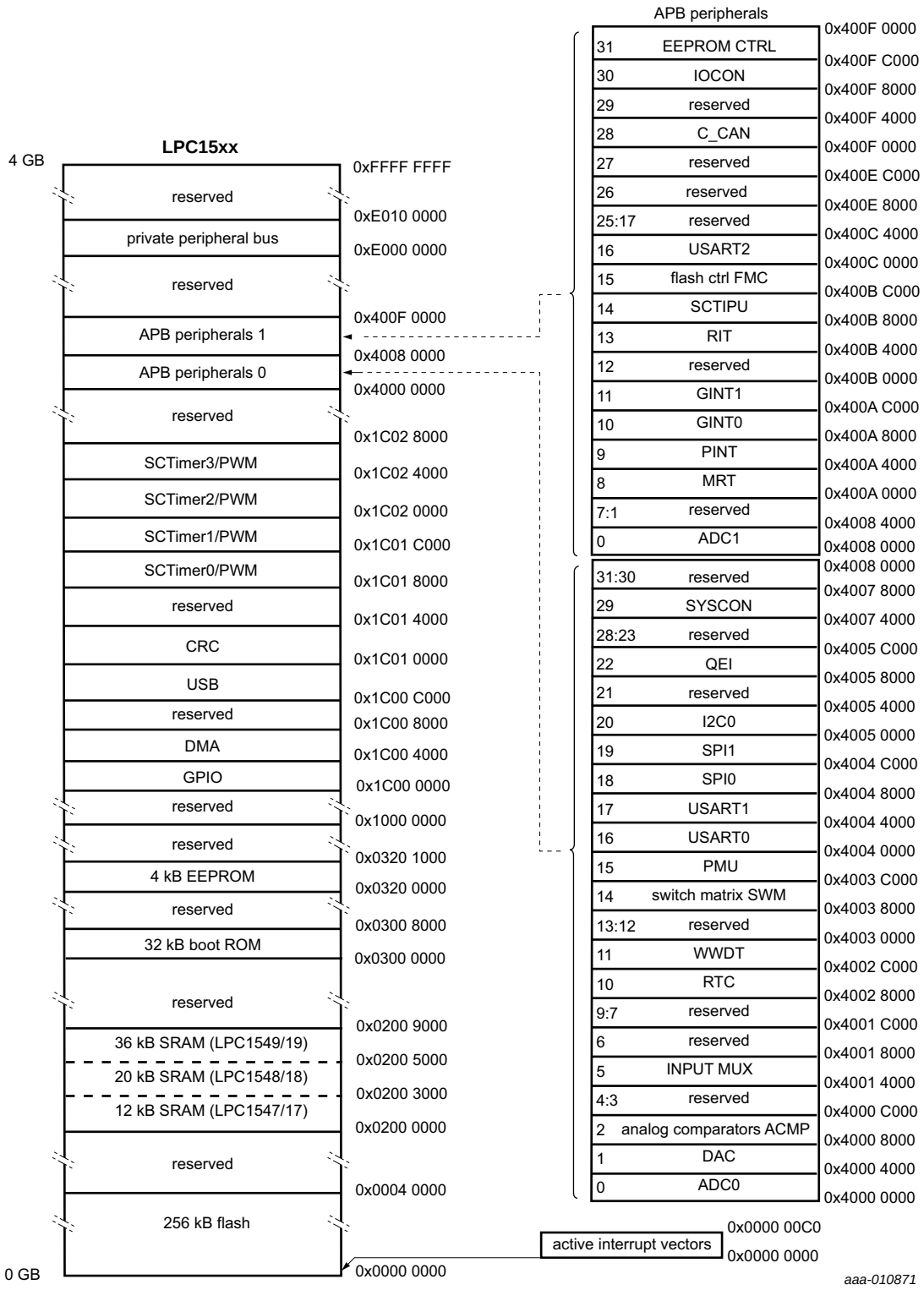
	SRAM0	SRAM1	SRAM2
LPC1549/19 (total SRAM = 36 kB)			
address range	0x0200 0000 to 0x0200 3FFF	0x0200 4000 to 0x0200 7FFF	0x0200 8000 to 0x0200 8FFF
size	16 kB	16 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1548/18 (total SRAM = 20 kB)			
address range	0x0200 0000 to 0x0200 1FFF	0x0200 2000 to 0x0200 3FFF	0x0200 4000 to 0x0200 4FFF
size	8 kB	8 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1547/17 (total SRAM = 12 kB)			
address range	0x0200 0000 to 0x0200 0FFF	0x0200 1000 to 0x0200 1FFF	0x0200 2000 to 0x0200 2FFF
size	4 kB	4 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled

8.6 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Flash updates via USB and C_CAN supported.
- USB API (HID, CDC, and MSC drivers).
- DMA, I2C, USART, SPI, and C_CAN drivers.
- Power profiles for configuring power consumption and PLL settings.

8.8 Memory map



See Section 8.5 “SRAM” for SRAM configuration.

Fig 10. Memory map

8.9 Nested Vectored Interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.9.1 Features

- Nested Vectored Interrupt Controller that is an integral part of the ARM Cortex-M3.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- The NVIC supports 47 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Support for NMI.
- ARM Cortex-M3 Vector table offset register VTOR implemented.

8.9.2 Interrupt sources

Typically, each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.10 IOCON block

The IOCON block configures the electrical properties of the pins such as pull-up and pull-down resistors, hysteresis, open-drain modes and input filters.

Remark: The pin function and whether the pin operates in digital or analog mode are entirely under the control of the switch matrix.

Enabling an analog function through the switch matrix disables the digital pad. However, the internal pull-up and pull-down resistors as well as the pin hysteresis must be disabled to obtain an accurate reading of the analog input.

8.10.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All pins (except PIO0_22 and PIO0_23) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable (on/off) 10 ns glitch filter on 36 pins (PIO0_0 to PIO0_17, PIO0_25 to PIO0_31, PIO1_0 to PIO1_10). The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.
- Digital filter with programmable filter constant on all pins.

8.10.2 Standard I/O pad configuration

Figure 11 shows the possible pin modes for standard I/O pins with analog input function:

8.12 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function through the switch matrix are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC15xx use accelerated GPIO functions.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.12.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.13 Pin interrupt/pattern match engine (PINT)

The pin interrupt block configures up to eight pins from the digital pins on ports 1 and 2 for providing eight external interrupts connected to the NVIC. The input multiplexer block is used to select the pins.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin on ports 0 and 1 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.13.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU.
  - The pattern match engine does not facilitate wake-up.

- Four registers to indicate which specific input sources caused the abort input to the SCTs.
- Four additional outputs which can be sampled at certain times and latched at others before being routed to SCT inputs.
- Nine abort inputs. Any combination of the abort inputs can trigger the dedicated abort input of each SCT.

8.23 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.23.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clock and direction).

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are internal connections to other on-chip peripherals such as the SCT and analog comparator outputs, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions.

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCT inputs for tight timing control between the ADC and the SCTs.

8.38 Clock output

The LPC15xx feature a clock output function that routes the internal oscillator outputs, the PLL outputs, or the main clock an output pin where they can be observed directly.

8.39 Wake-up process

The LPC15xx begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the system oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and system oscillator as a clock source.

8.40 Power control

The LPC15xx support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides additional power control.

8.40.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC15xx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock and to easily set the configuration options for Deep-sleep and power-down modes.

Remark: When using the USB, configure the LPC15xx in Default mode.

8.40.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

8.41 System control

8.41.1 Reset

Reset has four sources on the LPC15xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

The $\overline{\text{RESET}}$ pin is operational in active, sleep, deep-sleep, and power-down modes if the $\overline{\text{RESET}}$ function is selected through the switch matrix for pin PIO0_21 (this is the default). A LOW-going pulse as short as 50 ns executes the reset and thereby wakes up the part to its active state. The $\overline{\text{RESET}}$ pin is not functional in Deep power-down mode and must be pulled HIGH externally while the part is in Deep power-down mode.

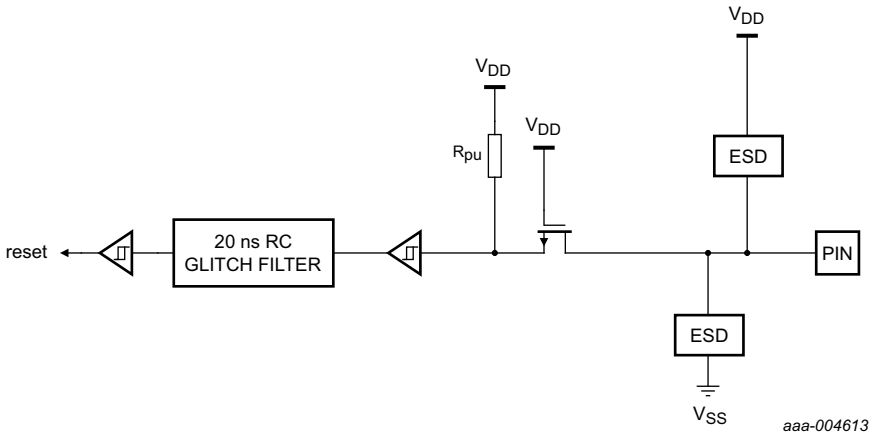


Fig 16. $\overline{\text{RESET}}$ pin configuration

8.41.2 Brownout detection

The LPC15xx includes brown-out detection (BOD) with two levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of two selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels can be selected to cause a forced reset of the chip.

8.41.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

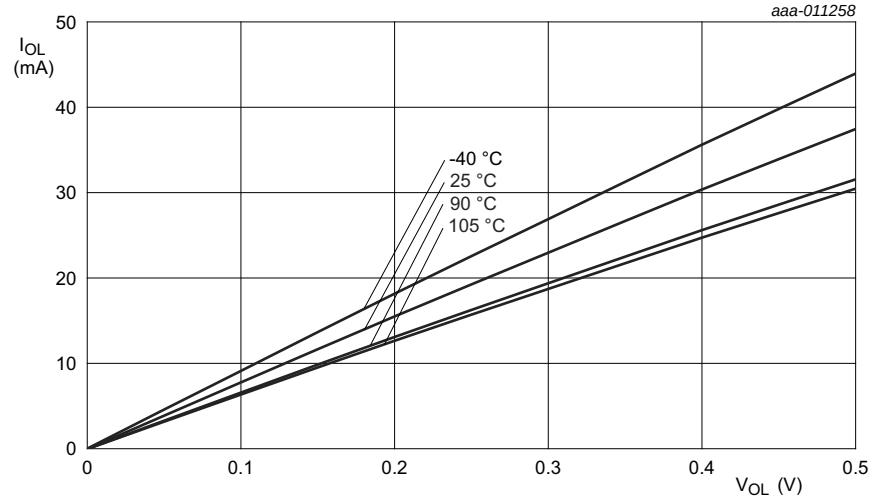
The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

11. Static characteristics

Table 11. Static characteristics

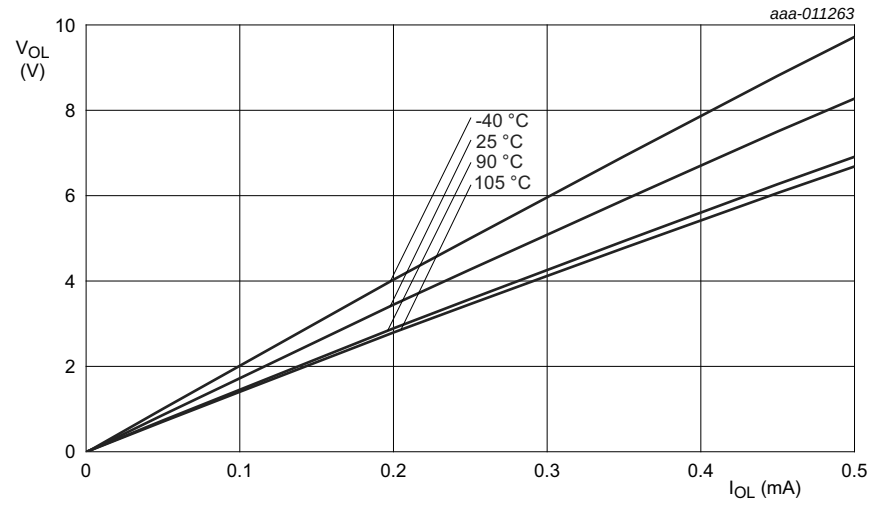
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)	[2]	2.4	3.3	V_{DDA}	V
V_{DDA}	analog supply voltage		2.4	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP_DAC_VDDCMP	2.4	-	V_{DDA}	V
		on pin VREFP_ADC	-	-	V_{DDA}	V
V_{BAT}	battery supply voltage		2.4	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	4.3	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.7	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	19.3	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	18	-	mA
		Sleep mode;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.1	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	1.5	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	8.0	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	7.3	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; [3][4][11]	-			
		T_{amb} = 25 °C		310	380	µA
		T_{amb} = 105 °C	-	-	620	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V [3][4][11]	-			
		T_{amb} = 25 °C		3.8	15	µA
		T_{amb} = 105 °C	-	-	163	µA



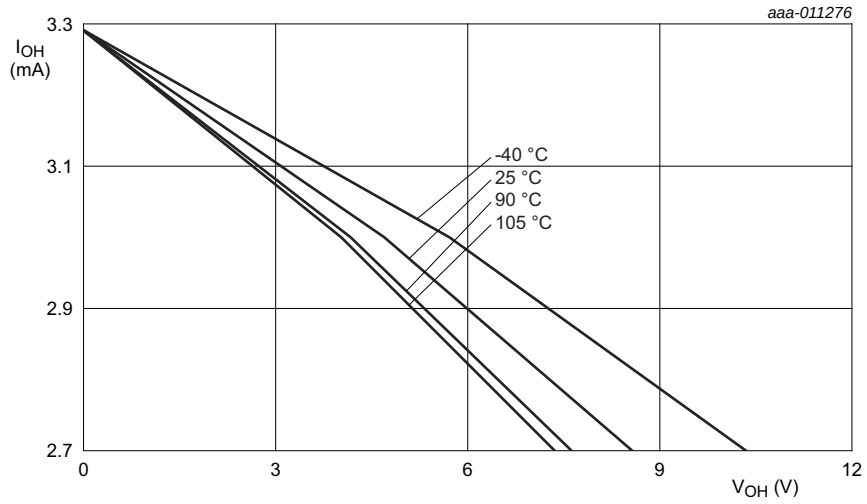
Conditions: V_{DD} = 3.3 V; on pins PIO0_22 and PIO0_23.

Fig 28. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



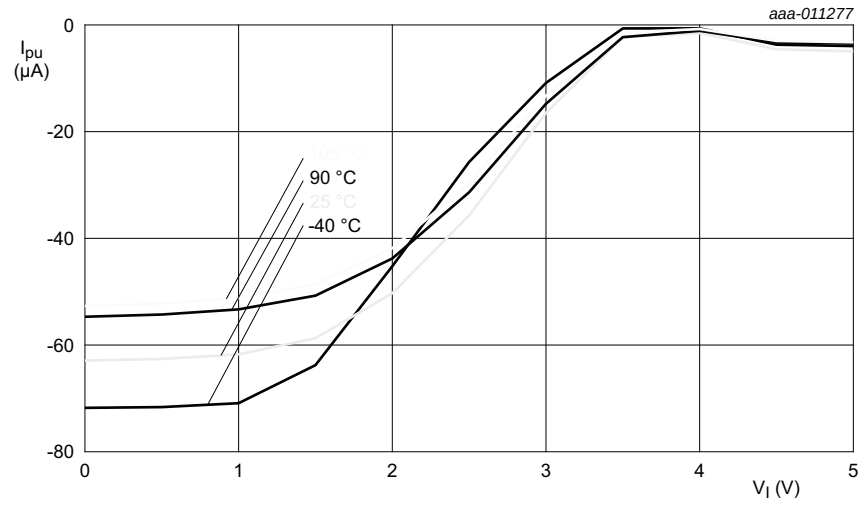
Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_24.

Fig 29. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 30. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



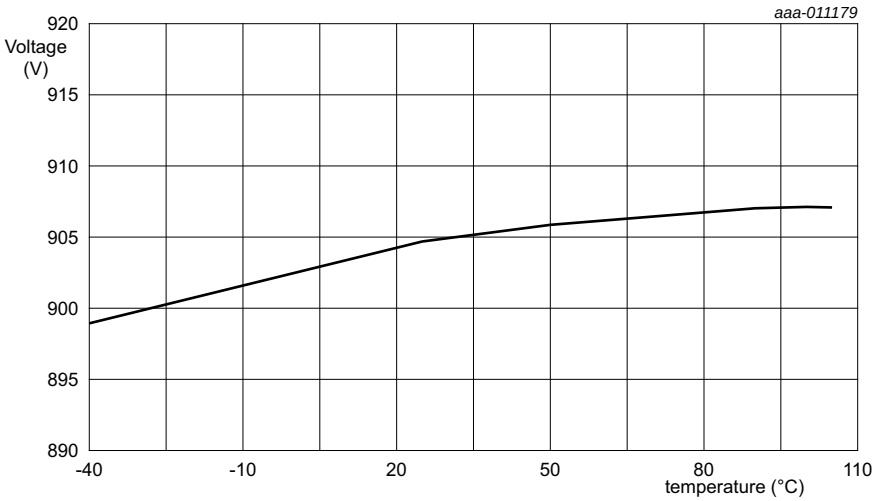
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 31. Typical pull-up current I_{pu} versus input voltage V_I

Table 26. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = −40 °C to +105 °C [1]	875	-	925	mV
		T_{amb} = 25 °C		905		mV
$t_{s(pu)}$	power-up settling time	to 99% of V_O	-	-	125	µs

[1] Maximum and minimum values are measured on samples from the corners of the process matrix lot.



V_{DDA} = 3.3 V; averaged over process corners

Fig 42. Average internal voltage reference output voltage

Table 27. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C [1]	-	-	5	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C	-	-	5	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value [2][3]	-	81	110	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models). Maximum values are derived from worst case simulation (V_{DDA} = 2.6 V; T_{amb} = 105 °C; slow process models).

[3] Internal voltage reference must be powered before the temperature sensor can be turned on.

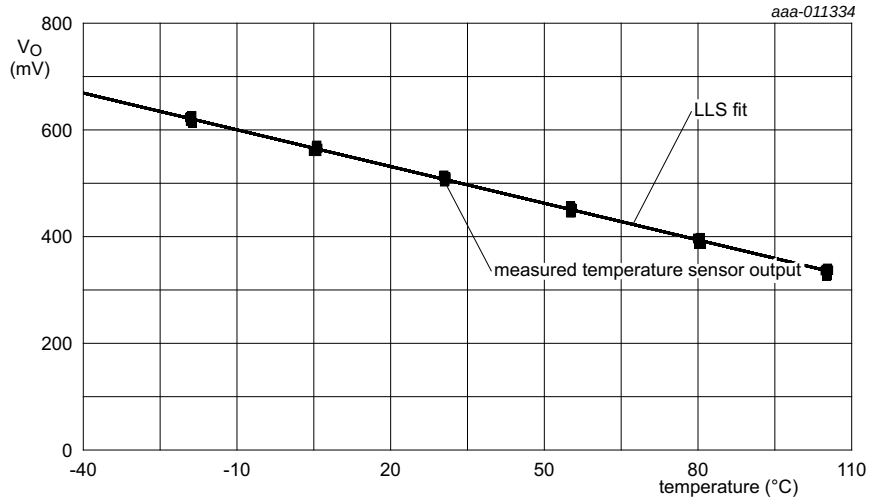
[4] Settling time applies to switching between comparator and ADC channels.

Table 28. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range	Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C [1]	-	-2.29	-	mV/°C
LLS intercept at 0 °C	T_{amb} = −40 °C to +105 °C [1]	-	577.3	-	mV
Value at 30 °C	[2]	502	-	514	mV

[1] Measured over matrix samples.

[2] Measured for samples over process corners.



V_{DDA} = 3.3 V; measured on matrix samples.

Fig 43. LLS fit of the temperature sensor output voltage

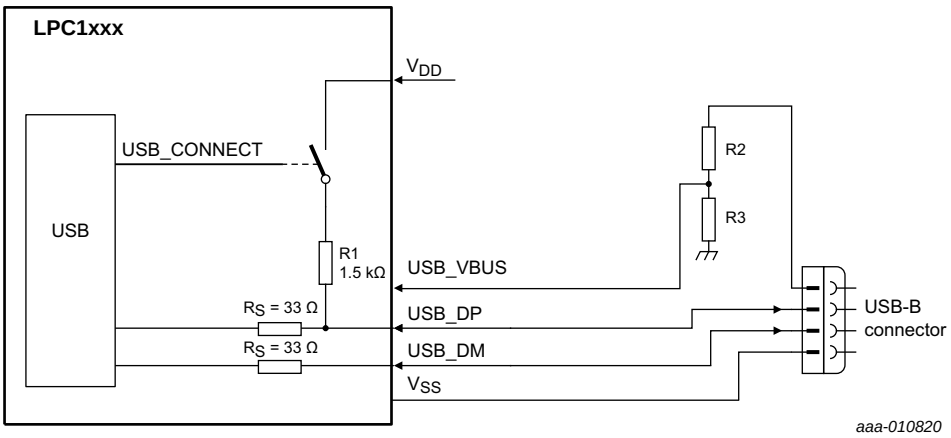


Fig 44. USB interface on a self-powered device where USB_VBUS = 5 V

For a bus-powered device, the VBUS signal does not need to be connected to the USB_VBUS pin (see Figure 45). The USB_CONNECT function can additionally be enabled internally by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required for the USB_CONNECT functionality.

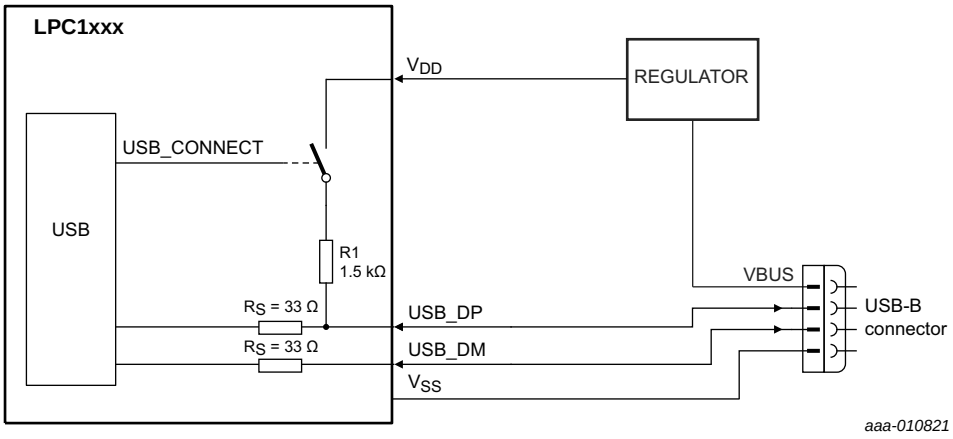


Fig 45. USB interface on a bus-powered device

Remark: When a bus-powered circuit as shown in Figure 45 is used or, for a self-powered device, when the VBUS pin is not connected, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) in the IOCON block. This ties the VBUS signal HIGH internally.

14.2.1 USB Low-speed operation

The USB device controller can be used in low-speed mode supporting 1.5 Mbit/s data exchange with a USB host controller.

Remark: To operate in low-speed mode, change the board connections as follows:

1. Connect USB_DP to the D- pin of the connector.
2. Connect USB_DM to the D+ pin of the connector.

14.5 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 48. If the RTC is not used, the RTCXIN pin can be grounded.

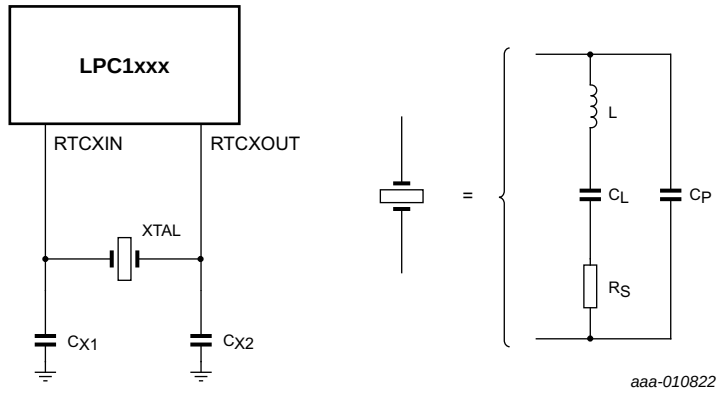


Fig 48. RTC oscillator components

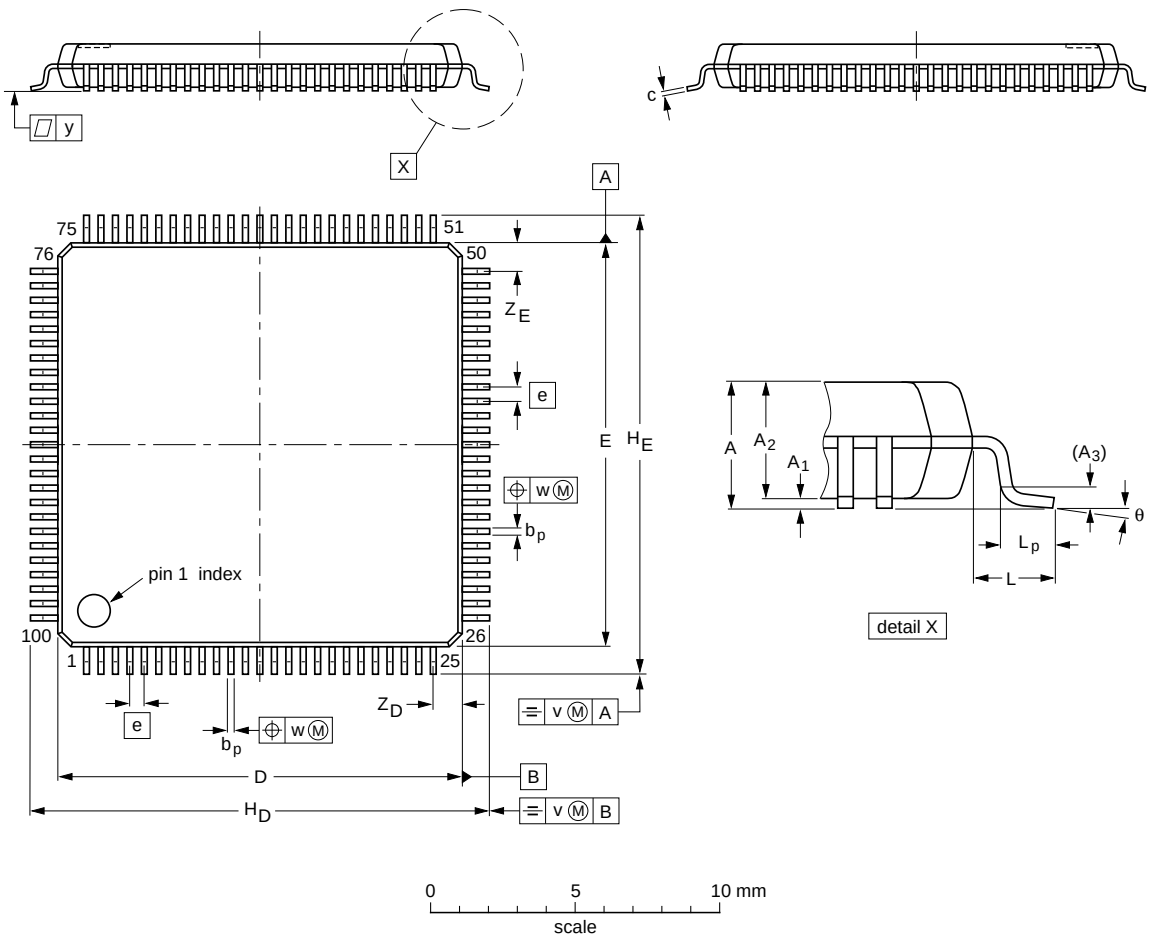
Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry.The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If the external crystal's load capacitance is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$C_{x1} = C_{x2} = 2 \times C_L - C_P$

14.6 Connecting power, clocks, and debug functions

Figure 49 shows the basic board connections used to power the LPC15xx, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

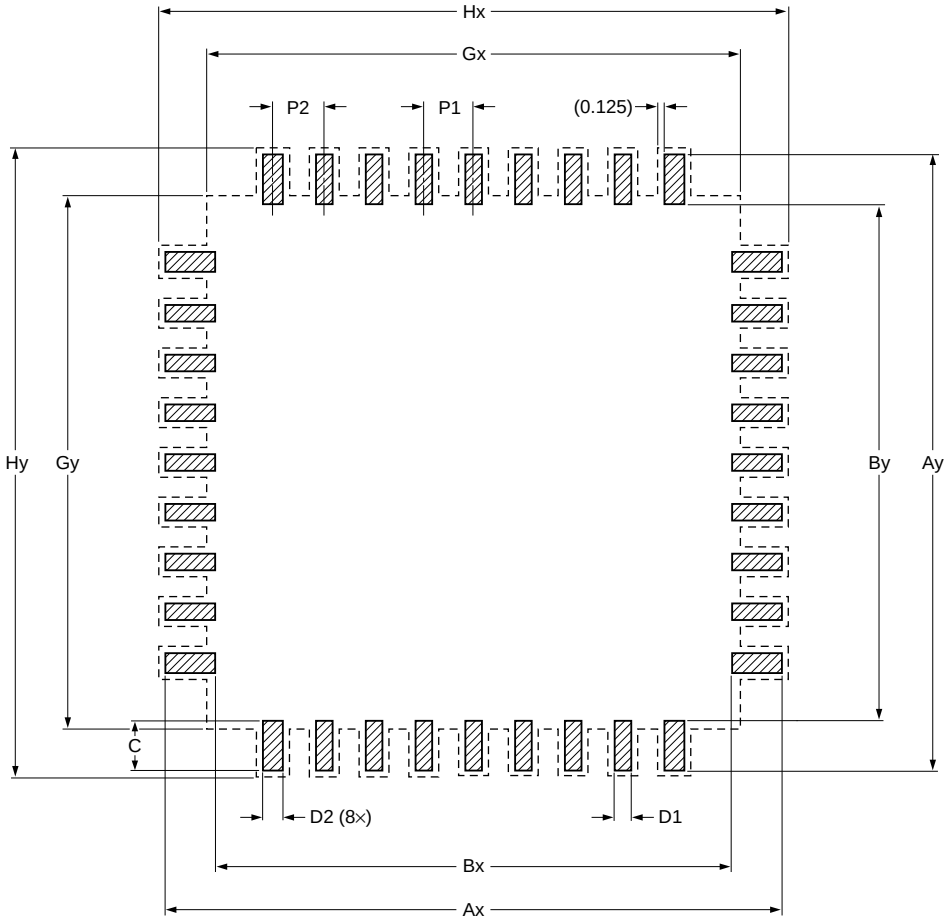
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 52. Package outline LQFP100 (SOT407-1)

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 54. Reflow soldering for the LQFP64 package