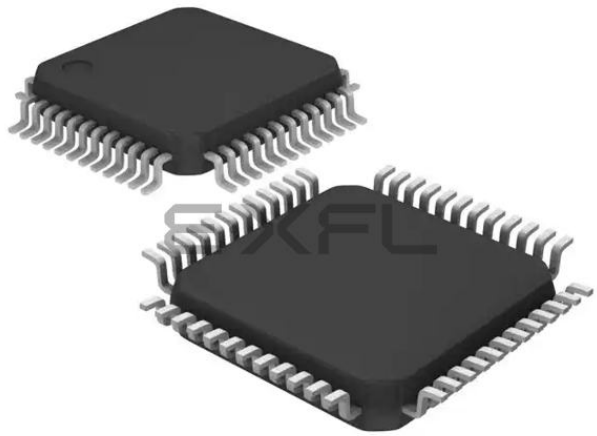

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	30
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1547jbd48ql

7. Pinning information

7.1 Pinning

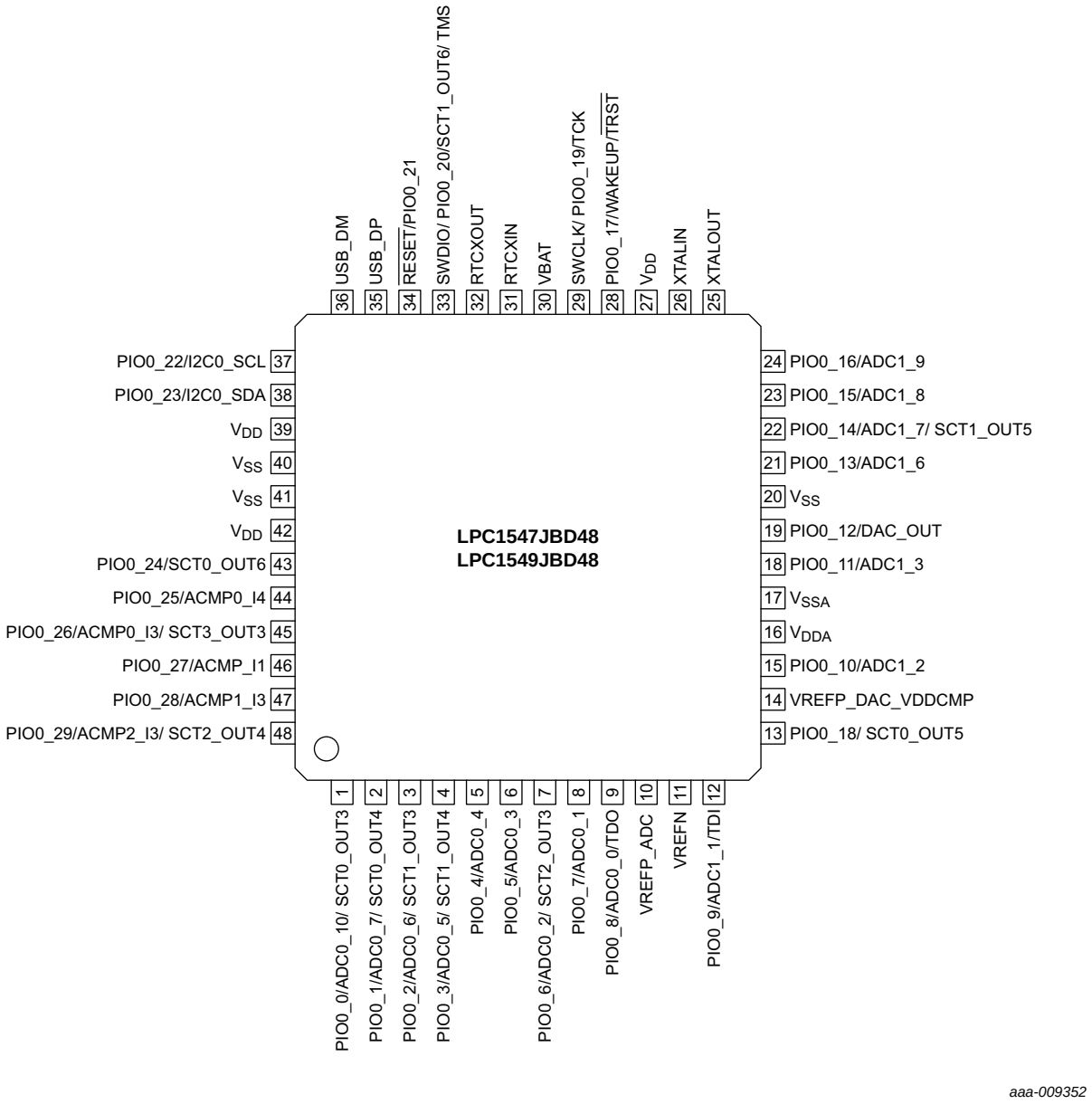


Fig 4. LQFP48 pin configuration (with USB)

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_27/ACMP_I1	46	62	97	[2]	I; PU	IO	**PIO0_27 —** General purpose port 0 input/output 27.
						A	**ACMP_I1 —** Analog comparator common input 1.
PIO0_28/ACMP1_I3	47	63	98	[2]	I; PU	IO	**PIO0_28 —** General purpose port 0 input/output 28.
						A	**ACMP1_I3 —** Analog comparator 1 input 3.
PIO0_29/ACMP2_I3/ SCT2_OUT4	48	64	100	[2]	I; PU	IO	**PIO0_29 —** General purpose port 0 input/output 29.
						A	**ACMP2_I3 —** Analog comparator 2 input 3.
						O	**SCT2_OUT4 —** SCTimer2/PWM output 4.
PIO0_30/ADC0_11	-	1	1	[2]	I; PU	IO	**PIO0_30 —** General purpose port 0 input/output 30.
						A	**ADC0_11 —** ADC0 input 11.
PIO0_31/ADC0_9	-	3	3	[2]	I; PU	IO	**PIO0_31 —** General purpose port 0 input/output 31. On the LQFP64 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						A	**ADC0_9 —** ADC0 input 9.
PIO1_0/ADC0_8	-	4	5	[2]	I; PU	IO	**PIO1_0 —** General purpose port 1 input/output 0.
						A	**ADC0_8 —** ADC0 input 8.
PIO1_1/ADC1_0	-	15	23	[2]	I; PU	IO	**PIO1_1 —** General purpose port 1 input/output 1.
						A	**ADC1_0 —** ADC1 input 0.
PIO1_2/ADC1_4	-	25	36	[2]	I; PU	IO	**PIO1_2 —** General purpose port 1 input/output 2.
						A	**ADC1_4 —** ADC1 input 4.
PIO1_3/ADC1_5	-	28	41	[2]	I; PU	IO	**PIO1_3 —** General purpose port 1 input/output 3.
						A	**ADC1_5 —** ADC1 input 5.
PIO1_4/ADC1_10	-	33	51	[2]	I; PU	IO	**PIO1_4 —** General purpose port 1 input/output 4.
						A	**ADC1_10 —** ADC1 input 10.
PIO1_5/ADC1_11	-	34	52	[2]	I; PU	IO	**PIO1_5 —** General purpose port 1 input/output 5.
						A	**ADC1_11 —** ADC1 input 11.
PIO1_6/ACMP_I2	-	46	73	[2]	I; PU	IO	**PIO1_6 —** General purpose port 1 input/output 6.
						A	**ACMP_I2 —** Analog comparator common input 2.
PIO1_7/ACMP3_I4	-	51	81	[2]	I; PU	IO	**PIO1_7 —** General purpose port 1 input/output 7.
						A	**ACMP3_I4 —** Analog comparator 3 input 4.
PIO1_8/ACMP3_I3/ SCT3_OUT4	-	53	84	[2]	I; PU	IO	**PIO1_8 —** General purpose port 1 input/output 8.
						A	**ACMP3_I3 —** Analog comparator 3 input 3.
						O	**SCT3_OUT4 —** SCTimer3/PWM output 4.
PIO1_9/ACMP2_I4	-	54	85	[2]	I; PU	IO	**PIO1_9 —** General purpose port 1 input/output 9. On the LQFP64 package, this is the ISP_0 boot pin.
						A	**ACMP2_I4 —** Analog comparator 2 input 4.
PIO1_10/ACMP1_I4	-	59	91	[2]	I; PU	IO	**PIO1_10 —** General purpose port 1 input/output 10.
						A	**ACMP1_I4 —** Analog comparator 1 input 4.
PIO1_11	-	38	58	[5]	I; PU	IO	**PIO1_11 —** General purpose port 1 input/output 11. On the LQFP64 package, this is the ISP_1 boot pin.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO1_12	-	-	9	[5]	I; PU	IO	**PIO1_12 —** General purpose port 1 input/output 12.
PIO1_13	-	-	11	[5]	I; PU	IO	**PIO1_13 —** General purpose port 1 input/output 13.
PIO1_14/SCT0_OUT7	-	-	12	[5]	I; PU	IO	**PIO1_14 —** General purpose port 1 input/output 14.
						O	**SCT0_OUT7 —** SCTimer0/PWM output 7.
PIO1_15	-	-	15	[5]	I; PU	IO	**PIO1_15 —** General purpose port 1 input/output 15.
PIO1_16	-	-	18	[5]	I; PU	IO	**PIO1_16 —** General purpose port 1 input/output 16.
PIO1_17/SCT1_OUT7	-	-	20	[5]	I; PU	IO	**PIO1_17 —** General purpose port 1 input/output 17.
						O	**SCT1_OUT7 —** SCTimer1/PWM output 7.
PIO1_18	-	-	25	[5]	I; PU	IO	**PIO1_18 —** General purpose port 1 input/output 18.
PIO1_19	-	-	29	[5]	I; PU	IO	**PIO1_19 —** General purpose port 1 input/output 19.
PIO1_20/SCT2_OUT5	-	-	34	[5]	I; PU	IO	**PIO1_20 —** General purpose port 1 input/output 20.
						O	**SCT2_OUT5 —** SCTimer2/PWM output 5.
PIO1_21	-	-	37	[5]	I; PU	IO	**PIO1_21 —** General purpose port 1 input/output 21.
PIO1_22	-	-	38	[5]	I; PU	IO	**PIO1_22 —** General purpose port 1 input/output 22.
PIO1_23	-	-	42	[5]	I; PU	IO	**PIO1_23 —** General purpose port 1 input/output 23.
PIO1_24/SCT3_OUT5	-	-	44	[5]	I; PU	IO	**PIO1_24 —** General purpose port 1 input/output 24.
						O	**SCT3_OUT5 —** SCTimer3/PWM output 5.
PIO1_25	-	-	46	[5]	I; PU	IO	**PIO1_25 —** General purpose port 1 input/output 25.
PIO1_26	-	-	48	[5]	I; PU	IO	**PIO1_26 —** General purpose port 1 input/output 26.
PIO1_27	-	-	50	[5]	I; PU	IO	**PIO1_27 —** General purpose port 1 input/output 27.
PIO1_28	-	-	55	[5]	I; PU	IO	**PIO1_28 —** General purpose port 1 input/output 28.
PIO1_29	-	-	56	[5]	I; PU	IO	**PIO1_29 —** General purpose port 1 input/output 29.
PIO1_30	-	-	59	[5]	I; PU	IO	**PIO1_30 —** General purpose port 1 input/output 30.
PIO1_31	-	-	60	[5]	I; PU	IO	**PIO1_31 —** General purpose port 1 input/output 31.
PIO2_0	-	-	62	[5]	I; PU	IO	**PIO2_0 —** General purpose port 2 input/output 0.
PIO2_1	-	-	64	[5]	I; PU	IO	**PIO2_1 —** General purpose port 2 input/output 1.
PIO2_2	-	-	72	[5]	I; PU	IO	**PIO2_2 —** General purpose port 2 input/output 2.
PIO2_3	-	-	76	[5]	I; PU	IO	**PIO2_3 —** General purpose port 2 input/output 3.
PIO2_4	-	-	77	[5]	I; PU	IO	**PIO2_4 —** General purpose port 2 input/output 4. On the LQFP100 package, this is the ISP_1 boot pin.
PIO2_5	-	-	80	[5]	I; PU	IO	**PIO2_5 —** General purpose port 2 input/output 5. On the LQFP100 package, this is the ISP_0 boot pin.
PIO2_6	-	-	82	[5]	I; PU	IO	**PIO2_6 —** General purpose port 2 input/output 6. On the LQFP100 package, this pin is assigned to U0_TXD in ISP USART mode.
PIO2_7	-	-	86	[5]	I; PU	IO	**PIO2_7 —** General purpose port 2 input/output 7. On the LQFP100 package, this pin is assigned to U0_RXD in ISP USART mode.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
VREFP_ADC	10	13	21		-		ADC positive reference voltage. The voltage level on VREFP_ADC must be equal to or lower than the voltage applied to V_{DDA}. If the ADC is not used, tie VREFP_ADC to V_{DD}.
V_{SSA}	17	21	31		-		Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	41, 20, 40	56, 26, 27, 55	88, 7, 39, 40, 68, 87		-		Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[3] This pin is not 5 V tolerant due to special analog functionality. When configured for a digital function, this pin is 3 V tolerant and provides standard digital I/O functions with configurable internal pull-up and pull-down resistors and hysteresis. When configured for DAC_OUT, the digital section of the pin is disabled and this pin is a 3 V tolerant analog output. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, and configurable hysteresis. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on. This pin is powered in deep power-down mode and can wake up the part. The wake-up pin function can be disabled and the pin can be used for other purposes, if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[9] Special analog pin.

[10] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[11] When the main oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. Movable functions

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.

Table 4. Movable functions *…continued*

Function name	Type	Description
DAC_PINTRIG	I	DAC external pin trigger input.
DAC_SHUTOFF	I	DAC shut-off external input.
ACMP0_O	O	Analog comparator 0 output.
ACMP1_O	O	Analog comparator 1 output.
ACMP2_O	O	Analog comparator 2 output.
ACMP3_O	O	Analog comparator 3 output.
CLKOUT	O	Clock output.
ROSC	O	Analog comparator ring oscillator output.
ROSC_RESET	I	Analog comparator ring oscillator reset.
USB_FTOGGLE	O	USB frame toggle. Do not assign this function to a pin until a USB device is connected and the first SOF interrupt has been received by the device.
QEI_PHA	I	QEI phase A input.
QEI_PHB	I	QEI phase B input.
QEI_IDX	I	QEI index input.
GPIO_INT_BMAT	O	Output of the pattern match engine.
SWO	O	Serial wire output.

Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO0_2/ADC0_6/SCT1_OUT3	3	6	8	SCT0 input multiplexer
PIO0_3/ADC0_5/SCT1_OUT4	4	7	10	SCT0 input multiplexer
PIO0_4/ADC0_4	5	8	13	SCT2 input multiplexer
PIO0_5/ADC0_3	6	9	14	FREQMEAS
PIO0_7/ADC0_1	8	11	17	SCT3 input multiplexer
PIO0_14/ADC1_7/SCT1_OUT5	22	30	45	SCTIPU input SAMPLE_IN_A0
PIO0_15/ADC1_8	23	31	47	SCT1 input multiplexer
PIO0_16/ADC1_9	24	32	49	SCT1 input multiplexer
PIO0_17/WAKEUP/$\overline{\text{TRST}}$	28	39	61	SCT0 input multiplexer
SWCLK/PIO0_19/TCK	29	40	63	FREQMEAS
$\overline{\text{RESET}}$/PIO0_21	34	45	71	SCT1 input multiplexer
PIO0_25/ACMP0_I4	44	60	93	SCTIPU input SAMPLE_IN_A1
PIO0_27/ACMP_I1	46	62	97	SCT2 input multiplexer
PIO0_30/ADC0_11	-	1	1	FREQMEAS
				SCT0 input multiplexer
PIO0_31/ADC0_9	-	3	3	SCT1 input multiplexer
PIO1_4/ADC1_10	-	33	51	SCT1 input multiplexer
PIO1_5/ADC1_11	-	34	52	SCT1 input multiplexer
PIO1_6/ACMP_I2	-	46	73	SCT0 input multiplexer

8.21 C_CAN

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller can build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

The C_CAN functions are movable functions and are assigned to pins through the switch matrix. Do not connect C_CAN functions to the open-drain pins PIO0_22 and PIO0_23.

8.21.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

8.22 PWM/timer/motor control subsystem

The SCTimer/PWMs (State Configurable Timer/Pulse Width Modulators) and the analog peripherals support multiple ways of interconnecting their inputs and outputs and of interfacing to the pins and the DMA controller. Using the highly flexible and programmable connection scheme makes it easy to configure various subsystems for motor control and complex timing and tracking applications. Specifically, the inputs to the SCTs and the trigger inputs of the ADCs and DMA are selected through the input multiplexer which offers a choice of many possible sources for each input or trigger. SCT outputs are assigned to pins through the switch matrix allowing for many pinout solutions.

8.22.1 SCtimer/PWM subsystem

The SCTimer/PWMs can be configured to build a PWM controller with multiple outputs by programming the MATCH and MATCHRELOAD registers to control the base frequency and the duty cycle of each SCTimer/PWM output. More complex waveforms that span multiple counter cycles or change behavior across or within counter cycles can be generated using the state capability built into the SCTimer/PWMs.

Combining the PWM functions with the analog functions, the PWM output can react to control signals like comparator outputs or the ADC interrupts. The SCT IPU adds emergency shut-down functions and pre-processing of controlling events. For an overview of the PWM subsystem, see Figure 12 “PWM-Analog subsystem”.

For high-speed PWM functionality, use only outputs that are fixed-pin functions to minimize pin-to-pin differences in output skew. See also Table 22 “SCTimer/PWM output dynamic characteristics”. This reduces the number of PWM outputs to five for each large SCT.

- Four registers to indicate which specific input sources caused the abort input to the SCTs.
- Four additional outputs which can be sampled at certain times and latched at others before being routed to SCT inputs.
- Nine abort inputs. Any combination of the abort inputs can trigger the dedicated abort input of each SCT.

8.23 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.23.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clock and direction).

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are internal connections to other on-chip peripherals such as the SCT and analog comparator outputs, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions.

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCT inputs for tight timing control between the ADC and the SCTs.

- When the ADC is accurately calibrated, the internal voltage reference can be used to measure the power supply voltage. This requires calibration by recording the ADC code of the internal voltage reference at different power supply levels yielding a different ADC code value for each supply voltage level. In a particular application, the internal voltage reference can be measured and the actual power supply voltage can be determined from the stored calibration values. The calibration values can be stored in the EEPROM for easy access.

After power-up, the internal voltage reference must be allowed to settle to its stable value before it can be used as an ADC reference voltage input.

For an accurate measurement of the internal voltage reference by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.29 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.29.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

8.30 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.30.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WWDT is clocked by the dedicated watchdog oscillator (WDOsc) running at a fixed frequency.

8.34 Clock generation

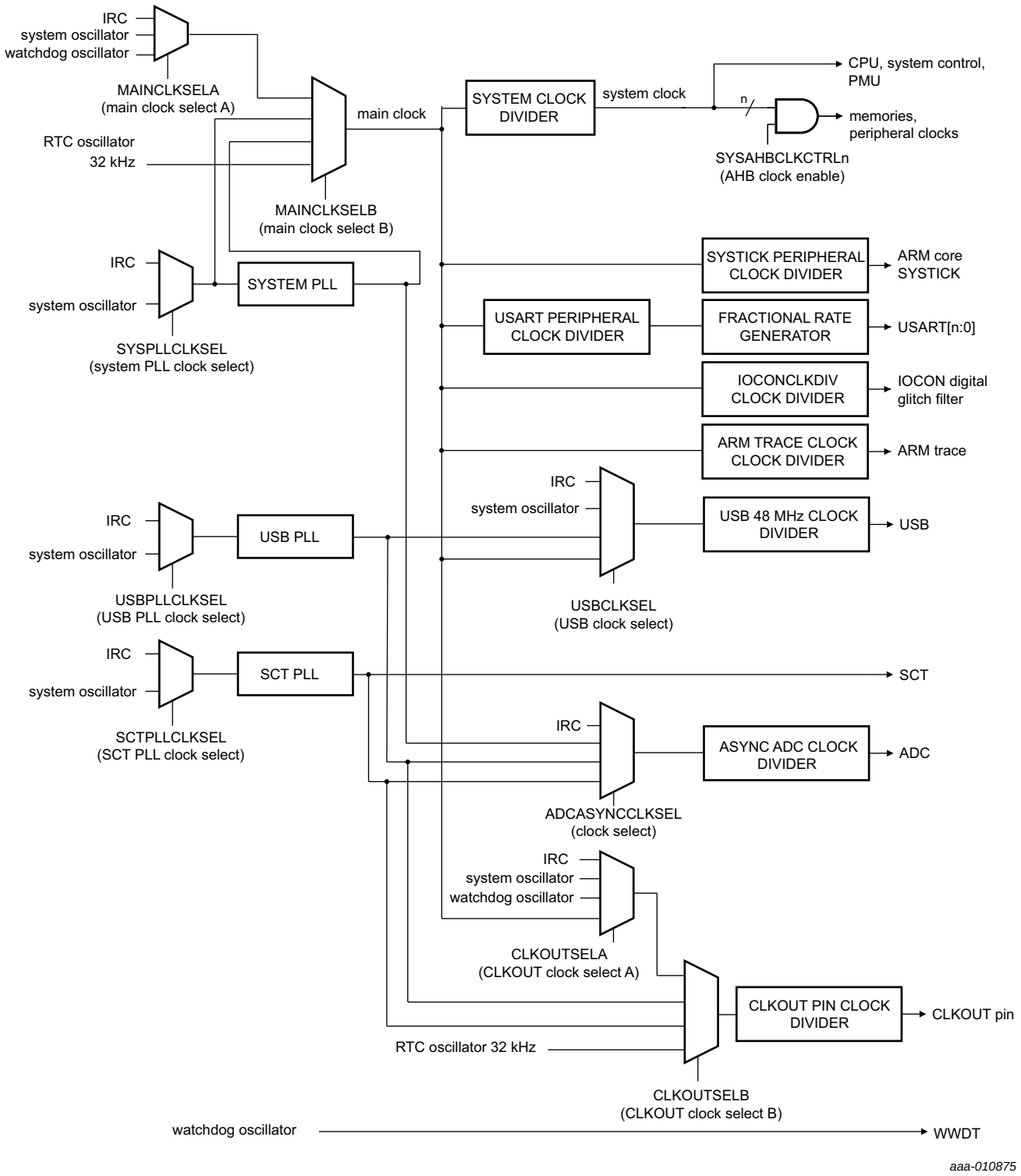


Fig 14. Clock generation

8.38 Clock output

The LPC15xx feature a clock output function that routes the internal oscillator outputs, the PLL outputs, or the main clock an output pin where they can be observed directly.

8.39 Wake-up process

The LPC15xx begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the system oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and system oscillator as a clock source.

8.40 Power control

The LPC15xx support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides additional power control.

8.40.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC15xx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock and to easily set the configuration options for Deep-sleep and power-down modes.

Remark: When using the USB, configure the LPC15xx in Default mode.

8.40.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

In addition, ISP entry the external pins can be disabled without enabling CRP. For details, see the LPC15xx *user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using ISP pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP pins for valid user code can be disabled. For details, see the LPC15xx *user manual*.

Table 9. Limiting values *...continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C	-	100	mA
T_{stg}	storage temperature	[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins [11]	-	5	kV

[1] The following applies to the limiting values:
  a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
  b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 11) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_22 and PIO0_23 and except the 3 V tolerant pin PIO0_12.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

[6] Applies to 3 V tolerant pin PIO0_12.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

11. Static characteristics

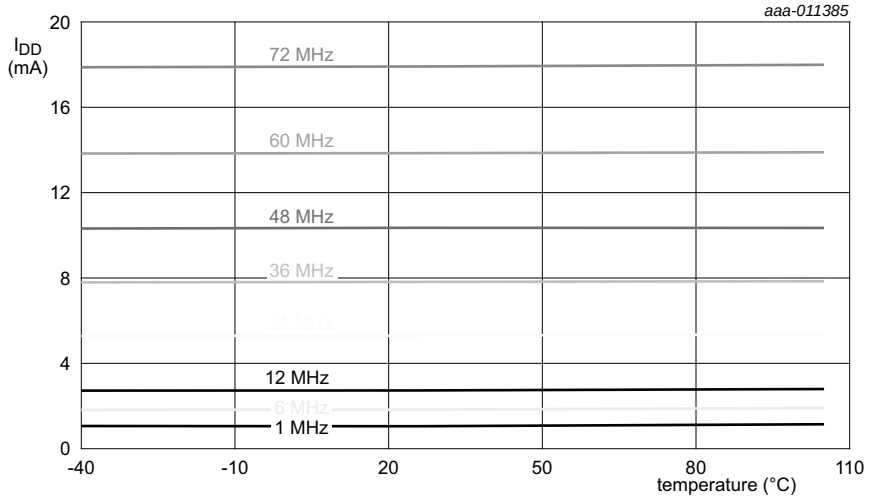
Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)	[2]	2.4	3.3	V_{DDA}	V
V_{DDA}	analog supply voltage		2.4	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP_DAC_VDDCMP	2.4	-	V_{DDA}	V
		on pin VREFP_ADC	-	-	V_{DDA}	V
V_{BAT}	battery supply voltage		2.4	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	4.3	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.7	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	19.3	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	18	-	mA
		Sleep mode;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.1	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	1.5	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	8.0	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	7.3	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; [3][4][11]	-			
		T_{amb} = 25 °C		310	380	µA
		T_{amb} = 105 °C	-	-	620	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V [3][4][11]	-			
		T_{amb} = 25 °C		3.8	15	µA
		T_{amb} = 105 °C	-	-	163	µA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
High-drive output pin configured as digital pin (PIO0_24); see Figure 17						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10[14]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10[14]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10[14]	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V [16] [18]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage	2.4 V <= V_{DD} < 3.0 V	0.30	-	-	V
		3.0 V <= V_{DD} <= 3.6 V	0.35	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.7 V <= V_{DD} < 3.6 V	$V_{DD} - 0.4$	-	-	V
		I_{OH} = 12 mA; 2.4 V <= V_{DD} < 2.7 V	$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.7 V <= V_{DD} < 3.6 V	20	-	-	mA
		$V_{OH} = V_{DD} - 0.4$ V; 2.4 V <= V_{DD} < 2.7 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [19]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [20]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V [20]	−10	−50	−85	µA
		$V_{DD} < V_I < 5$ V	0	0	0	µA
I^2C-bus pins (PIO0_22 and PIO0_23); see Figure 17						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins	3.5	-	-	mA



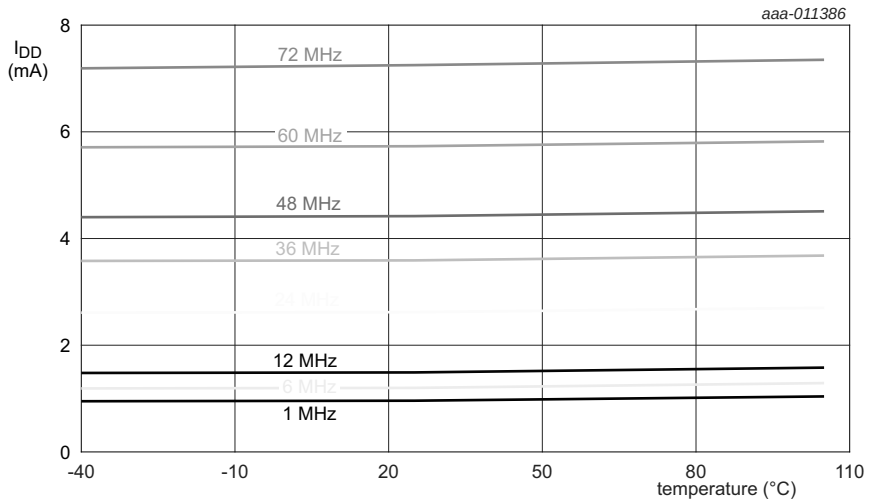
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 19. Active mode: Typical supply current I_{DD} versus temperature



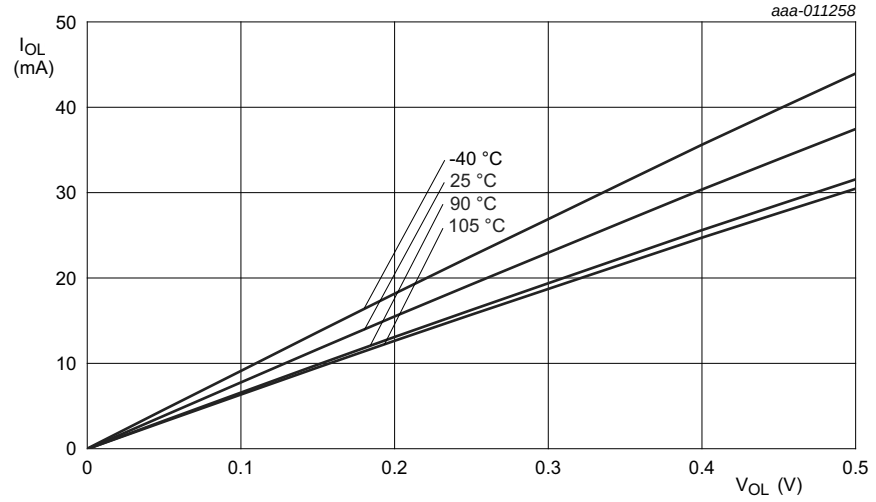
Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

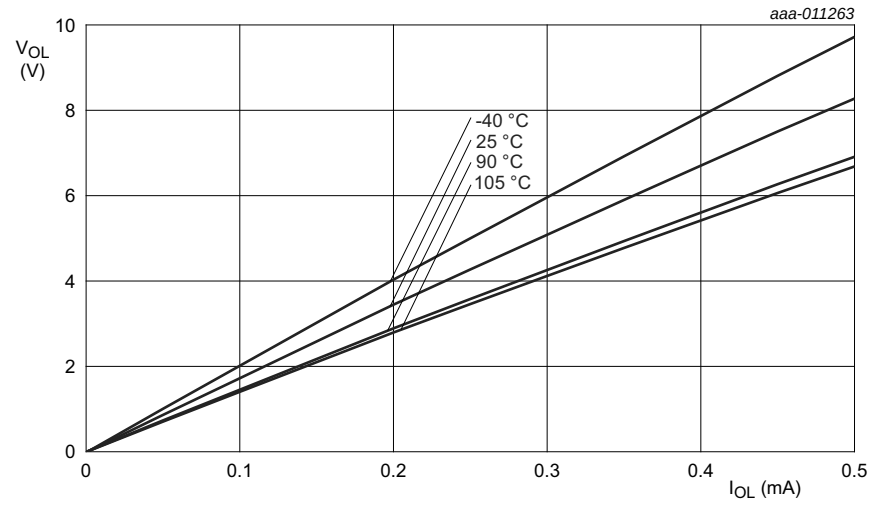
24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 20. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



Conditions: V_{DD} = 3.3 V; on pins PIO0_22 and PIO0_23.

Fig 28. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_24.

Fig 29. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

Table 24. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DDA}; V_{SSA} = 0; VREFN = V_{SSA}.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IA}	analog input voltage	[1]	0	V_{DDA}	V
C_{ia}	analog input capacitance		-	0.32	pF
$f_{clk(ADC)}$	ADC clock frequency	$V_{DDA} \geq 2.7$ V		50	MHz
		$V_{DDA} \geq 2.4$ V		25	MHz
f_s	sampling frequency	$V_{DDA} \geq 2.7$ V	-	2	Msamples/s
		$V_{DDA} \geq 2.4$ V	-	1	Msamples/s
E_D	differential linearity error	[2]	-	+/- 2	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	+/- 2	LSB
E_O	offset error	[4]	-	+/- 3	LSB
$V_{err(fs)}$	full-scale error voltage	2 Msamples/s [5]	-	+/- 0.12	%
		1 Msamples/s		+/- 0.07	%
Z_i	input impedance	f_s = 2 Msamples/s [6][7]	0.1	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 40.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 40.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 40.

[5] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 40.

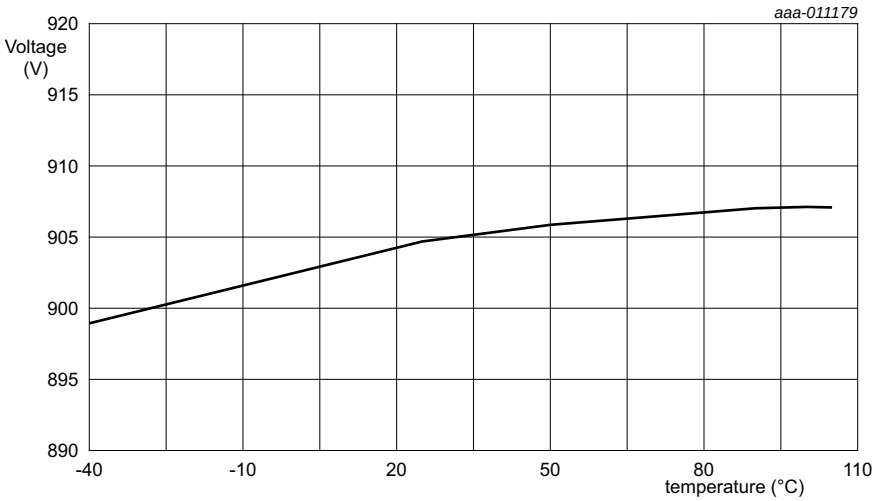
[6] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0. 32 pF.

[7] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 11 for C_{io}.

Table 26. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = −40 °C to +105 °C [1]	875	-	925	mV
		T_{amb} = 25 °C		905		mV
$t_{s(pu)}$	power-up settling time	to 99% of V_O	-	-	125	µs

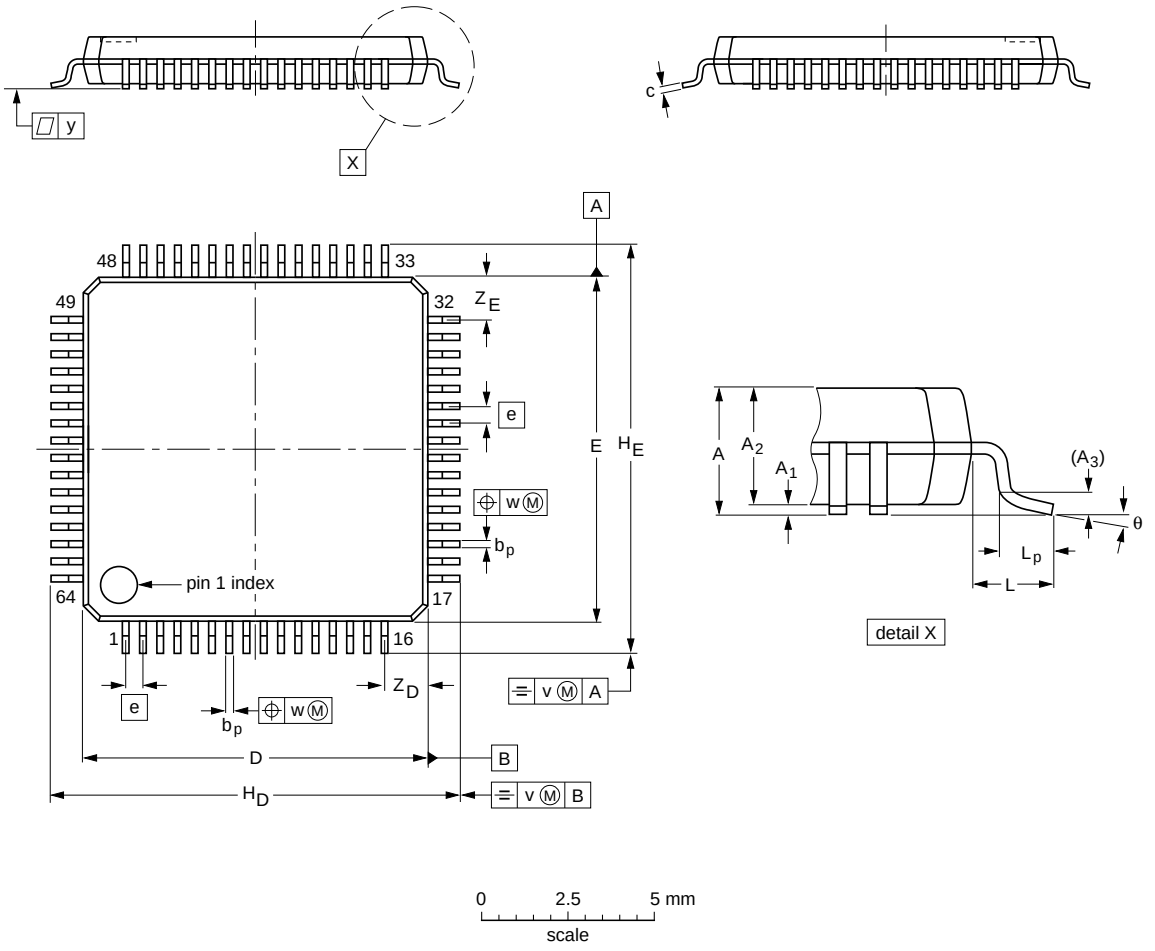
[1] Maximum and minimum values are measured on samples from the corners of the process matrix lot.



V_{DDA} = 3.3 V; averaged over process corners

Fig 42. Average internal voltage reference output voltage

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 51. Package outline LQFP64 (SOT314-2)

18. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC15XX v.1.1	20150429	Product data sheet	-	LPC15XX v.1
Modifications:	• Pin description table updated for clarification (I2C-bus pins, VBAT, WAKEUP, RTCXIN/OUT). • Table note 11 added in Table 3. • Section 14.1 “ADC usage notes” added. • Section 14.6 “Connecting power, clocks, and debug functions” added. • Section 14.7 “Termination of unused pins” added. • Section 14.8 “Pin states in different power modes” added. • Section 14.9 “ElectroMagnetic Compatibility (EMC)” added. • Table 11 “Static characteristics”: Changed the power-down max specification value: I_{DD} Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C from 8 μA to 15 μA.			
LPC15XX v.1	<tbd>	Product data sheet	-	-