Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1547jbd64ql

- Single power supply 2.4 V to 3.6 V.
- Temperature range −40 °C to +105 °C.
- Available as LQFP100, LQFP64, and LQFP48 packages.

3. Applications

- Motor control
- Motion drives
- Digital power supplies
- Industrial and medical
- Solar inverters
- Home appliances
- Building and factory automation

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1549JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1549JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1549JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1548JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1548JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1519JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1519JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1518JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1518JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO1_7/ACMP3_I4	-	51	81	SCT0 input multiplexer
PIO1_11	-	38	58	SCT3 input multiplexer
				SCTIPU input SAMPLE_IN_A2
PIO1_12	-	-	9	SCT0 input multiplexer
PIO1_13	-	-	11	SCT0 input multiplexer
PIO1_15	-	-	12	SCT1 input multiplexer
PIO1_16	-	-	18	SCT1 input multiplexer
PIO1_18	-	-	25	SCT2 input multiplexer
PIO1_19	-	-	29	SCT2 input multiplexer
PIO1_21	-	-	37	SCT3 input multiplexer
PIO1_22	-	-	38	SCT3 input multiplexer
PIO1_26	-	-	48	SCTIPU input SAMPLE_IN_A3
PIO1_27	-	-	50	FREQMEAS

8. Functional description

8.1 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

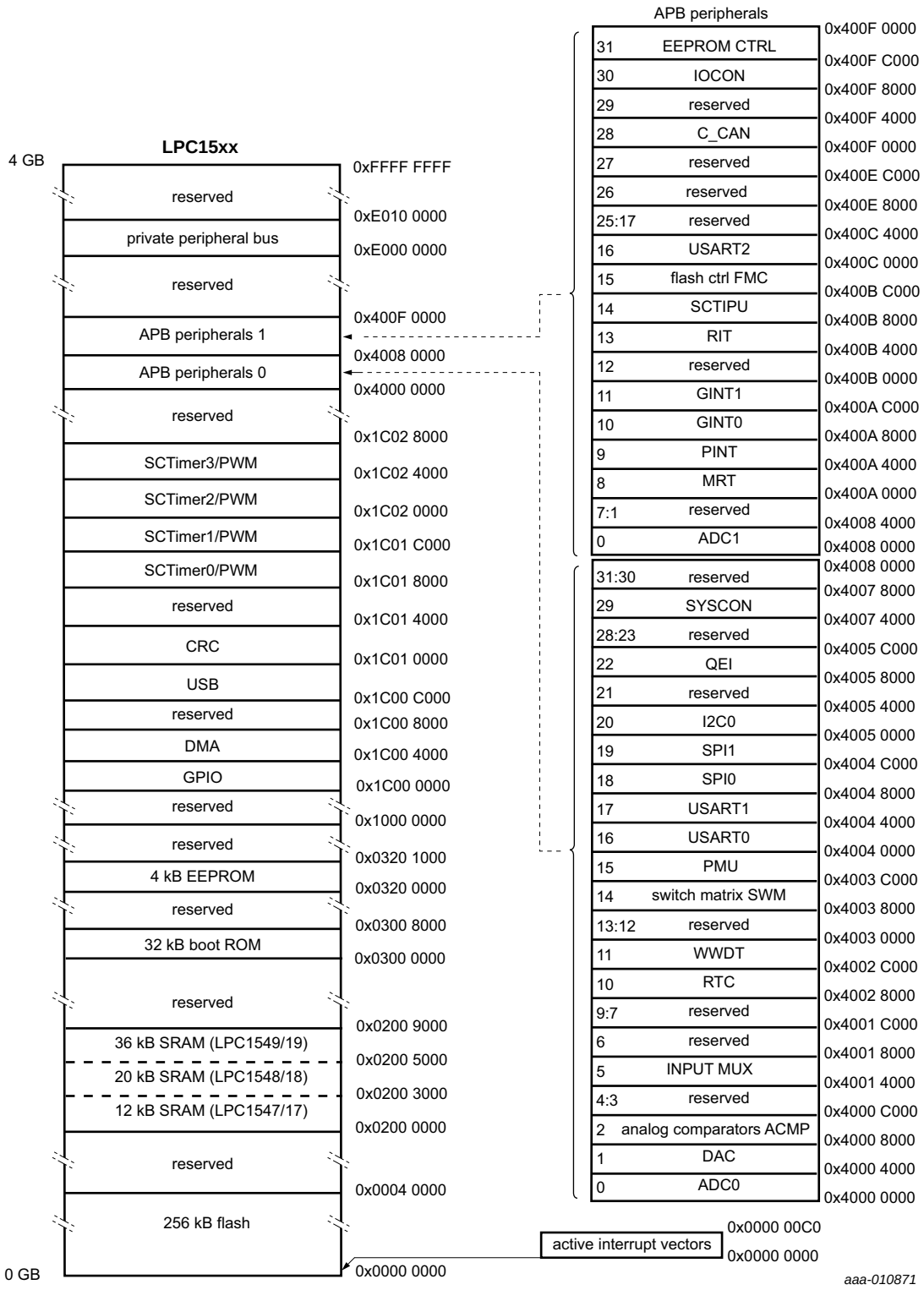
The ARM Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual*, which is available on the official ARM website.

8.2 Memory Protection Unit (MPU)

The LPC15xx have a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

8.8 Memory map



See Section 8.5 “SRAM” for SRAM configuration.

Fig 10. Memory map

8.21 C_CAN

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller can build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

The C_CAN functions are movable functions and are assigned to pins through the switch matrix. Do not connect C_CAN functions to the open-drain pins PIO0_22 and PIO0_23.

8.21.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

8.22 PWM/timer/motor control subsystem

The SCTimer/PWMs (State Configurable Timer/Pulse Width Modulators) and the analog peripherals support multiple ways of interconnecting their inputs and outputs and of interfacing to the pins and the DMA controller. Using the highly flexible and programmable connection scheme makes it easy to configure various subsystems for motor control and complex timing and tracking applications. Specifically, the inputs to the SCTs and the trigger inputs of the ADCs and DMA are selected through the input multiplexer which offers a choice of many possible sources for each input or trigger. SCT outputs are assigned to pins through the switch matrix allowing for many pinout solutions.

8.22.1 SCtimer/PWM subsystem

The SCTimer/PWMs can be configured to build a PWM controller with multiple outputs by programming the MATCH and MATCHRELOAD registers to control the base frequency and the duty cycle of each SCTimer/PWM output. More complex waveforms that span multiple counter cycles or change behavior across or within counter cycles can be generated using the state capability built into the SCTimer/PWMs.

Combining the PWM functions with the analog functions, the PWM output can react to control signals like comparator outputs or the ADC interrupts. The SCT IPU adds emergency shut-down functions and pre-processing of controlling events. For an overview of the PWM subsystem, see Figure 12 “PWM-Analog subsystem”.

For high-speed PWM functionality, use only outputs that are fixed-pin functions to minimize pin-to-pin differences in output skew. See also Table 22 “SCTimer/PWM output dynamic characteristics”. This reduces the number of PWM outputs to five for each large SCT.

8.34 Clock generation

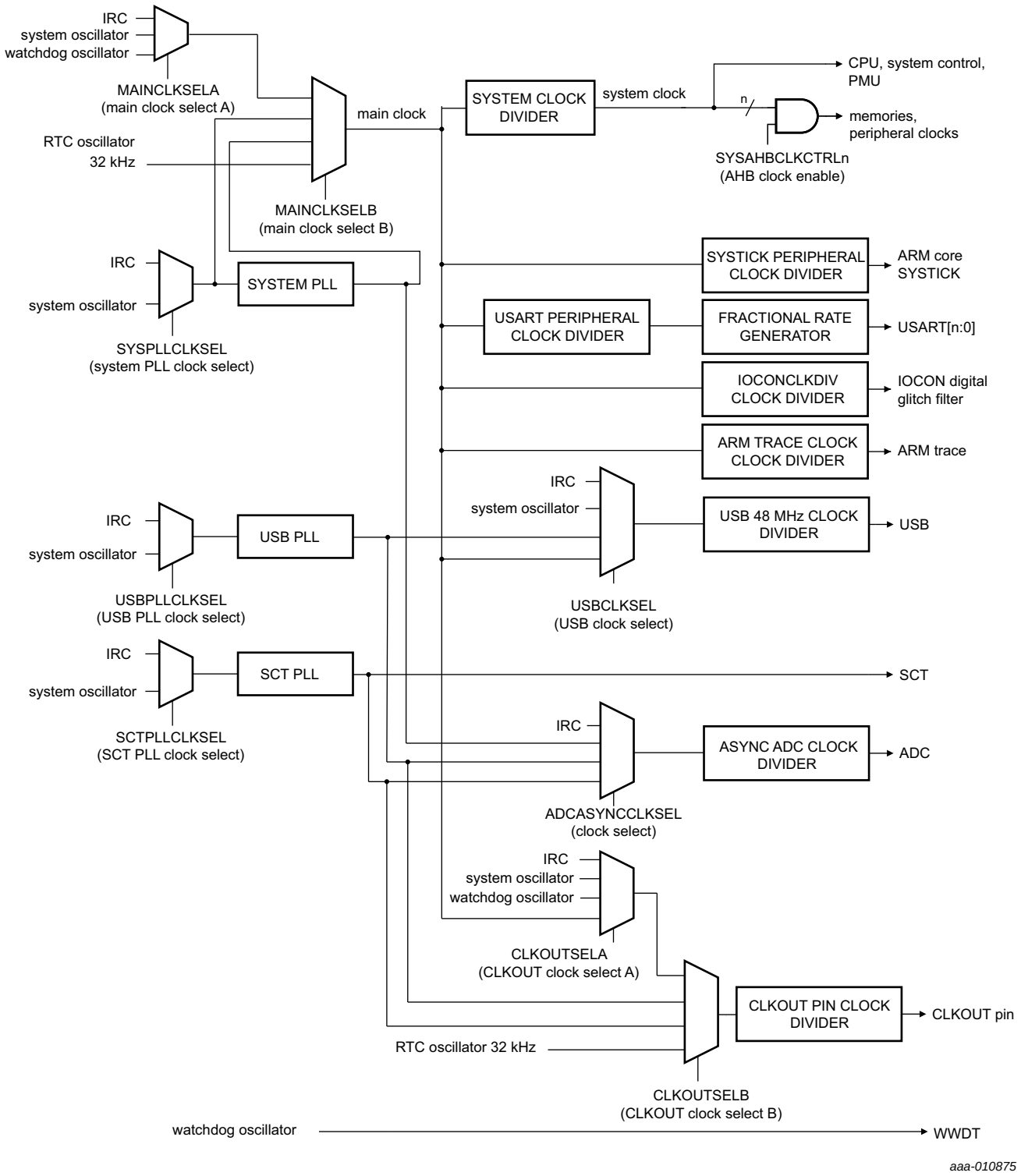


Fig 14. Clock generation

8.38 Clock output

The LPC15xx feature a clock output function that routes the internal oscillator outputs, the PLL outputs, or the main clock an output pin where they can be observed directly.

8.39 Wake-up process

The LPC15xx begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the system oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and system oscillator as a clock source.

8.40 Power control

The LPC15xx support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides additional power control.

8.40.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC15xx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock and to easily set the configuration options for Deep-sleep and power-down modes.

Remark: When using the USB, configure the LPC15xx in Default mode.

8.40.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

In addition, ISP entry the external pins can be disabled without enabling CRP. For details, see the LPC15xx *user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using ISP pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP pins for valid user code can be disabled. For details, see the LPC15xx *user manual*.

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

11. Static characteristics

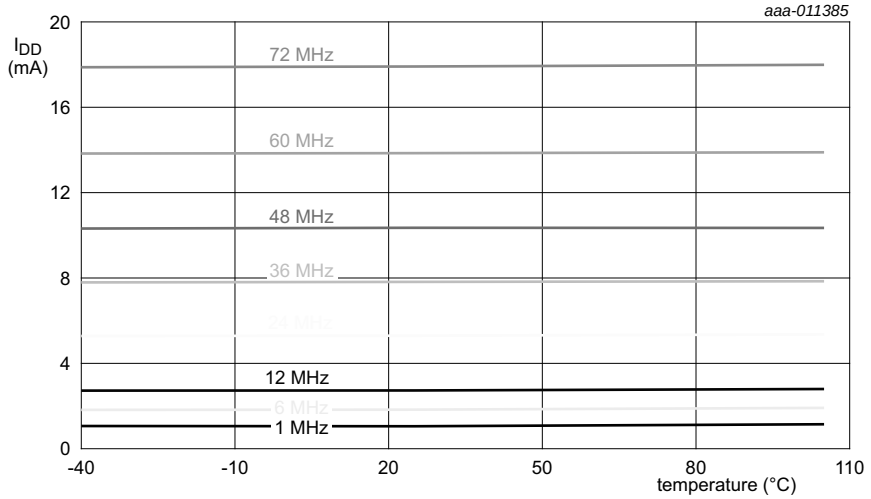
Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)	[2]	2.4	3.3	V_{DDA}	V
V_{DDA}	analog supply voltage		2.4	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP_DAC_VDDCMP	2.4	-	V_{DDA}	V
		on pin VREFP_ADC	-	-	V_{DDA}	V
V_{BAT}	battery supply voltage		2.4	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	4.3	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.7	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	19.3	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	18	-	mA
		Sleep mode;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.1	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	1.5	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	8.0	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	7.3	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; [3][4][11]	-			
		T_{amb} = 25 °C		310	380	µA
		T_{amb} = 105 °C	-	-	620	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V [3][4][11]	-			
		T_{amb} = 25 °C		3.8	15	µA
		T_{amb} = 105 °C	-	-	163	µA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
High-drive output pin configured as digital pin (PIO0_24); see Figure 17						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10[14]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10[14]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10[14]	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V [16] [18]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage	2.4 V <= V_{DD} < 3.0 V	0.30	-	-	V
		3.0 V <= V_{DD} <= 3.6 V	0.35	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.7 V <= V_{DD} < 3.6 V	$V_{DD} - 0.4$	-	-	V
		I_{OH} = 12 mA; 2.4 V <= V_{DD} < 2.7 V	$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.7 V <= V_{DD} < 3.6 V	20	-	-	mA
		$V_{OH} = V_{DD} - 0.4$ V; 2.4 V <= V_{DD} < 2.7 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [19]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [20]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V [20]	−10	−50	−85	µA
		$V_{DD} < V_I < 5$ V	0	0	0	µA
I^2C-bus pins (PIO0_22 and PIO0_23); see Figure 17						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins	3.5	-	-	mA



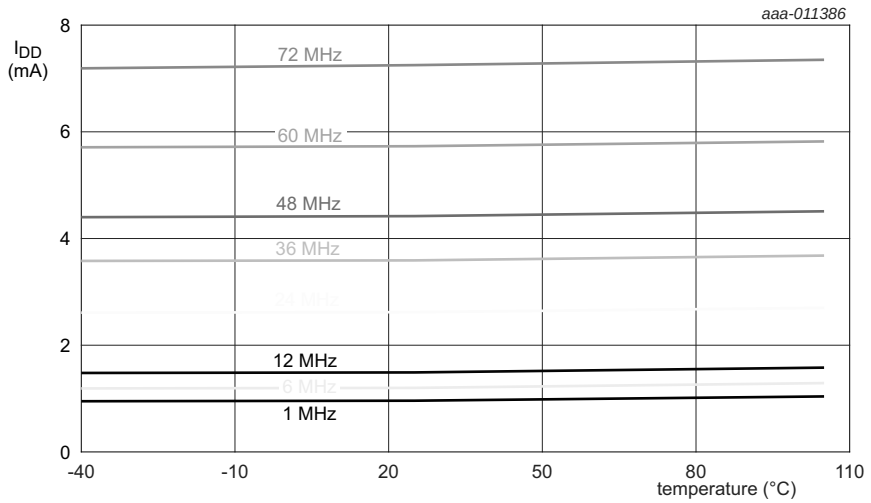
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 19. Active mode: Typical supply current I_{DD} versus temperature



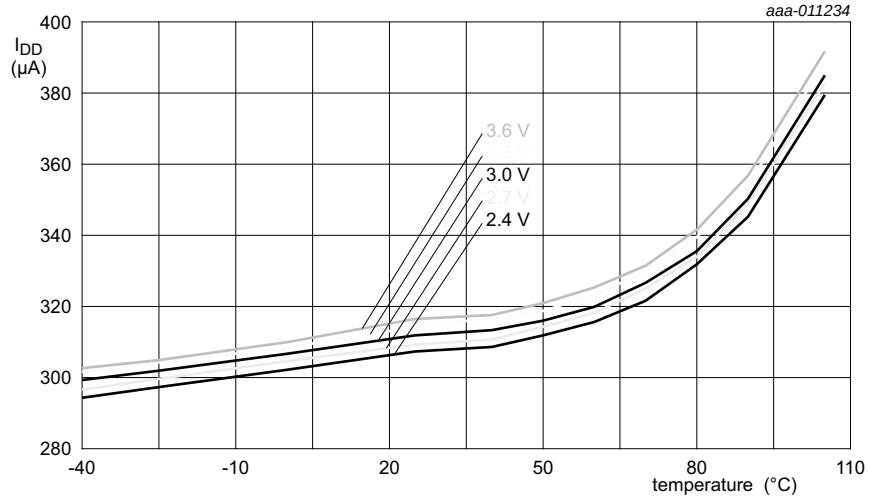
Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

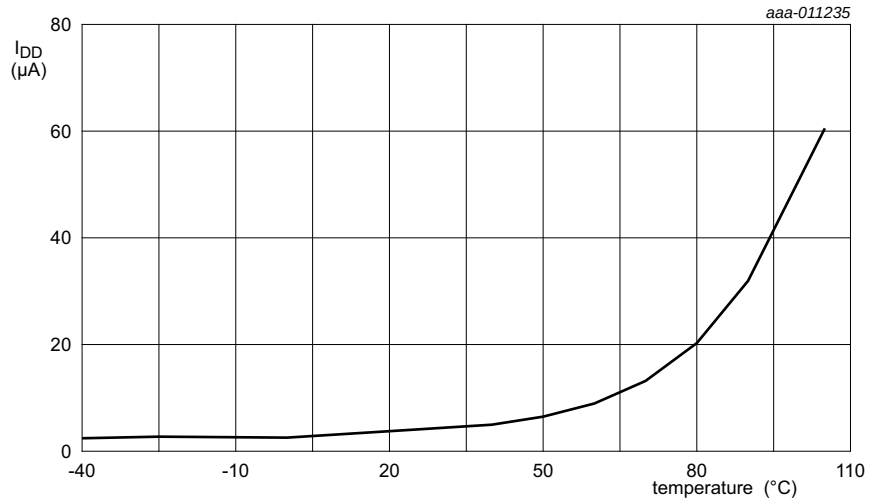
24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 20. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled. Use API power_mode_configure() with mode parameter set to DEEP_SLEEP and peripheral parameter set to 0xFF.

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



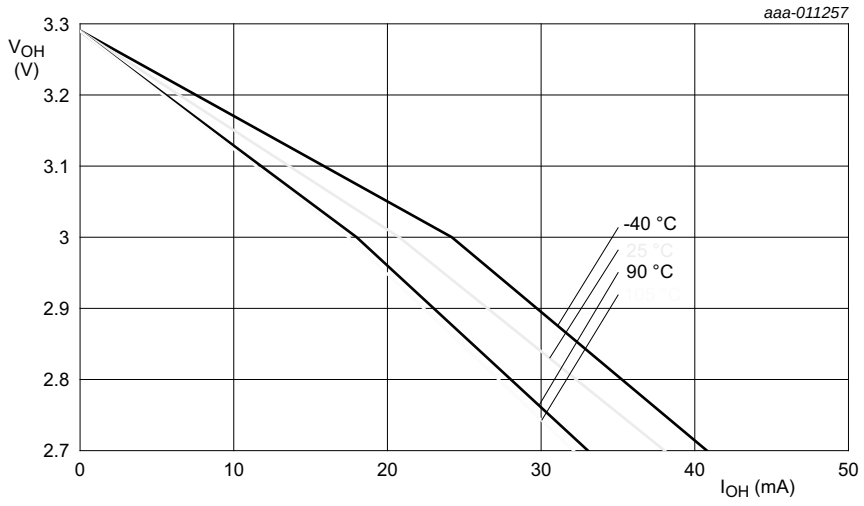
Conditions: BOD disabled; all oscillators and analog blocks disabled; V_{DD} = 2.4 V to 3.6 V. Use API power_mode_configure() with mode parameter set to POWER_DOWN and peripheral parameter set to 0xFF.

Fig 22. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 12. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	72 MHz	
USART0	-	0.02	0.15	-
USART1	-	0.02	0.16	-
USART2	-	0.02	0.15	-
C_CAN	-	0.50	3.00	
USB	-	0.10	0.50	
Comparator ACMP0/1/2/3	-	0.01	0.03	-
ADC0	-	0.05	0.33	-
ADC1	-	0.04	0.33	-
temperature sensor	-	0.03	0.03	
internal voltage reference/band gap	-	0.03	0.04	
DAC	-	0.02	0.09	-
DMA	-	0.36	1.5	
CRC	-	0.01	0.08	-

11.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_24.

Fig 27. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

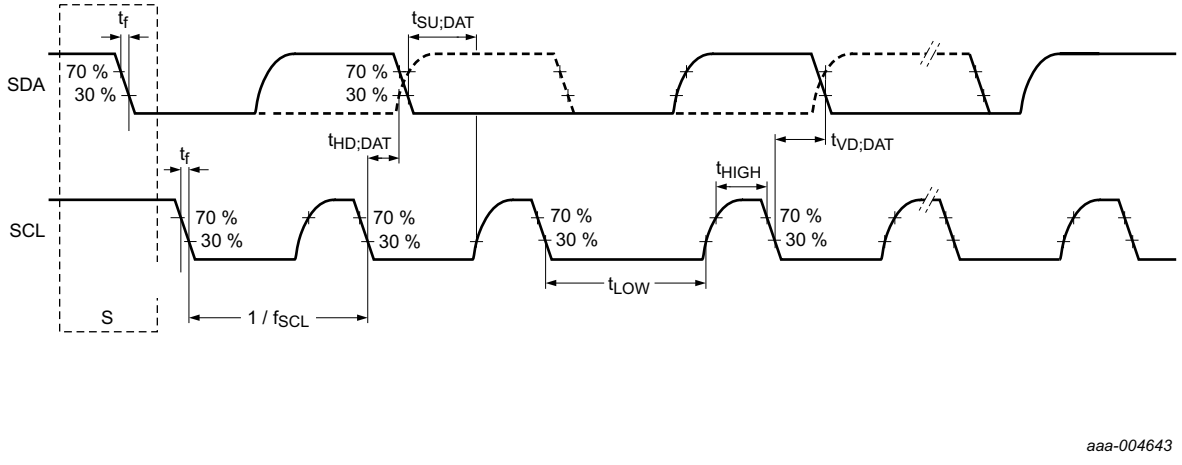
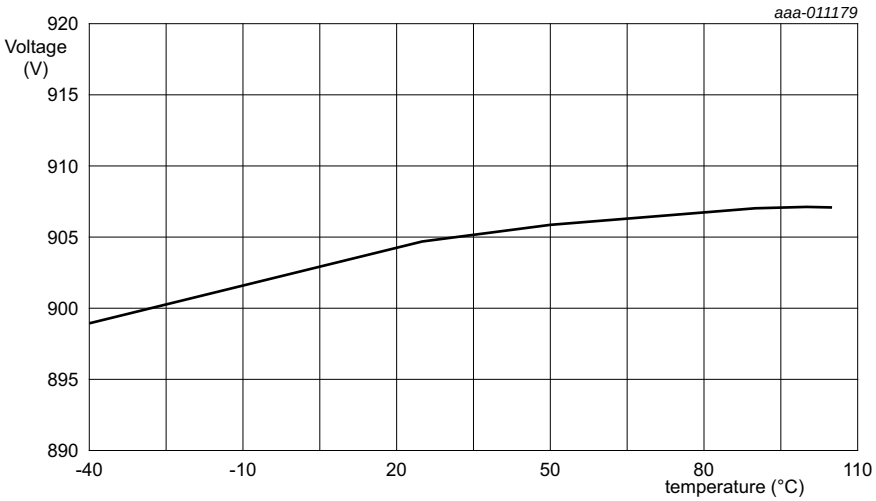


Fig 35. I²C-bus pins clock timing

Table 26. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = −40 °C to +105 °C [1]	875	-	925	mV
		T_{amb} = 25 °C		905		mV
$t_{s(pu)}$	power-up settling time	to 99% of V_O	-	-	125	µs

[1] Maximum and minimum values are measured on samples from the corners of the process matrix lot.



V_{DDA} = 3.3 V; averaged over process corners

Fig 42. Average internal voltage reference output voltage

Table 29. Comparator characteristics

V_{DDA} = 3.0 V. DLY = 0x0 in the analog comparator CTRL register for shortest propagation delay setting. See the LPC15xx user manual UM10736.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{DD}	supply current	VP > VM	-	48	-	μA
		VM > VP	-	38	-	μA
V_{IC}	common-mode input voltage		0	-	V_{DDA}	V
DV_O	output voltage variation		0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V	-	+/- 3	-	mV
		V_{IC} = 1.5 V	-	+/- 3	-	mV
		V_{IC} = 2.9 V	-	+/- 6	-	mV
Dynamic characteristics						
$t_{startup}$	start-up time	nominal process	-	4.5	6	μs
t_{PD}	propagation delay	HIGH to LOW; V_{DDA} = 3.0 V;				
		V_{IC} = 0.1 V; 50 mV overdrive input [1]	-	86	130	ns
		V_{IC} = 0.1 V; rail-to-rail input [1]	-	196	250	ns
		V_{IC} = 1.5 V; 50 mV overdrive input [1]	-	68	110	ns
		V_{IC} = 1.5 V; rail-to-rail input [1]	-	64	90	ns
		V_{IC} = 2.9 V; 50 mV overdrive input [1]	-	86	130	ns
		V_{IC} = 2.9 V; rail-to-rail input [1]	-	48	80	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DDA} = 3.0 V;				
		V_{IC} = 0.1 V; 50 mV overdrive input [1]	-	98	130	ns
		V_{IC} = 0.1 V; rail-to-rail input [1]	-	24	40	ns
		V_{IC} = 1.5 V; 50 mV overdrive input [1]	-	88	130	ns
		V_{IC} = 1.5 V; rail-to-rail input [1]	-	68	120	ns
		V_{IC} = 2.9 V; 50 mV overdrive input [1]	-	84	110	ns
		V_{IC} = 2.9 V; rail-to-rail input [1]	-	98	180	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V; settings: [2]				
		5 mV	3	-	8	mV
		10 mV	8	-	13	mV
		15 mV	17	-	25	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V; settings: [1][2]				
		5 mV	3	-	9	mV
		10 mV	8	-	18	mV
		15 mV	18	-	27	mV
R_{lad}	ladder resistance	-	-	1	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +105 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

14.5 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 48. If the RTC is not used, the RTCXIN pin can be grounded.

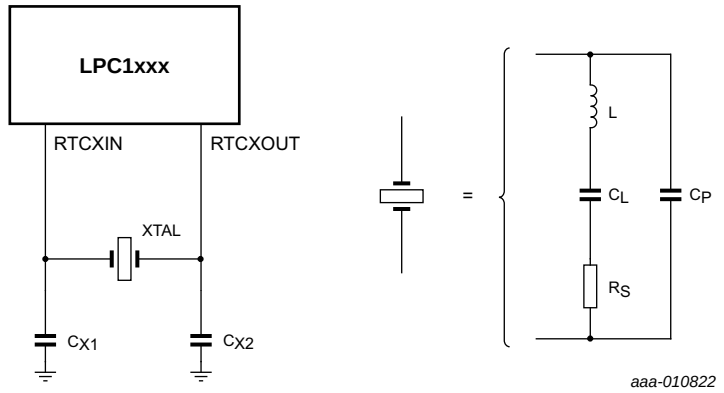


Fig 48. RTC oscillator components

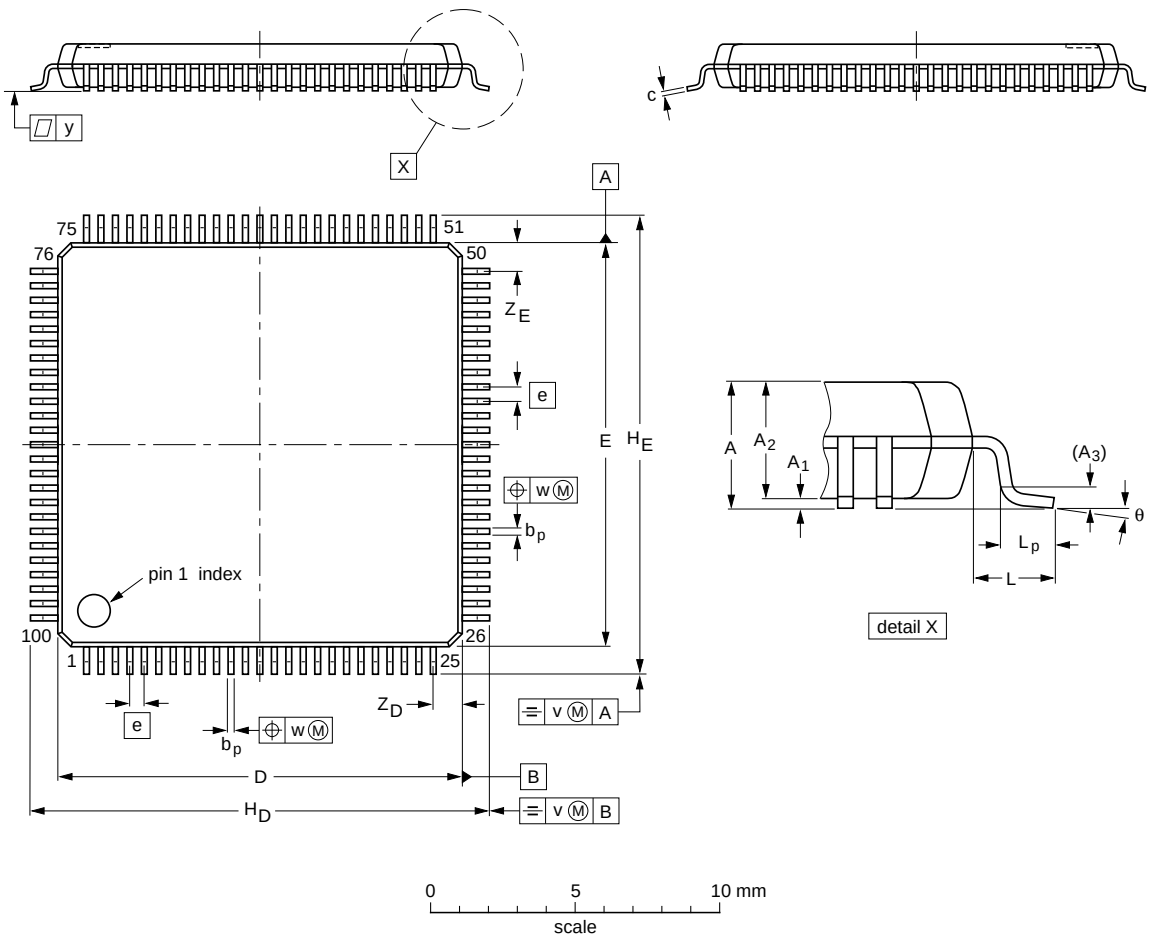
Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry.The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If the external crystal's load capacitance is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$C_{x1} = C_{x2} = 2 \times C_L - C_P$

14.6 Connecting power, clocks, and debug functions

Figure 49 shows the basic board connections used to power the LPC15xx, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

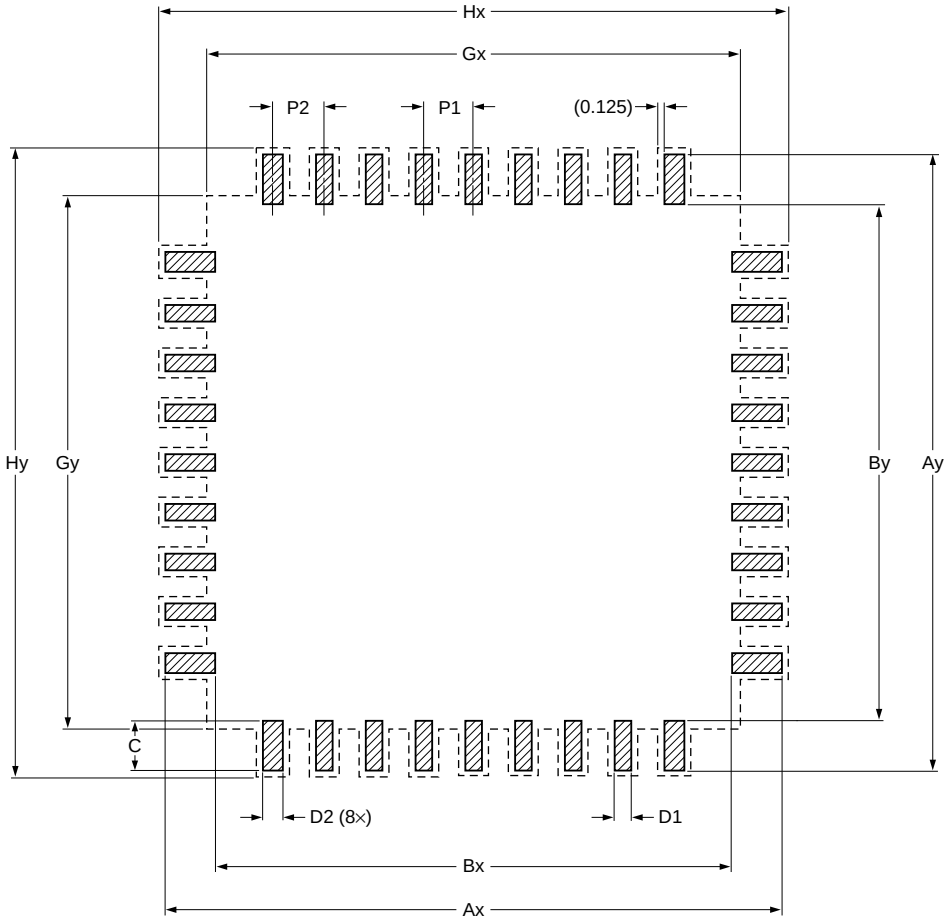
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 52. Package outline LQFP100 (SOT407-1)

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

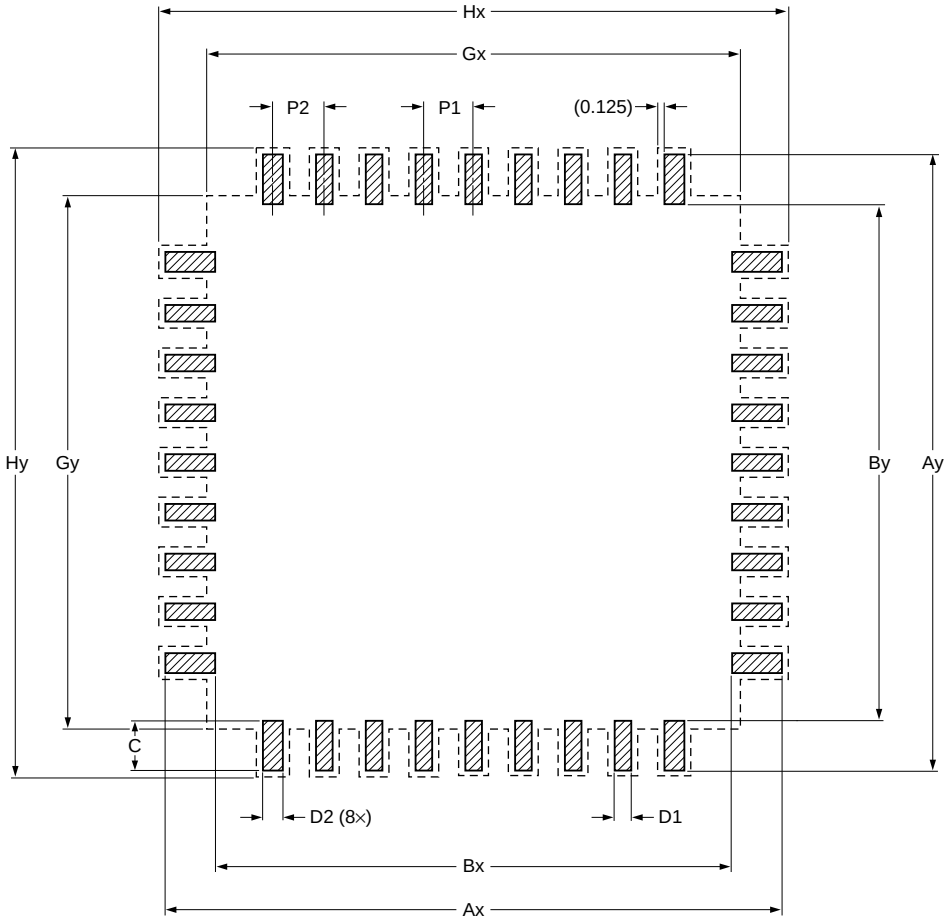
DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 54. Reflow soldering for the LQFP64 package

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 55. Reflow soldering for the LQFP100 package

17. References

[1] LPC15xx User manual UM10736:
http://www.nxp.com/documents/user_manual/UM10736.pdf

[2] LPC15xx Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC15XX.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf