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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1548jbd100e

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_8/ADC0_0/TDO	9	12	19	[2]	I; PU	IO	**PIO0_8 —** General purpose port 0 input/output 8. In boundary scan mode: TDO (Test Data Out).
						A	**ADC0_0 —** ADC0 input 0.
PIO0_9/ADC1_1/TDI	12	16	24	[2]	I; PU	IO	**PIO0_9 —** General purpose port 0 input/output 9. In boundary scan mode: TDI (Test Data In).
						A	**ADC1_1 —** ADC1 input 1.
PIO0_10/ADC1_2	15	19	28	[2]	I; PU	IO	**PIO0_10 —** General purpose port 0 input/output 10.
						A	**ADC1_2 —** ADC1 input 2.
PIO0_11/ADC1_3	18	23	33	[2]	I; PU	IO	**PIO0_11 —** General purpose port 0 input/output 11. On the LQFP64 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_3 —** ADC1 input 3.
PIO0_12/DAC_OUT	19	24	35	[3]	I; PU	IO	**PIO0_12 —** General purpose port 0 input/output 12. If this pin is configured as a digital input, the input voltage level must not be higher than V_{DDA}.
						A	**DAC_OUT —** DAC analog output.
PIO0_13/ADC1_6	21	29	43	[2]	I; PU	IO	**PIO0_13 —** General purpose port 0 input/output 13. On the LQFP64 package, this pin is assigned to U0_RXD in ISP USART mode. On the LQFP48 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_6 —** ADC1 input 6.
PIO0_14/ADC1_7/ SCT1_OUT5	22	30	45	[2]	I; PU	IO	**PIO0_14 —** General purpose port 0 input/output 14. On the LQFP48 package, this pin is assigned to U0_RXD in ISP USART mode.
						A	**ADC1_7 —** ADC1 input 7.
						O	**SCT1_OUT5 —** SCTimer1/PWM output 5.
PIO0_15/ADC1_8	23	31	47	[2]	I; PU	IO	**PIO0_15 —** General purpose port 0 input/output 15. On the LQFP48 package, this pin is assigned to U0_TXD in ISP USART mode.
						A	**ADC1_8 —** ADC1 input 8.
PIO0_16/ADC1_9	24	32	49	[2]	I; PU	IO	**PIO0_16 —** General purpose port 0 input/output 16. On the LQFP48 package, this is the ISP_1 boot pin.
						A	**ADC1_9 —** ADC1 input 9.
PIO0_17/WAKEUP/ $\overline{\text{TRST}}$	28	39	61	[4]	I; PU	IO	**PIO0_17 —** General purpose port 0 input/output 17. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. For wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. Pull this pin HIGH externally while in Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
VREFP_ADC	10	13	21		-		ADC positive reference voltage. The voltage level on VREFP_ADC must be equal to or lower than the voltage applied to V_{DDA}. If the ADC is not used, tie VREFP_ADC to V_{DD}.
V_{SSA}	17	21	31		-		Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	41, 20, 40	56, 26, 27, 55	88, 7, 39, 40, 68, 87		-		Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[3] This pin is not 5 V tolerant due to special analog functionality. When configured for a digital function, this pin is 3 V tolerant and provides standard digital I/O functions with configurable internal pull-up and pull-down resistors and hysteresis. When configured for DAC_OUT, the digital section of the pin is disabled and this pin is a 3 V tolerant analog output. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, and configurable hysteresis. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on. This pin is powered in deep power-down mode and can wake up the part. The wake-up pin function can be disabled and the pin can be used for other purposes, if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[9] Special analog pin.

[10] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[11] When the main oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. Movable functions

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.

Table 4. Movable functions *…continued*

Function name	Type	Description
DAC_PINTRIG	I	DAC external pin trigger input.
DAC_SHUTOFF	I	DAC shut-off external input.
ACMP0_O	O	Analog comparator 0 output.
ACMP1_O	O	Analog comparator 1 output.
ACMP2_O	O	Analog comparator 2 output.
ACMP3_O	O	Analog comparator 3 output.
CLKOUT	O	Clock output.
ROSC	O	Analog comparator ring oscillator output.
ROSC_RESET	I	Analog comparator ring oscillator reset.
USB_FTOGGLE	O	USB frame toggle. Do not assign this function to a pin until a USB device is connected and the first SOF interrupt has been received by the device.
QEI_PHA	I	QEI phase A input.
QEI_PHB	I	QEI phase B input.
QEI_IDX	I	QEI index input.
GPIO_INT_BMAT	O	Output of the pattern match engine.
SWO	O	Serial wire output.

Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO0_2/ADC0_6/SCT1_OUT3	3	6	8	SCT0 input multiplexer
PIO0_3/ADC0_5/SCT1_OUT4	4	7	10	SCT0 input multiplexer
PIO0_4/ADC0_4	5	8	13	SCT2 input multiplexer
PIO0_5/ADC0_3	6	9	14	FREQMEAS
PIO0_7/ADC0_1	8	11	17	SCT3 input multiplexer
PIO0_14/ADC1_7/SCT1_OUT5	22	30	45	SCTIPU input SAMPLE_IN_A0
PIO0_15/ADC1_8	23	31	47	SCT1 input multiplexer
PIO0_16/ADC1_9	24	32	49	SCT1 input multiplexer
PIO0_17/WAKEUP/$\overline{\text{TRST}}$	28	39	61	SCT0 input multiplexer
SWCLK/PIO0_19/TCK	29	40	63	FREQMEAS
$\overline{\text{RESET}}$/PIO0_21	34	45	71	SCT1 input multiplexer
PIO0_25/ACMP0_I4	44	60	93	SCTIPU input SAMPLE_IN_A1
PIO0_27/ACMP_I1	46	62	97	SCT2 input multiplexer
PIO0_30/ADC0_11	-	1	1	FREQMEAS
				SCT0 input multiplexer
PIO0_31/ADC0_9	-	3	3	SCT1 input multiplexer
PIO1_4/ADC1_10	-	33	51	SCT1 input multiplexer
PIO1_5/ADC1_11	-	34	52	SCT1 input multiplexer
PIO1_6/ACMP_I2	-	46	73	SCT0 input multiplexer

Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO1_7/ACMP3_I4	-	51	81	SCT0 input multiplexer
PIO1_11	-	38	58	SCT3 input multiplexer
				SCTIPU input SAMPLE_IN_A2
PIO1_12	-	-	9	SCT0 input multiplexer
PIO1_13	-	-	11	SCT0 input multiplexer
PIO1_15	-	-	12	SCT1 input multiplexer
PIO1_16	-	-	18	SCT1 input multiplexer
PIO1_18	-	-	25	SCT2 input multiplexer
PIO1_19	-	-	29	SCT2 input multiplexer
PIO1_21	-	-	37	SCT3 input multiplexer
PIO1_22	-	-	38	SCT3 input multiplexer
PIO1_26	-	-	48	SCTIPU input SAMPLE_IN_A3
PIO1_27	-	-	50	FREQMEAS

8. Functional description

8.1 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual*, which is available on the official ARM website.

8.2 Memory Protection Unit (MPU)

The LPC15xx have a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

8.4 EEPROM

The LPC15xx contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

8.5 SRAM

The LPC15xx contain a total 36 kB, 20 kB or 12 kB of contiguous, on-chip static RAM memory. For each SRAM configuration, the SRAM is divided into three blocks: 2 x 16 kB + 4 kB for 36 kB SRAM, 2 x 8 kB + 4 kB for 20 kB SRAM, and 2 x 4 kB + 4 kB for 12 kB SRAM. The bottom 16 kB, 8 kB, or 4 kB are enabled by the bootloader and cannot be disabled. The next two SRAM blocks in each configuration can be disabled or enabled individually in the SYSCON block to save power.

Table 8. LPC15xx SRAM configurations

	SRAM0	SRAM1	SRAM2
LPC1549/19 (total SRAM = 36 kB)			
address range	0x0200 0000 to 0x0200 3FFF	0x0200 4000 to 0x0200 7FFF	0x0200 8000 to 0x0200 8FFF
size	16 kB	16 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1548/18 (total SRAM = 20 kB)			
address range	0x0200 0000 to 0x0200 1FFF	0x0200 2000 to 0x0200 3FFF	0x0200 4000 to 0x0200 4FFF
size	8 kB	8 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1547/17 (total SRAM = 12 kB)			
address range	0x0200 0000 to 0x0200 0FFF	0x0200 1000 to 0x0200 1FFF	0x0200 2000 to 0x0200 2FFF
size	4 kB	4 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled

8.6 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Flash updates via USB and C_CAN supported.
- USB API (HID, CDC, and MSC drivers).
- DMA, I2C, USART, SPI, and C_CAN drivers.
- Power profiles for configuring power consumption and PLL settings.

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter configurable on all pins
- Digital input: Input glitch filter enabled/disabled on select pins
- Analog input

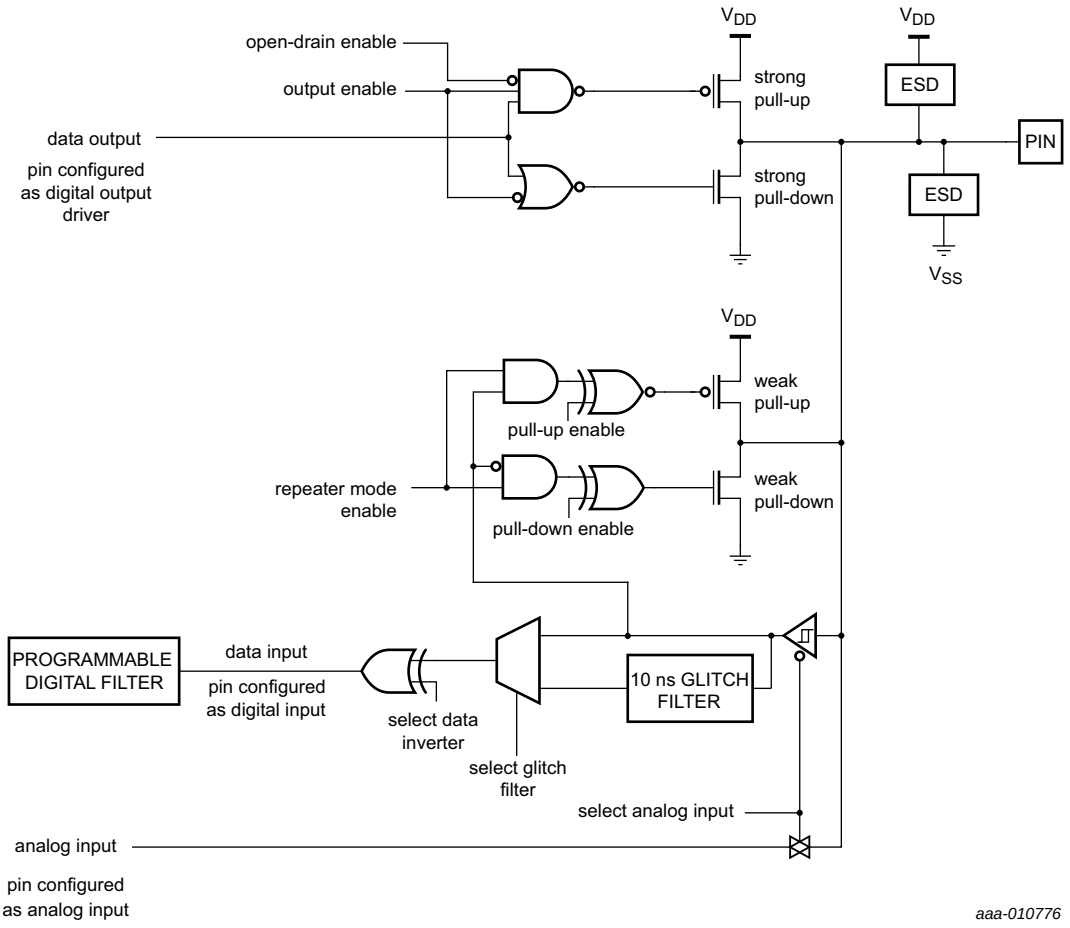


Fig 11. Standard I/O pin configuration

8.11 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the ADC or analog comparator inputs can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.26.1 Features

- Seven selectable inputs. Fully configurable on either the positive side or the negative input channel.
- 32-stage voltage ladder internal reference for selectable voltages on each comparator; configurable on either positive or negative comparator input.
- Voltage ladder source voltage is selectable from an external pin or the 3.3 V analog voltage supply.
- 0.9 V internal band gap reference voltage selectable as either positive or negative input on each comparator.
- Temperature sensor voltage selectable as either positive or negative input on each comparator.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Individual comparator outputs can be connected internally to the SCT and ADC trigger inputs or the external pins.
- Separate interrupt for each comparator.
- Pin filter included on each comparator output.
- Three propagation delay values are programmable to optimize between speed and power consumption.
- Relaxation oscillator circuitry output for a 555 style timer operation using comparator blocks 0 and 1.

8.27 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.28 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.905 V. The internal voltage reference can be used in the following applications:

- When the supply voltage V_{DD} is known accurately, the internal voltage reference can be used to reduce the offset error E_O of the ADC code output. The ADC error correction then increases the accuracy of temperature sensor voltage output measurements.

8.38 Clock output

The LPC15xx feature a clock output function that routes the internal oscillator outputs, the PLL outputs, or the main clock an output pin where they can be observed directly.

8.39 Wake-up process

The LPC15xx begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the system oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and system oscillator as a clock source.

8.40 Power control

The LPC15xx support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides additional power control.

8.40.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC15xx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock and to easily set the configuration options for Deep-sleep and power-down modes.

Remark: When using the USB, configure the LPC15xx in Default mode.

8.40.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

[5] IRC enabled; system oscillator disabled; system PLL disabled.

[6] System oscillator enabled; IRC disabled; system PLL disabled.

[7] BOD disabled.

[8] All peripherals disabled in the SYSAHBCLKCTRL0/1 registers. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[9] IRC enabled; system oscillator disabled; system PLL enabled.

[10] IRC disabled; system oscillator enabled; system PLL enabled.

[11] All oscillators and analog blocks turned off: Use API power_mode_configure() with mode parameter set to DEEP_SLEEP or POWER_DOWN and peripheral parameter set to 0xFF.

[12] WAKEUP pin pulled HIGH externally.

[13] RTC running or not running.

[14] Characterized on samples. Not tested in production.

[15] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[16] Including voltage on outputs in tri-state mode.

[17] V_{DD} supply voltage must be present.

[18] Tri-state outputs go into tri-state mode in Deep power-down mode.

[19] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[20] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 17.

[21] To V_{SS}.

[22] The parameter values specified are simulated and absolute values.

[23] The input voltage of the RTC oscillator is limited as follows: $V_{i(rtcx)}$, $V_{o(rtcx)}$ < max(VBAT, V_{DD}).

[24] Including bonding pad capacitance.

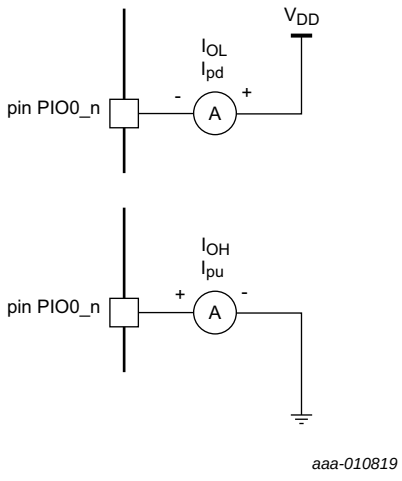
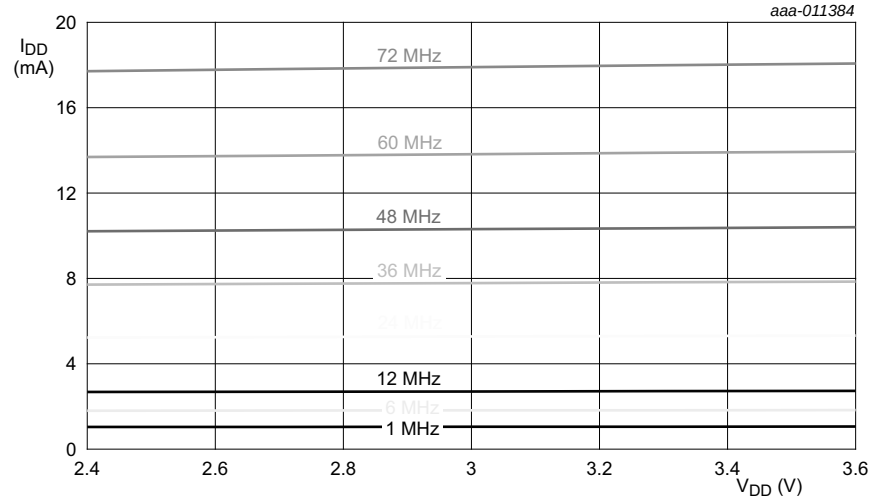


Fig 17. Pin input/output current measurement

11.1 Power consumption

Power measurements in Active, Sleep, Deep-sleep, and Power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.



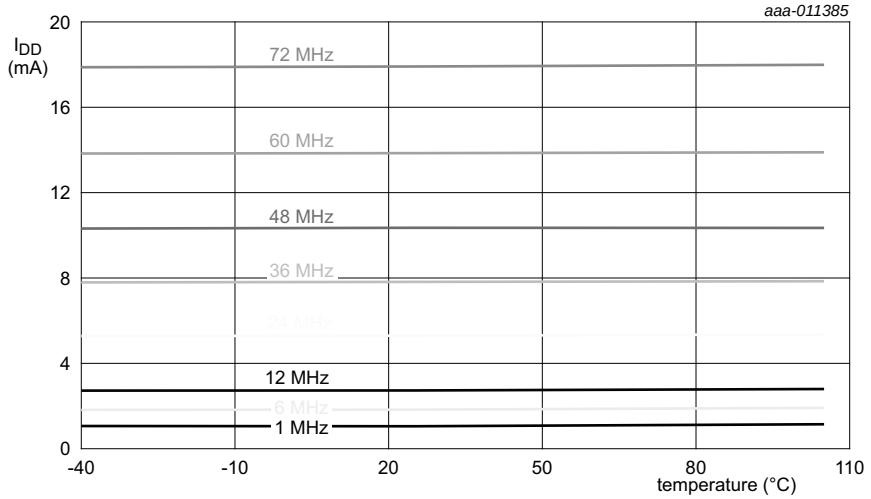
Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 18. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD}



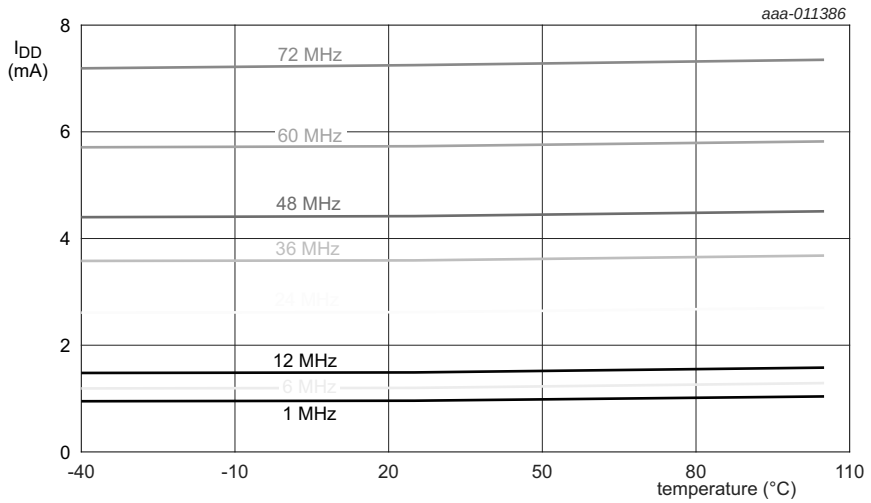
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 19. Active mode: Typical supply current I_{DD} versus temperature



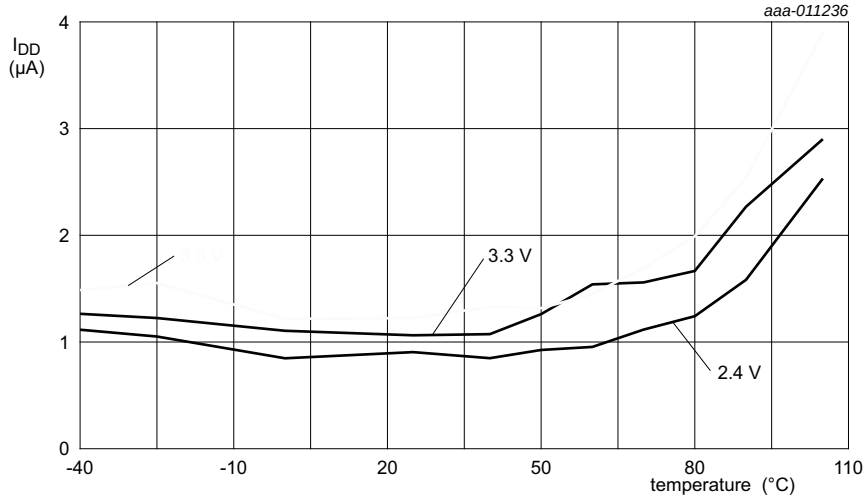
Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

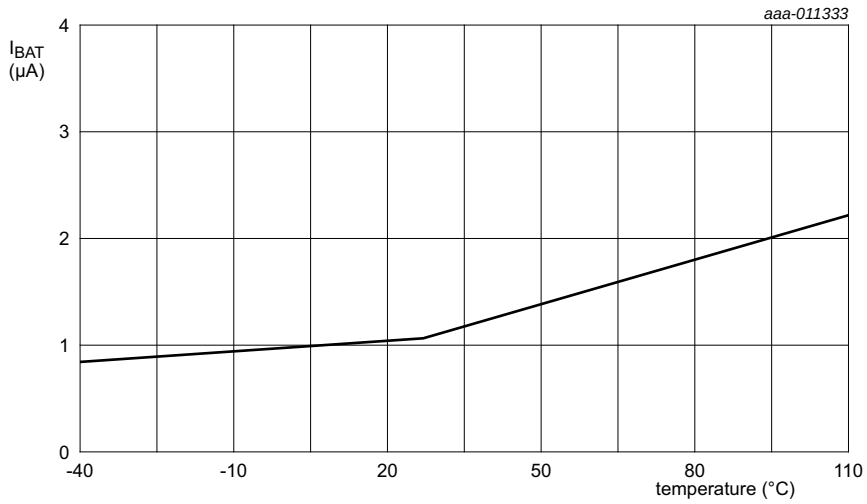
24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 20. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



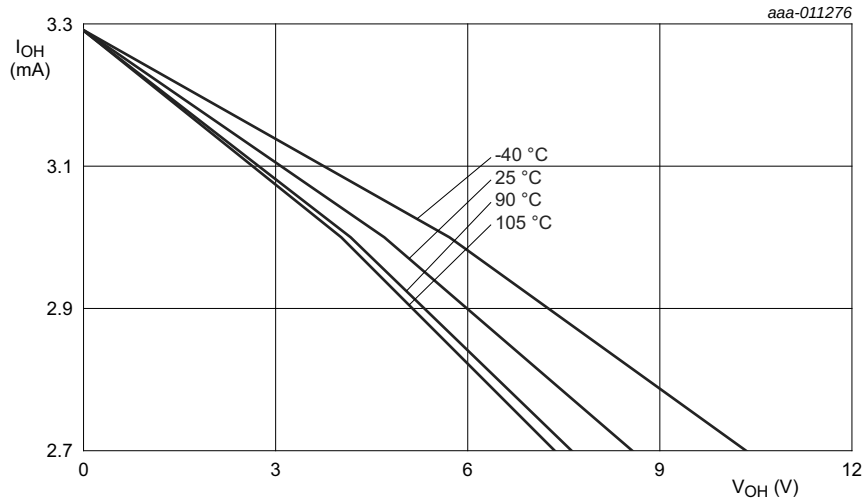
VBAT = 0 V.

Fig 23. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



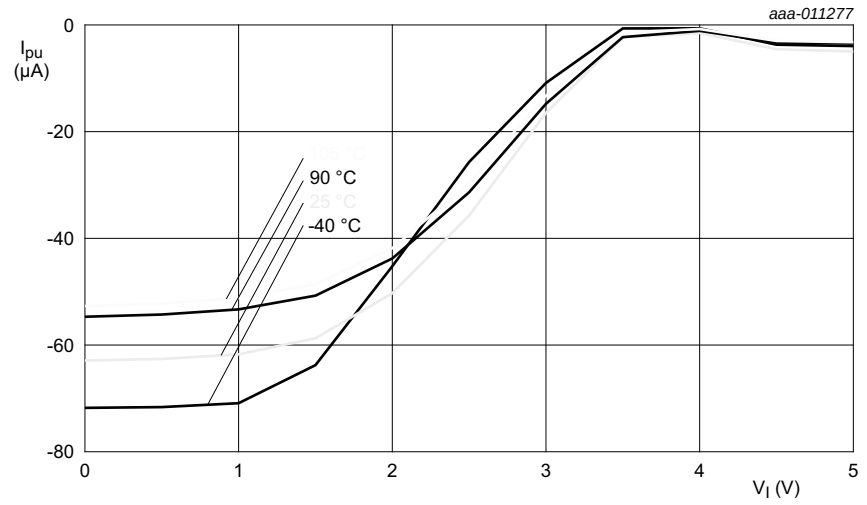
VBAT = 3.3 V; V_{DD} floating.

Fig 24. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 30. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 31. Typical pull-up current I_{pu} versus input voltage V_I

12. Dynamic characteristics

12.1 Flash/EEPROM memory

Table 13. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	20	-	years
		not powered	20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC15xx user manual*).

Table 14. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		not powered	150	300	-	years
t_{prog}	programming time	64 bytes	-	2.9	-	ms

12.2 External clock for the oscillator in slave mode

Remark: The input voltage on the XTALIN and XTALOUT pins must be ≤ 1.95 V (see Table 11). For connecting the oscillator to the XTAL pins, also see Section 14.3.

Table 15. Dynamic characteristic: external clock (XTALIN input)

T_{amb} = −40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

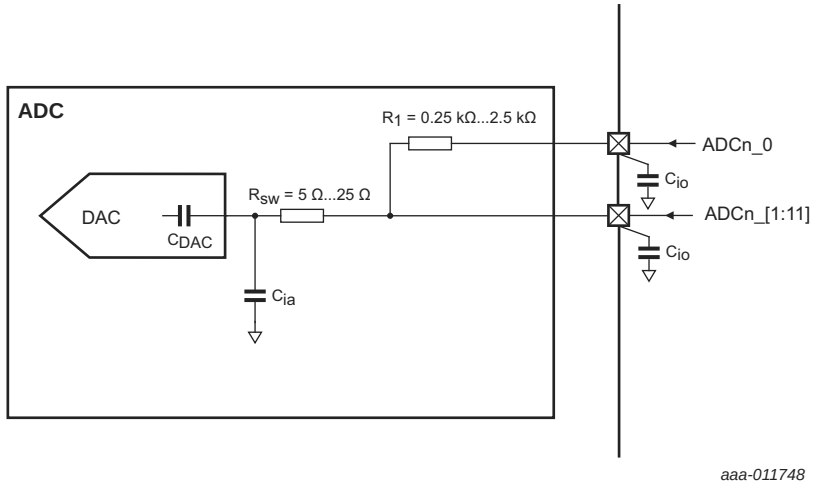


Fig 39. ADC input impedance

14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 24:

- The ADC input trace must be short and as close as possible to the LPC15xx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 44) or bus-powered device (see Figure 45).

On the LPC15xx, the PIO0_3/USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always greater than 0 V while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.

14.8 Pin states in different power modes

Table 35. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_22, PIO0_23 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$/PIO0_21	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, addan external pull-up to the $\overline{\text{RESET}}$ pin to reduce power consumption.
PIO0_17/ WAKEUP/$\overline{\text{TRST}}$	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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