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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	44
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1548jbd64ql

- Analog peripherals:
  - Two 12-bit ADC with up to 12 input channels per ADC and with multiple internal and external trigger inputs and sample rates of up to 2 Msamples/s. Each ADC supports two independent conversion sequences. ADC conversion clock can be the system clock or an asynchronous clock derived from one of the three PLLs.
  - One 12-bit DAC.
  - Integrated temperature sensor and band gap internal reference voltage.
  - Four comparators with external and internal voltage references (ACMP0 to 3). Comparator outputs are internally connected to the SCTimer/PWMs and ADCs and externally to pins. Each comparator output contains a programmable glitch filter.
- Serial interfaces:
  - Three USART interfaces with DMA, RS-485 support, autobaud, and with synchronous mode and 32 kHz mode for wake-up from Deep-sleep and Power-down modes. The USARTs share a fractional baud-rate generator.
  - Two SPI controllers.
  - One I^2C-bus interface supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode.
  - One C_CAN controller.
  - One USB 2.0 full-speed device controller with on-chip PHY.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Watchdog oscillator with a frequency range of 503 kHz.
  - 32 kHz low-power RTC oscillator with 32 kHz, 1 kHz, and 1 Hz outputs.
  - System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Two additional PLLs for generating the USB and SCTimer/PWM clocks.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - APIs provided for optimizing power consumption in active and sleep modes and for configuring Deep-sleep, Power-down, and Deep power-down modes.
  - Wake-up from Deep-sleep and Power-down modes on activity on USB, USART, SPI, and I2C peripherals.
  - Wake-up from Sleep, Deep-sleep, Power-down, and Deep power-down modes from the RTC alarm or wake-up interrupts.
  - Timer-controlled self wake-up from Deep power-down mode using the RTC high-resolution/wake-up 1 kHz timer.
  - Power-On Reset (POR).
  - BrownOut Detect BOD).
- JTAG boundary scan modes supported.
- Unique device serial number for identification.

- Single power supply 2.4 V to 3.6 V.
- Temperature range −40 °C to +105 °C.
- Available as LQFP100, LQFP64, and LQFP48 packages.

3. Applications

- Motor control
- Motion drives
- Digital power supplies
- Industrial and medical
- Solar inverters
- Home appliances
- Building and factory automation

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1549JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1549JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1549JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1548JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1548JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1519JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1519JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1518JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1518JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_27/ACMP_I1	46	62	97	[2]	I; PU	IO	**PIO0_27 —** General purpose port 0 input/output 27.
						A	**ACMP_I1 —** Analog comparator common input 1.
PIO0_28/ACMP1_I3	47	63	98	[2]	I; PU	IO	**PIO0_28 —** General purpose port 0 input/output 28.
						A	**ACMP1_I3 —** Analog comparator 1 input 3.
PIO0_29/ACMP2_I3/ SCT2_OUT4	48	64	100	[2]	I; PU	IO	**PIO0_29 —** General purpose port 0 input/output 29.
						A	**ACMP2_I3 —** Analog comparator 2 input 3.
						O	**SCT2_OUT4 —** SCTimer2/PWM output 4.
PIO0_30/ADC0_11	-	1	1	[2]	I; PU	IO	**PIO0_30 —** General purpose port 0 input/output 30.
						A	**ADC0_11 —** ADC0 input 11.
PIO0_31/ADC0_9	-	3	3	[2]	I; PU	IO	**PIO0_31 —** General purpose port 0 input/output 31. On the LQFP64 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						A	**ADC0_9 —** ADC0 input 9.
PIO1_0/ADC0_8	-	4	5	[2]	I; PU	IO	**PIO1_0 —** General purpose port 1 input/output 0.
						A	**ADC0_8 —** ADC0 input 8.
PIO1_1/ADC1_0	-	15	23	[2]	I; PU	IO	**PIO1_1 —** General purpose port 1 input/output 1.
						A	**ADC1_0 —** ADC1 input 0.
PIO1_2/ADC1_4	-	25	36	[2]	I; PU	IO	**PIO1_2 —** General purpose port 1 input/output 2.
						A	**ADC1_4 —** ADC1 input 4.
PIO1_3/ADC1_5	-	28	41	[2]	I; PU	IO	**PIO1_3 —** General purpose port 1 input/output 3.
						A	**ADC1_5 —** ADC1 input 5.
PIO1_4/ADC1_10	-	33	51	[2]	I; PU	IO	**PIO1_4 —** General purpose port 1 input/output 4.
						A	**ADC1_10 —** ADC1 input 10.
PIO1_5/ADC1_11	-	34	52	[2]	I; PU	IO	**PIO1_5 —** General purpose port 1 input/output 5.
						A	**ADC1_11 —** ADC1 input 11.
PIO1_6/ACMP_I2	-	46	73	[2]	I; PU	IO	**PIO1_6 —** General purpose port 1 input/output 6.
						A	**ACMP_I2 —** Analog comparator common input 2.
PIO1_7/ACMP3_I4	-	51	81	[2]	I; PU	IO	**PIO1_7 —** General purpose port 1 input/output 7.
						A	**ACMP3_I4 —** Analog comparator 3 input 4.
PIO1_8/ACMP3_I3/ SCT3_OUT4	-	53	84	[2]	I; PU	IO	**PIO1_8 —** General purpose port 1 input/output 8.
						A	**ACMP3_I3 —** Analog comparator 3 input 3.
						O	**SCT3_OUT4 —** SCTimer3/PWM output 4.
PIO1_9/ACMP2_I4	-	54	85	[2]	I; PU	IO	**PIO1_9 —** General purpose port 1 input/output 9. On the LQFP64 package, this is the ISP_0 boot pin.
						A	**ACMP2_I4 —** Analog comparator 2 input 4.
PIO1_10/ACMP1_I4	-	59	91	[2]	I; PU	IO	**PIO1_10 —** General purpose port 1 input/output 10.
						A	**ACMP1_I4 —** Analog comparator 1 input 4.
PIO1_11	-	38	58	[5]	I; PU	IO	**PIO1_11 —** General purpose port 1 input/output 11. On the LQFP64 package, this is the ISP_1 boot pin.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO1_12	-	-	9	[5]	I; PU	IO	**PIO1_12 —** General purpose port 1 input/output 12.
PIO1_13	-	-	11	[5]	I; PU	IO	**PIO1_13 —** General purpose port 1 input/output 13.
PIO1_14/SCT0_OUT7	-	-	12	[5]	I; PU	IO	**PIO1_14 —** General purpose port 1 input/output 14.
						O	**SCT0_OUT7 —** SCTimer0/PWM output 7.
PIO1_15	-	-	15	[5]	I; PU	IO	**PIO1_15 —** General purpose port 1 input/output 15.
PIO1_16	-	-	18	[5]	I; PU	IO	**PIO1_16 —** General purpose port 1 input/output 16.
PIO1_17/SCT1_OUT7	-	-	20	[5]	I; PU	IO	**PIO1_17 —** General purpose port 1 input/output 17.
						O	**SCT1_OUT7 —** SCTimer1/PWM output 7.
PIO1_18	-	-	25	[5]	I; PU	IO	**PIO1_18 —** General purpose port 1 input/output 18.
PIO1_19	-	-	29	[5]	I; PU	IO	**PIO1_19 —** General purpose port 1 input/output 19.
PIO1_20/SCT2_OUT5	-	-	34	[5]	I; PU	IO	**PIO1_20 —** General purpose port 1 input/output 20.
						O	**SCT2_OUT5 —** SCTimer2/PWM output 5.
PIO1_21	-	-	37	[5]	I; PU	IO	**PIO1_21 —** General purpose port 1 input/output 21.
PIO1_22	-	-	38	[5]	I; PU	IO	**PIO1_22 —** General purpose port 1 input/output 22.
PIO1_23	-	-	42	[5]	I; PU	IO	**PIO1_23 —** General purpose port 1 input/output 23.
PIO1_24/SCT3_OUT5	-	-	44	[5]	I; PU	IO	**PIO1_24 —** General purpose port 1 input/output 24.
						O	**SCT3_OUT5 —** SCTimer3/PWM output 5.
PIO1_25	-	-	46	[5]	I; PU	IO	**PIO1_25 —** General purpose port 1 input/output 25.
PIO1_26	-	-	48	[5]	I; PU	IO	**PIO1_26 —** General purpose port 1 input/output 26.
PIO1_27	-	-	50	[5]	I; PU	IO	**PIO1_27 —** General purpose port 1 input/output 27.
PIO1_28	-	-	55	[5]	I; PU	IO	**PIO1_28 —** General purpose port 1 input/output 28.
PIO1_29	-	-	56	[5]	I; PU	IO	**PIO1_29 —** General purpose port 1 input/output 29.
PIO1_30	-	-	59	[5]	I; PU	IO	**PIO1_30 —** General purpose port 1 input/output 30.
PIO1_31	-	-	60	[5]	I; PU	IO	**PIO1_31 —** General purpose port 1 input/output 31.
PIO2_0	-	-	62	[5]	I; PU	IO	**PIO2_0 —** General purpose port 2 input/output 0.
PIO2_1	-	-	64	[5]	I; PU	IO	**PIO2_1 —** General purpose port 2 input/output 1.
PIO2_2	-	-	72	[5]	I; PU	IO	**PIO2_2 —** General purpose port 2 input/output 2.
PIO2_3	-	-	76	[5]	I; PU	IO	**PIO2_3 —** General purpose port 2 input/output 3.
PIO2_4	-	-	77	[5]	I; PU	IO	**PIO2_4 —** General purpose port 2 input/output 4. On the LQFP100 package, this is the ISP_1 boot pin.
PIO2_5	-	-	80	[5]	I; PU	IO	**PIO2_5 —** General purpose port 2 input/output 5. On the LQFP100 package, this is the ISP_0 boot pin.
PIO2_6	-	-	82	[5]	I; PU	IO	**PIO2_6 —** General purpose port 2 input/output 6. On the LQFP100 package, this pin is assigned to U0_TXD in ISP USART mode.
PIO2_7	-	-	86	[5]	I; PU	IO	**PIO2_7 —** General purpose port 2 input/output 7. On the LQFP100 package, this pin is assigned to U0_RXD in ISP USART mode.

8.4 EEPROM

The LPC15xx contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

8.5 SRAM

The LPC15xx contain a total 36 kB, 20 kB or 12 kB of contiguous, on-chip static RAM memory. For each SRAM configuration, the SRAM is divided into three blocks: 2 x 16 kB + 4 kB for 36 kB SRAM, 2 x 8 kB + 4 kB for 20 kB SRAM, and 2 x 4 kB + 4 kB for 12 kB SRAM. The bottom 16 kB, 8 kB, or 4 kB are enabled by the bootloader and cannot be disabled. The next two SRAM blocks in each configuration can be disabled or enabled individually in the SYSCON block to save power.

Table 8. LPC15xx SRAM configurations

	SRAM0	SRAM1	SRAM2
LPC1549/19 (total SRAM = 36 kB)			
address range	0x0200 0000 to 0x0200 3FFF	0x0200 4000 to 0x0200 7FFF	0x0200 8000 to 0x0200 8FFF
size	16 kB	16 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1548/18 (total SRAM = 20 kB)			
address range	0x0200 0000 to 0x0200 1FFF	0x0200 2000 to 0x0200 3FFF	0x0200 4000 to 0x0200 4FFF
size	8 kB	8 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1547/17 (total SRAM = 12 kB)			
address range	0x0200 0000 to 0x0200 0FFF	0x0200 1000 to 0x0200 1FFF	0x0200 2000 to 0x0200 2FFF
size	4 kB	4 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled

8.6 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Flash updates via USB and C_CAN supported.
- USB API (HID, CDC, and MSC drivers).
- DMA, I2C, USART, SPI, and C_CAN drivers.
- Power profiles for configuring power consumption and PLL settings.

8.12 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function through the switch matrix are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC15xx use accelerated GPIO functions.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.12.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.13 Pin interrupt/pattern match engine (PINT)

The pin interrupt block configures up to eight pins from the digital pins on ports 1 and 2 for providing eight external interrupts connected to the NVIC. The input multiplexer block is used to select the pins.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin on ports 0 and 1 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.13.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU.
  - The pattern match engine does not facilitate wake-up.

8.18 USART0/1/2

Remark: All USART functions are movable functions and are assigned to pins through the switch matrix. Do not connect USART functions to the open-drain pins PIO0_22 and PIO0_23.

Interrupts generated by the USART peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled.

8.18.1 Features

- Maximum bit rates of 4.5 Mbit/s in asynchronous mode, 15 Mbit/s in synchronous mode master mode, and 18 Mbit/s in synchronous slave mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep and power-down modes.
- Special operating mode allows operation at up to 9600 baud using the 32 kHz RTC oscillator as the UART clock. This mode can be used while the device is in Deep-sleep or Power-down mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

8.19 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix. Do not connect SPI functions to the open-drain pins PIO0_22 and PIO0_23.

8.26.1 Features

- Seven selectable inputs. Fully configurable on either the positive side or the negative input channel.
- 32-stage voltage ladder internal reference for selectable voltages on each comparator; configurable on either positive or negative comparator input.
- Voltage ladder source voltage is selectable from an external pin or the 3.3 V analog voltage supply.
- 0.9 V internal band gap reference voltage selectable as either positive or negative input on each comparator.
- Temperature sensor voltage selectable as either positive or negative input on each comparator.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Individual comparator outputs can be connected internally to the SCT and ADC trigger inputs or the external pins.
- Separate interrupt for each comparator.
- Pin filter included on each comparator output.
- Three propagation delay values are programmable to optimize between speed and power consumption.
- Relaxation oscillator circuitry output for a 555 style timer operation using comparator blocks 0 and 1.

8.27 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.28 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.905 V. The internal voltage reference can be used in the following applications:

- When the supply voltage V_{DD} is known accurately, the internal voltage reference can be used to reduce the offset error E_O of the ADC code output. The ADC error correction then increases the accuracy of temperature sensor voltage output measurements.

Table 10. Thermal resistance value (C/W): ±15 %

Symbol	Parameter	Conditions	Typ	Unit
LQFP48				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	64	°C/W
		1 m/s	55	°C/W
		2.5 m/s	50	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	96	°C/W
		1 m/s	76	°C/W
		2.5 m/s	67	°C/W
θjc	thermal resistance junction-to-case		13	°C/W
θjb	thermal resistance junction-to-board		16	°C/W
LQFP64				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	51	°C/W
		1 m/s	45	°C/W
		2.5 m/s	41	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	75	°C/W
		1 m/s	60	°C/W
		2.5 m/s	54	°C/W
θjc	thermal resistance junction-to-case		13	°C/W
θjb	thermal resistance junction-to-board		17	°C/W
LQFP100				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	42	°C/W
		1 m/s	37	°C/W
		2.5 m/s	34	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	59	°C/W
		1 m/s	48	°C/W
		2.5 m/s	44	°C/W
θjc	thermal resistance junction-to-case		12	°C/W
θjb	thermal resistance junction-to-board		17	°C/W

[5] IRC enabled; system oscillator disabled; system PLL disabled.

[6] System oscillator enabled; IRC disabled; system PLL disabled.

[7] BOD disabled.

[8] All peripherals disabled in the SYSAHBCLKCTRL0/1 registers. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[9] IRC enabled; system oscillator disabled; system PLL enabled.

[10] IRC disabled; system oscillator enabled; system PLL enabled.

[11] All oscillators and analog blocks turned off: Use API power_mode_configure() with mode parameter set to DEEP_SLEEP or POWER_DOWN and peripheral parameter set to 0xFF.

[12] WAKEUP pin pulled HIGH externally.

[13] RTC running or not running.

[14] Characterized on samples. Not tested in production.

[15] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[16] Including voltage on outputs in tri-state mode.

[17] V_{DD} supply voltage must be present.

[18] Tri-state outputs go into tri-state mode in Deep power-down mode.

[19] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[20] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 17.

[21] To V_{SS}.

[22] The parameter values specified are simulated and absolute values.

[23] The input voltage of the RTC oscillator is limited as follows: $V_{i(rtcx)}$, $V_{o(rtcx)}$ < max(VBAT, V_{DD}).

[24] Including bonding pad capacitance.

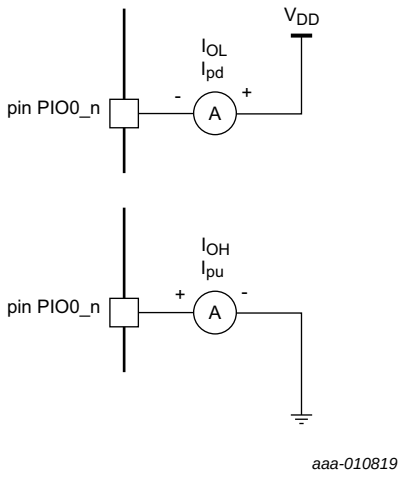
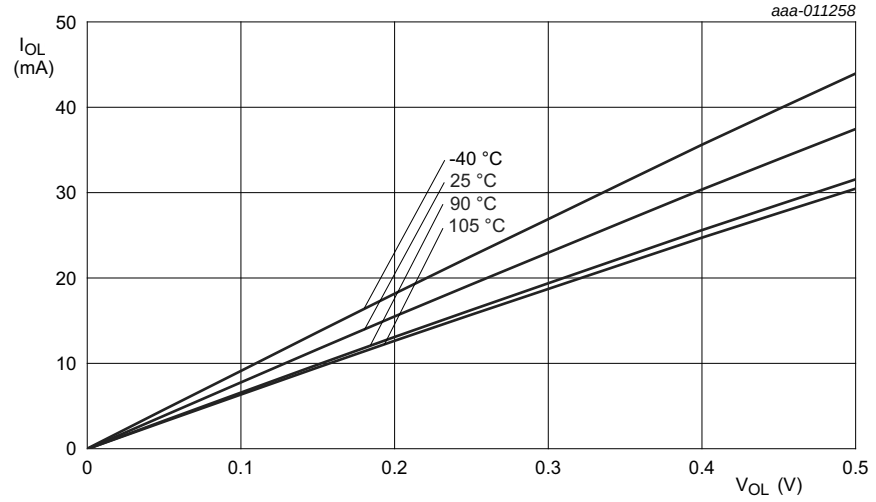
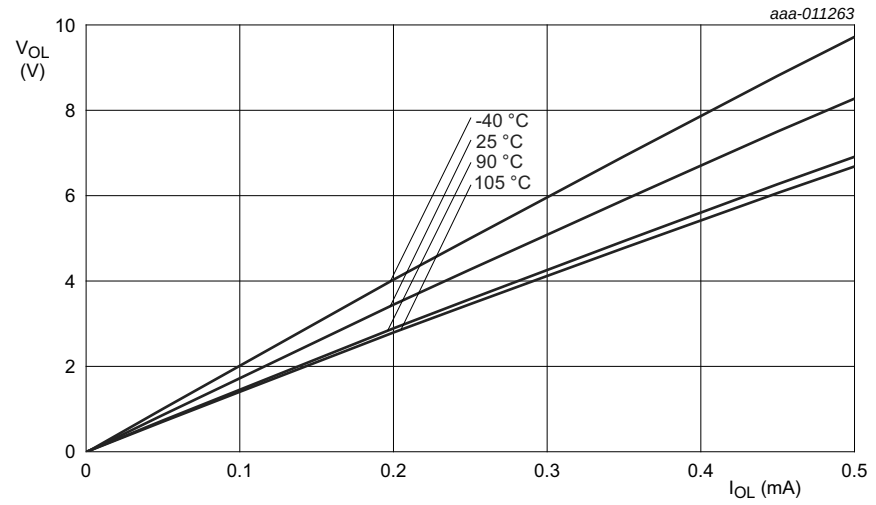


Fig 17. Pin input/output current measurement



Conditions: V_{DD} = 3.3 V; on pins PIO0_22 and PIO0_23.

Fig 28. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_24.

Fig 29. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

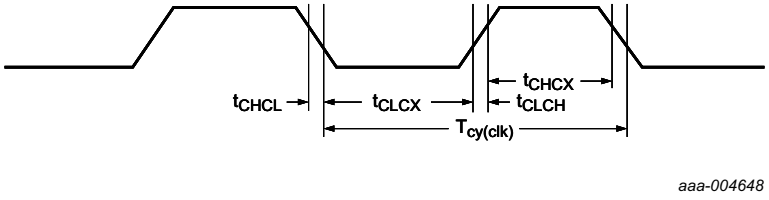


Fig 33. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

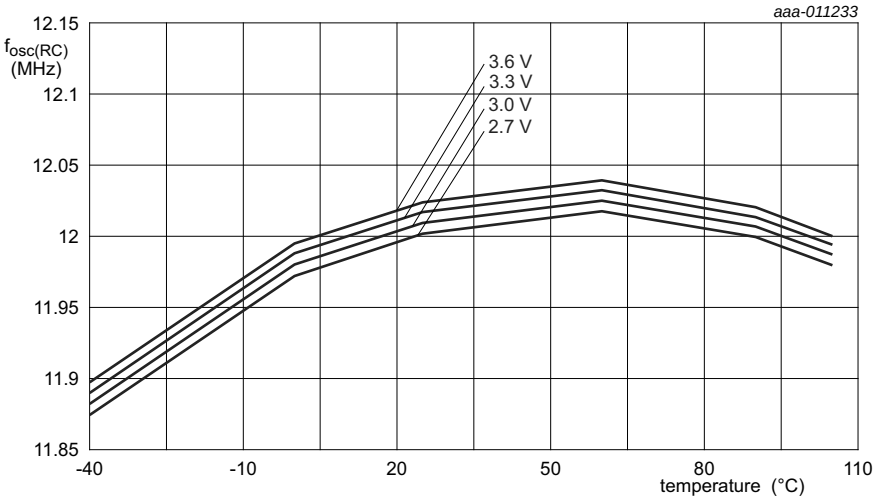
Table 16. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1%	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2%	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 34. Typical Internal RC oscillator frequency versus temperature

Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

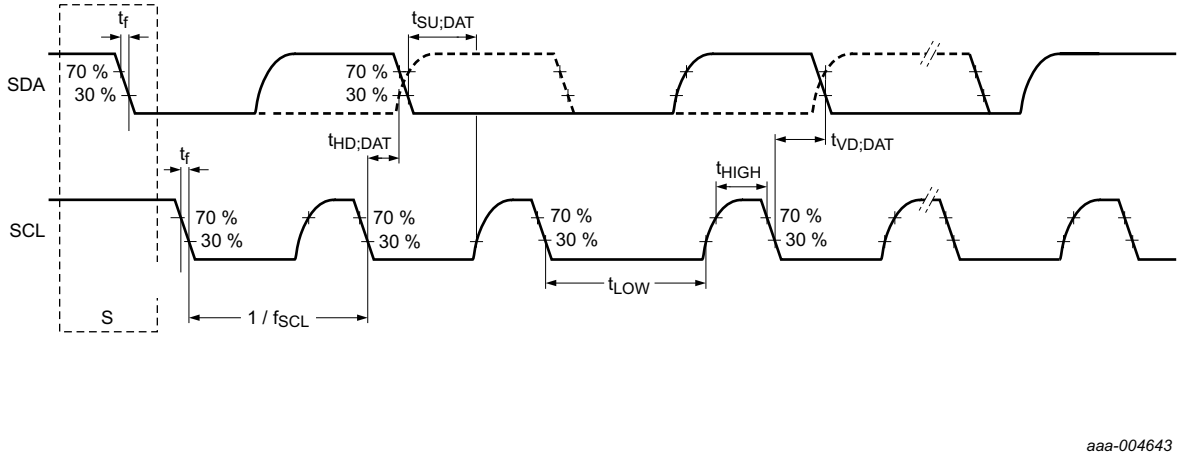


Fig 35. I²C-bus pins clock timing

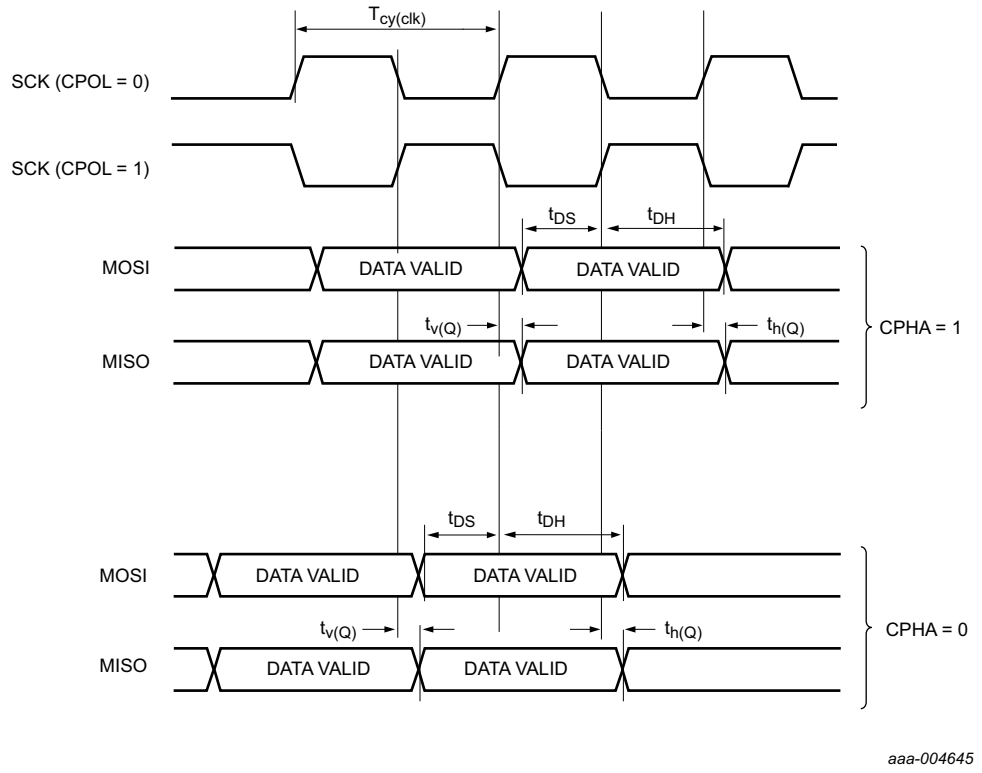


Fig 37. SPI slave timing

12.8 SCTimer/PWM output timing

Table 22. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V C_l = 10 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	SCTimer0/PWM	-	-	4	ns
		SCTimer1/PWM	-	-	3	ns
		SCTimer2/PWM	-	-	1	ns
		SCTimer3/PWM	-	-	2	ns

13. Characteristics of analog peripherals

Table 23. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2				
		assertion	-	2.55	-	V
		de-assertion	-	2.69	-	V
		interrupt level 3				
		assertion	-	2.83	-	V
		de-assertion	-	2.96	-	V
		reset level 2				
		assertion	-	2.34	-	V
		de-assertion	-	2.49	-	V
		reset level 3				
		assertion	-	2.64	-	V
		de-assertion	-	2.79	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC15xx *user manual*.

Table 25. DAC static and dynamic characteristics

V_{DDA} = 2.4 V to 3.6 V; T_{amb} = −40 °C to +105 °C unless otherwise specified; C_L = 100 pF; R_L = 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$f_{c(DAC)}$	DAC conversion frequency		-	-	500	kSamples/s
R_O	output resistance		-	300		Ω
t_s	settling time		-	-	2.5	μs
E_D	differential linearity error		-	-	+/-0.4	LSB
$E_{L(adj)}$	integral non-linearity		-	-	+/-3	LSB
E_O	offset error	VDDA = 3.3 V	-	-	+/-9	LSB
		VDDA = 2.4 V	-	-	+/-8	LSB
E_G	gain error		-	-	+/- 0.1	%
V_O	output voltage	Output voltage range with less than 1 LSB deviation; with minimum R_L connected to ground or power supply	-	-	V_{DDA} - 0.3	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

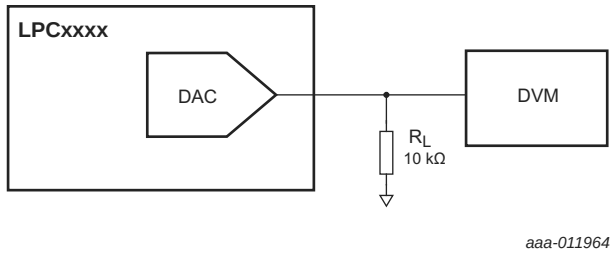


Fig 41. DAC test circuit

14.7 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as GPIO (switch matrix default) and setto outputs driving LOW with their internal pull-up disabled. To drive the output LOW, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

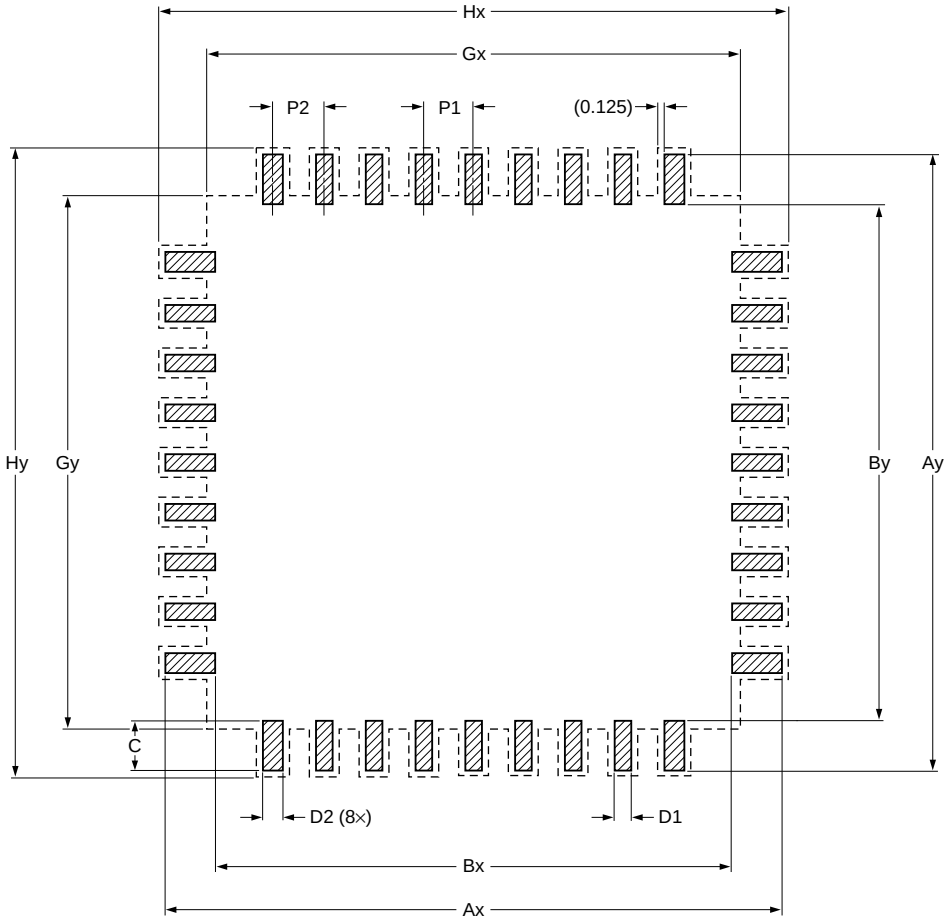
In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_21	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether Deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
USB_DP/USB_DM	F	Can be left unconnected. When the USP PHY is disabled, the pins are LOW.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP_DAC_VDDCMP	-	Tie to VDD.
VREFP_ADC		Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VBAT	-	Tie to VDD if no external battery connected.
VSSA	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 54. Reflow soldering for the LQFP64 package

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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