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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	76
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1549jbd100e

5. Marking

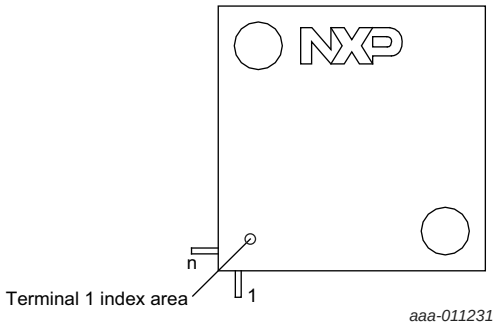


Fig 1. LQFP64/100 package marking

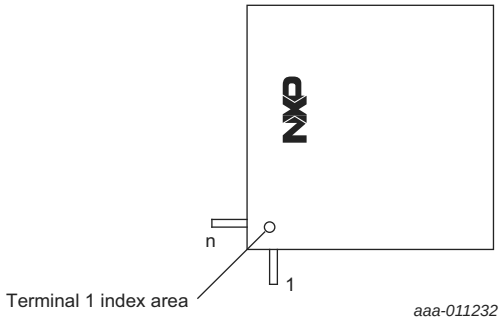


Fig 2. LQFP48 package marking

The LPC15xx devices typically have the following top-side marking for LQFP100 packages:

LPC15xxJxxx
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP64 packages:

LPC15xxJ
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP48 packages:

LPC15xxJ
Xxxxxx
Xxxyy
wwxxx

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

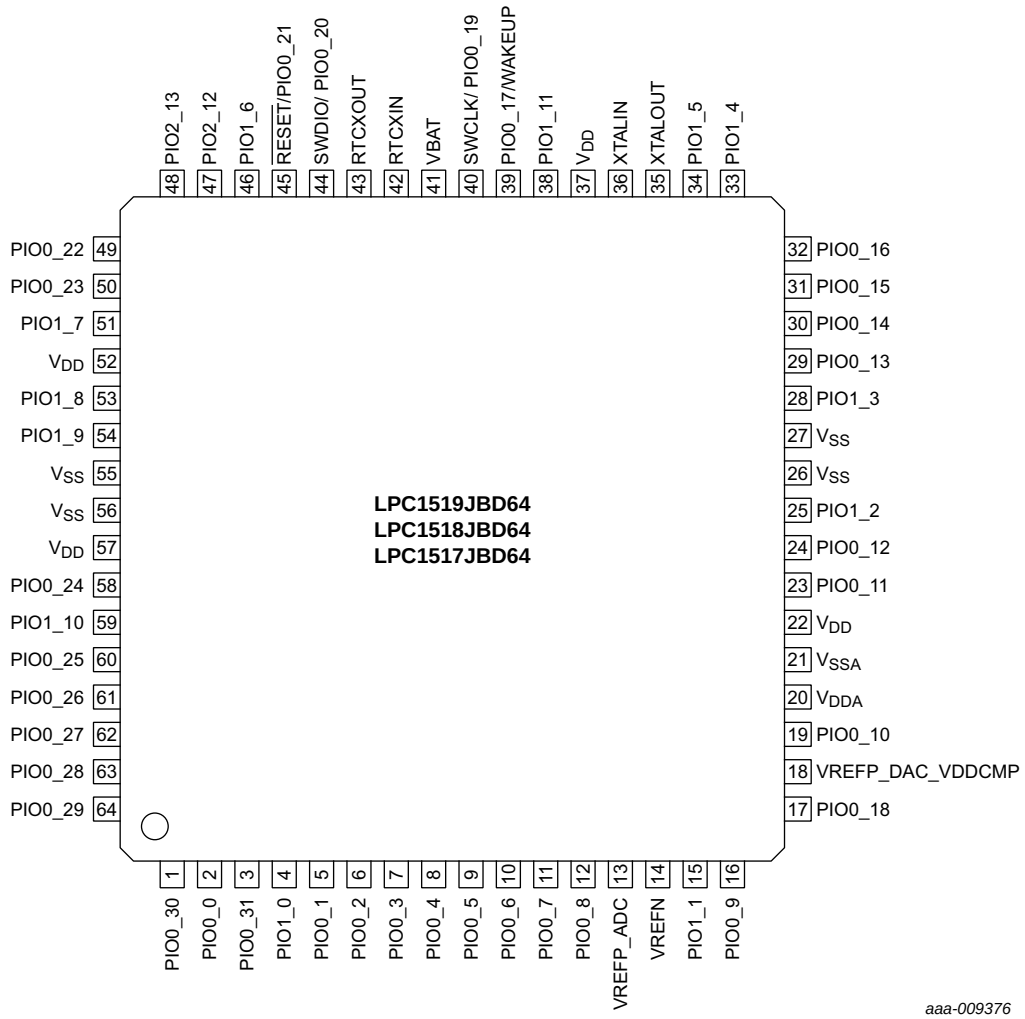


Fig 7. LQFP64 pin configuration (without USB)

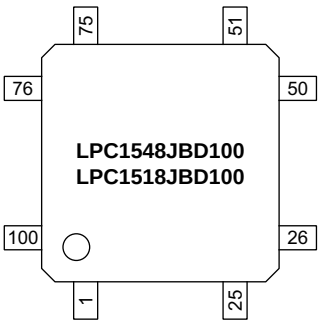


Fig 8. LQFP100 pin configuration

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO2_8	-	-	92	[5]	I; PU	IO	**PIO2_8 —** General purpose port 2 input/output 8. On the LQFP100 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
PIO2_9	-	-	94	[5]	I; PU	IO	**PIO2_9 —** General purpose port 2 input/output 9. On the LQFP100 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
PIO2_10	-	-	96	[5]	I; PU	IO	**PIO2_10 —** General purpose port 2 input/output 10.
PIO2_11	-	-	99	[5]	I; PU	IO	**PIO2_11 —** General purpose port 2 input/output 11.
PIO2_12	35	47	74	[5]	I; PU	IO	**PIO2_12 —** General purpose port 2 input/output 12. On parts LPC1519/17/18 only.
PIO2_13	36	48	75	[5]	I; PU	IO	**PIO2_13 —** General purpose port 2 input/output 13. On parts LPC1519/17/18 only.
USB_DP	35	47	74	[10]	-	IO	USB bidirectional D+ line. Pad includes internal 33 Ω series termination resistor. On parts LPC1549/48/47 only.
USB_DM	36	48	75	[10]	-	IO	USB bidirectional D− line. Pad includes internal 33 Ω series termination resistor. On parts LPC1549/48/47 only.
RTCXIN	31	42	66	[9]	-		RTC oscillator input. This input should be grounded if the RTC is not used.
RTCXOUT	32	43	67	[9]	-		RTC oscillator output.
XTALIN	26	36	54	[9] [11]	-		Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	25	35	53	[9] [11]	-		Output from the oscillator amplifier.
VBAT	30	41	65		-		Battery supply voltage. Supplies power to the RTC. If no battery is used, tie VBAT to VDD or to ground.
V_{DDA}	16	20	30		-		Analog supply voltage. V_{DD} and the analog reference voltages VREFP_ADC and VREFP_DAC_VDDCMP must not exceed the voltage level on V_{DDA}. V_{DDA}should typically be the same voltages as V_{DD} but should be isolated to minimize noise and error. V_{DDA} should be tied to V_{DD} if the ADC is not used.
V_{DD}	39, 27, 42	22, 52, 37, 57	4, 32, 70, 83, 57, 89		-		3.3 V supply voltage (2.4 V to 3.6 V). The voltage level on V_{DD} must be equal or lower than the analog supply voltage V_{DDA}.
VREFP_DAC_VDDCMP	14	18	27	[9]	-		DAC positive reference voltage and analog comparator reference voltage. The voltage level on VREFP_DAC_VDDCMP must be equal to or lower than the voltage applied to V_{DDA}.
VREFN	11	14	22		-		ADC and DAC negative voltage reference. If the ADC is not used, tie VREFN to V_{SS}.

8.4 EEPROM

The LPC15xx contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

8.5 SRAM

The LPC15xx contain a total 36 kB, 20 kB or 12 kB of contiguous, on-chip static RAM memory. For each SRAM configuration, the SRAM is divided into three blocks: 2 x 16 kB + 4 kB for 36 kB SRAM, 2 x 8 kB + 4 kB for 20 kB SRAM, and 2 x 4 kB + 4 kB for 12 kB SRAM. The bottom 16 kB, 8 kB, or 4 kB are enabled by the bootloader and cannot be disabled. The next two SRAM blocks in each configuration can be disabled or enabled individually in the SYSCON block to save power.

Table 8. LPC15xx SRAM configurations

	SRAM0	SRAM1	SRAM2
LPC1549/19 (total SRAM = 36 kB)			
address range	0x0200 0000 to 0x0200 3FFF	0x0200 4000 to 0x0200 7FFF	0x0200 8000 to 0x0200 8FFF
size	16 kB	16 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1548/18 (total SRAM = 20 kB)			
address range	0x0200 0000 to 0x0200 1FFF	0x0200 2000 to 0x0200 3FFF	0x0200 4000 to 0x0200 4FFF
size	8 kB	8 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1547/17 (total SRAM = 12 kB)			
address range	0x0200 0000 to 0x0200 0FFF	0x0200 1000 to 0x0200 1FFF	0x0200 2000 to 0x0200 2FFF
size	4 kB	4 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled

8.6 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Flash updates via USB and C_CAN supported.
- USB API (HID, CDC, and MSC drivers).
- DMA, I2C, USART, SPI, and C_CAN drivers.
- Power profiles for configuring power consumption and PLL settings.

- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Selected events can limit, halt, start, or stop a counter.
- Events control state changes, outputs, interrupts, and DMA requests.
- Match register 0 can be used as an automatic limit.
- In bi-directional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can take place in the state while the counter is running.
  - A state changes into another state as result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- Integrated with an input pre-processing unit (SCTIPU) to combine or delay input events.

Inputs and outputs on the SCTimer2/PWM and SCTimer3/PWM are configured as follows:

- 3 inputs. Each input selects one of 21 sources from a pin multiplexer.
- 6 outputs (some outputs are connected to multiple locations)
  - Three outputs connected to external pins through the switch matrix as movable functions.
  - Three outputs connected to external pins through the switch matrix as fixed-pin functions.
  - Two outputs connected to the SCT IPU to sample or latch input events.
  - Four outputs connected to the accompanying large SCT
  - Two outputs connected to each ADC trigger input

8.22.5 SCT Input processing unit (SCTIPU)

The SCTIPU allows to block or propagate signals to inputs of the SCT under the control of an SCT output. Using the SCTIPU in this way, allows signals to be blocked from entering the SCT inputs for a certain amount of time, for example while they are known to be invalid.

In addition, the SCTIPU can generate a common signal from several combined input sources that can be selected on all SCT inputs. Such a mechanism can be useful to create an abort signal that stops all timers.

8.22.5.1 Features

The SCTIPU pre-processes inputs to the State-Configurable Timers (SCT).

- Four outputs created from a selection of input transitions. Each output can be used as abort input to the SCTs or for any other application which requires a collection of multiple SCT inputs to trigger an identical SCT response.

- When the ADC is accurately calibrated, the internal voltage reference can be used to measure the power supply voltage. This requires calibration by recording the ADC code of the internal voltage reference at different power supply levels yielding a different ADC code value for each supply voltage level. In a particular application, the internal voltage reference can be measured and the actual power supply voltage can be determined from the stored calibration values. The calibration values can be stored in the EEPROM for easy access.

After power-up, the internal voltage reference must be allowed to settle to its stable value before it can be used as an ADC reference voltage input.

For an accurate measurement of the internal voltage reference by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.29 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.29.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

8.30 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.30.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WWDT is clocked by the dedicated watchdog oscillator (WDOsc) running at a fixed frequency.

8.35 Power domains

The LPC15xx provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power (V_{DD}) is used to operate the RTC whenever V_{DD} is present. Therefore, there is no power drain from the RTC battery when V_{DD} is and V_{DD} >= VBAT + 0.3 V.

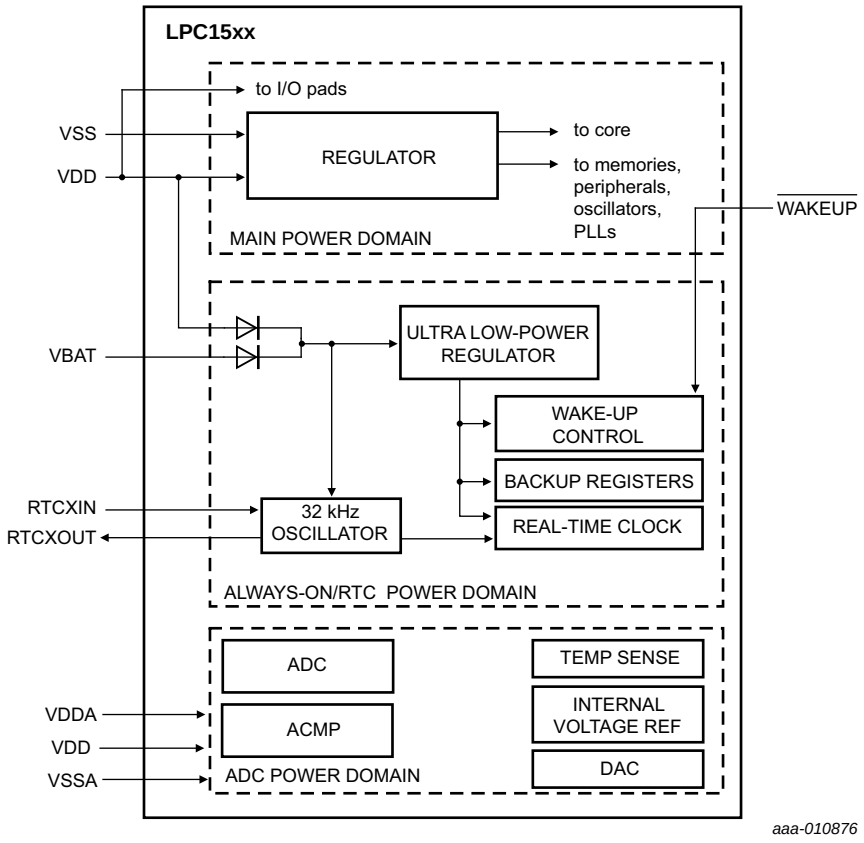


Fig 15. Power distribution

8.36 Integrated oscillators

The LPC15xx include the following independent oscillators: the system oscillator, the Internal RC oscillator (IRC), the watchdog oscillator, and the 32 kHz RTC oscillator. Each oscillator can be used for multiple purposes.

Following reset, the LPC15xx operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 14 for an overview of the LPC15xx clock generation.

8.38 Clock output

The LPC15xx feature a clock output function that routes the internal oscillator outputs, the PLL outputs, or the main clock an output pin where they can be observed directly.

8.39 Wake-up process

The LPC15xx begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the system oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and system oscillator as a clock source.

8.40 Power control

The LPC15xx support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides additional power control.

8.40.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC15xx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock and to easily set the configuration options for Deep-sleep and power-down modes.

Remark: When using the USB, configure the LPC15xx in Default mode.

8.40.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

In addition, ISP entry the external pins can be disabled without enabling CRP. For details, see the LPC15xx *user manual*.

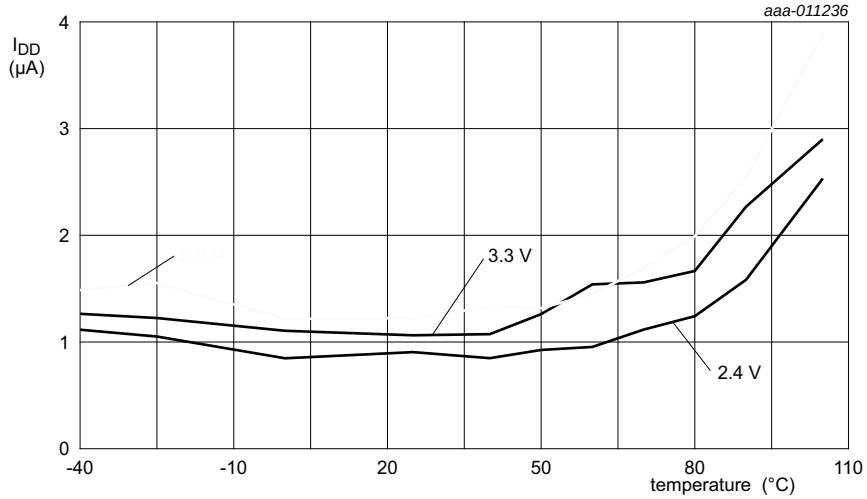
There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using ISP pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

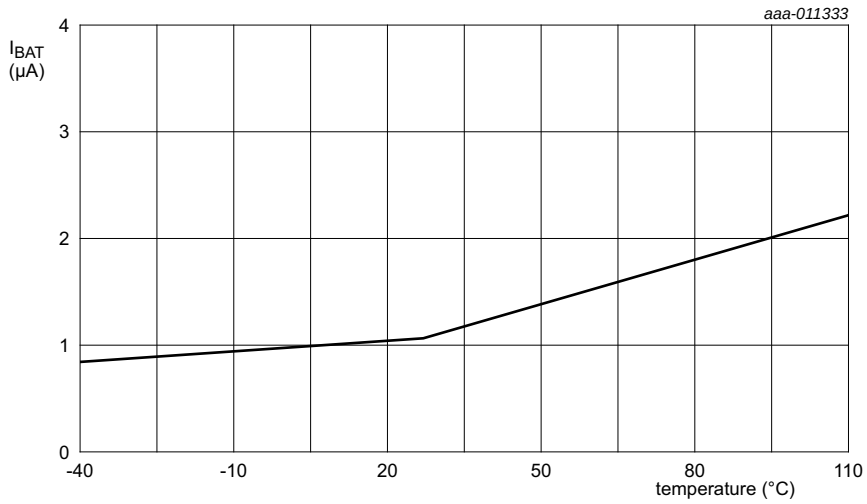
If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP pins for valid user code can be disabled. For details, see the LPC15xx *user manual*.



VBAT = 0 V.

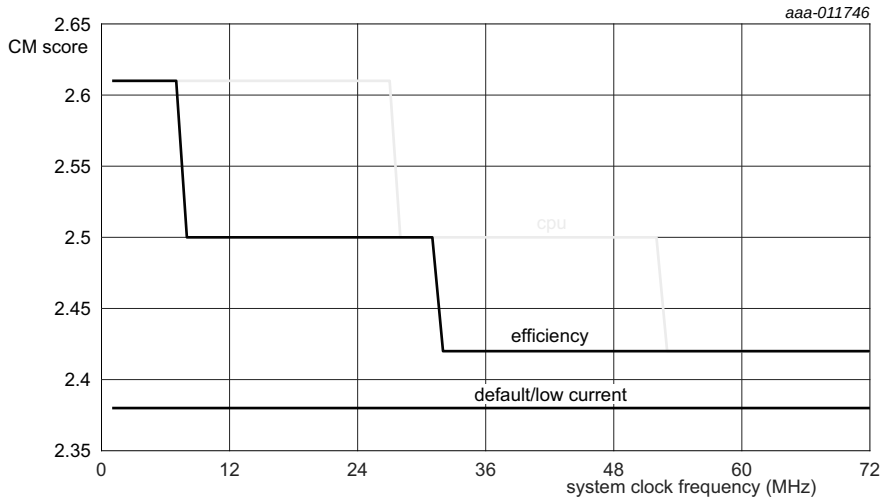
Fig 23. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



VBAT = 3.3 V; V_{DD} floating.

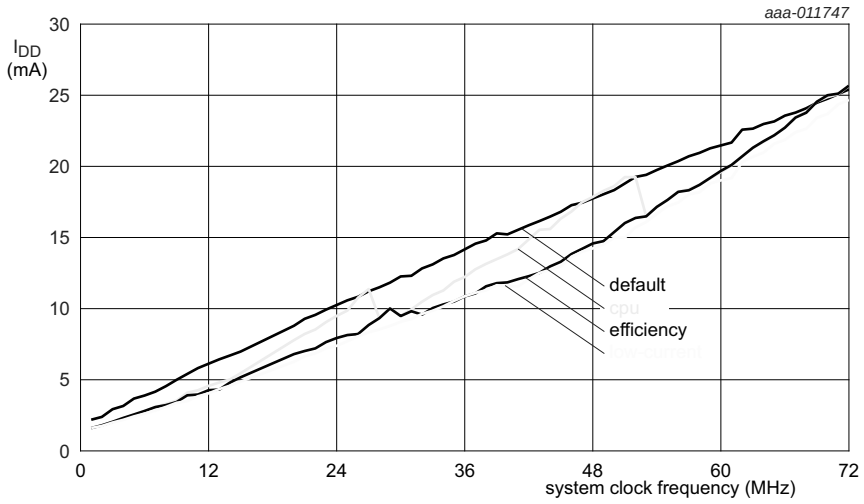
Fig 24. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

11.2 CoreMark data



Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL0/1 register; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.73.0.0, C compiler v.5.03.0.76.

Fig 25. CoreMark score



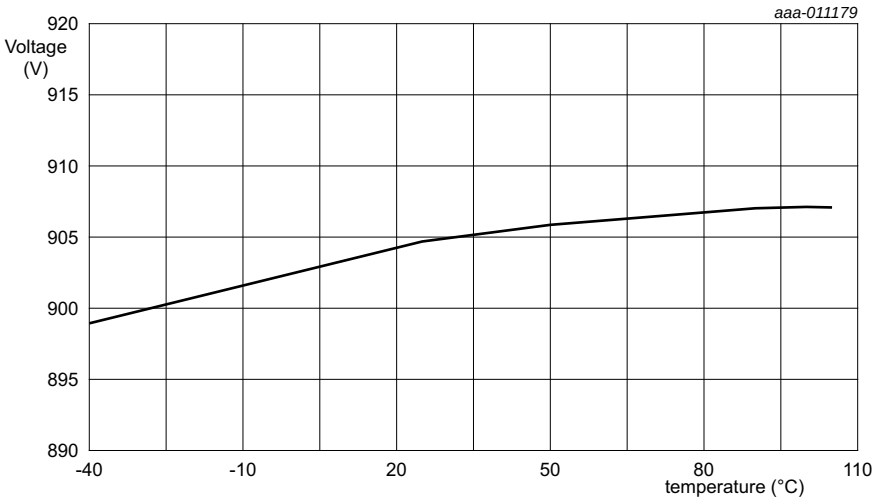
Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL0/1 registers; system clock derived from the IRC; system oscillator disabled; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.73.0.0, C compiler v.5.03.0.76.

Fig 26. Active mode: CoreMark power consumption I_{DD}

Table 26. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = −40 °C to +105 °C [1]	875	-	925	mV
		T_{amb} = 25 °C		905		mV
$t_{s(pu)}$	power-up settling time	to 99% of V_O	-	-	125	µs

[1] Maximum and minimum values are measured on samples from the corners of the process matrix lot.



V_{DDA} = 3.3 V; averaged over process corners

Fig 42. Average internal voltage reference output voltage

Table 27. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C [1]	-	-	5	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C	-	-	5	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value [2][3]	-	81	110	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models). Maximum values are derived from worst case simulation (V_{DDA} = 2.6 V; T_{amb} = 105 °C; slow process models).

[3] Internal voltage reference must be powered before the temperature sensor can be turned on.

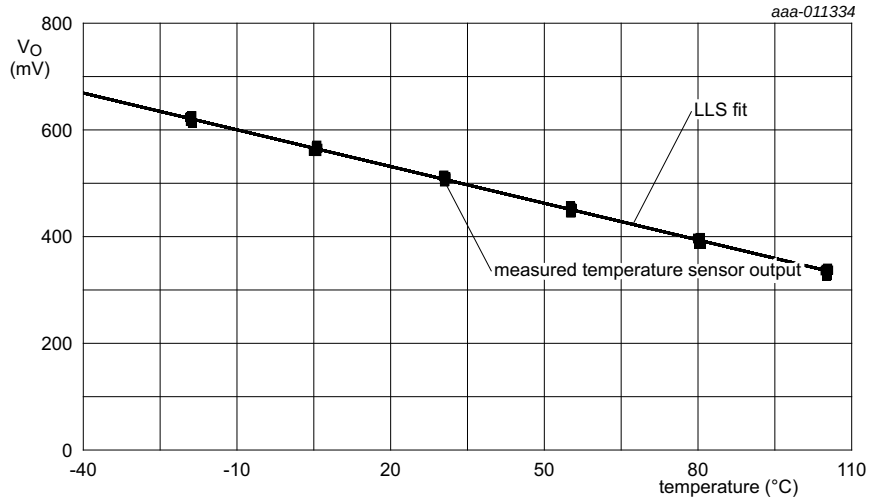
[4] Settling time applies to switching between comparator and ADC channels.

Table 28. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range	Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C [1]	-	-2.29	-	mV/°C
LLS intercept at 0 °C	T_{amb} = −40 °C to +105 °C [1]	-	577.3	-	mV
Value at 30 °C	[2]	502	-	514	mV

[1] Measured over matrix samples.

[2] Measured for samples over process corners.



V_{DDA} = 3.3 V; measured on matrix samples.

Fig 43. LLS fit of the temperature sensor output voltage

Table 29. Comparator characteristics

V_{DDA} = 3.0 V. DLY = 0x0 in the analog comparator CTRL register for shortest propagation delay setting. See the LPC15xx user manual UM10736.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{DD}	supply current	VP > VM	-	48	-	μA
		VM > VP	-	38	-	μA
V_{IC}	common-mode input voltage		0	-	V_{DDA}	V
DV_O	output voltage variation		0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V	-	+/- 3	-	mV
		V_{IC} = 1.5 V	-	+/- 3	-	mV
		V_{IC} = 2.9 V	-	+/- 6	-	mV
Dynamic characteristics						
$t_{startup}$	start-up time	nominal process	-	4.5	6	μs
t_{PD}	propagation delay	HIGH to LOW; V_{DDA} = 3.0 V;				
		V_{IC} = 0.1 V; 50 mV overdrive input [1]	-	86	130	ns
		V_{IC} = 0.1 V; rail-to-rail input [1]	-	196	250	ns
		V_{IC} = 1.5 V; 50 mV overdrive input [1]	-	68	110	ns
		V_{IC} = 1.5 V; rail-to-rail input [1]	-	64	90	ns
		V_{IC} = 2.9 V; 50 mV overdrive input [1]	-	86	130	ns
		V_{IC} = 2.9 V; rail-to-rail input [1]	-	48	80	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DDA} = 3.0 V;				
		V_{IC} = 0.1 V; 50 mV overdrive input [1]	-	98	130	ns
		V_{IC} = 0.1 V; rail-to-rail input [1]	-	24	40	ns
		V_{IC} = 1.5 V; 50 mV overdrive input [1]	-	88	130	ns
		V_{IC} = 1.5 V; rail-to-rail input [1]	-	68	120	ns
		V_{IC} = 2.9 V; 50 mV overdrive input [1]	-	84	110	ns
		V_{IC} = 2.9 V; rail-to-rail input [1]	-	98	180	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V; settings: [2]				
		5 mV	3	-	8	mV
		10 mV	8	-	13	mV
		15 mV	17	-	25	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V; settings: [1][2]				
		5 mV	3	-	9	mV
		10 mV	8	-	18	mV
		15 mV	18	-	27	mV
R_{lad}	ladder resistance	-	-	1	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +105 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

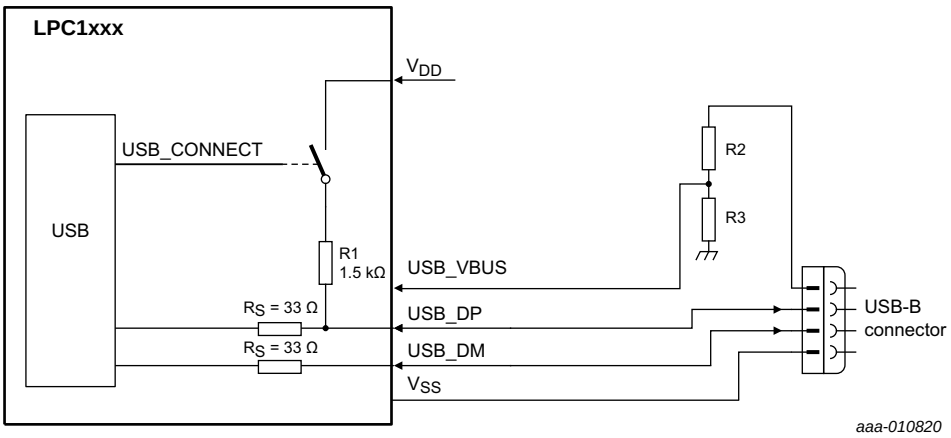


Fig 44. USB interface on a self-powered device where USB_VBUS = 5 V

For a bus-powered device, the VBUS signal does not need to be connected to the USB_VBUS pin (see Figure 45). The USB_CONNECT function can additionally be enabled internally by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required for the USB_CONNECT functionality.

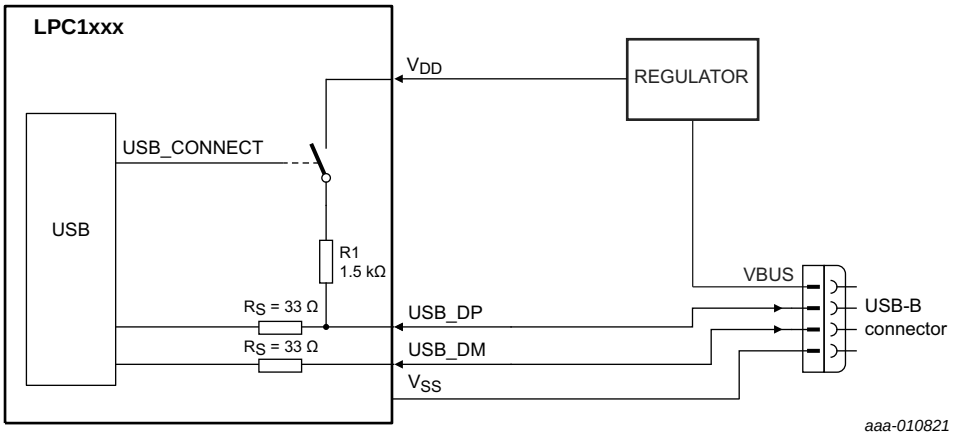


Fig 45. USB interface on a bus-powered device

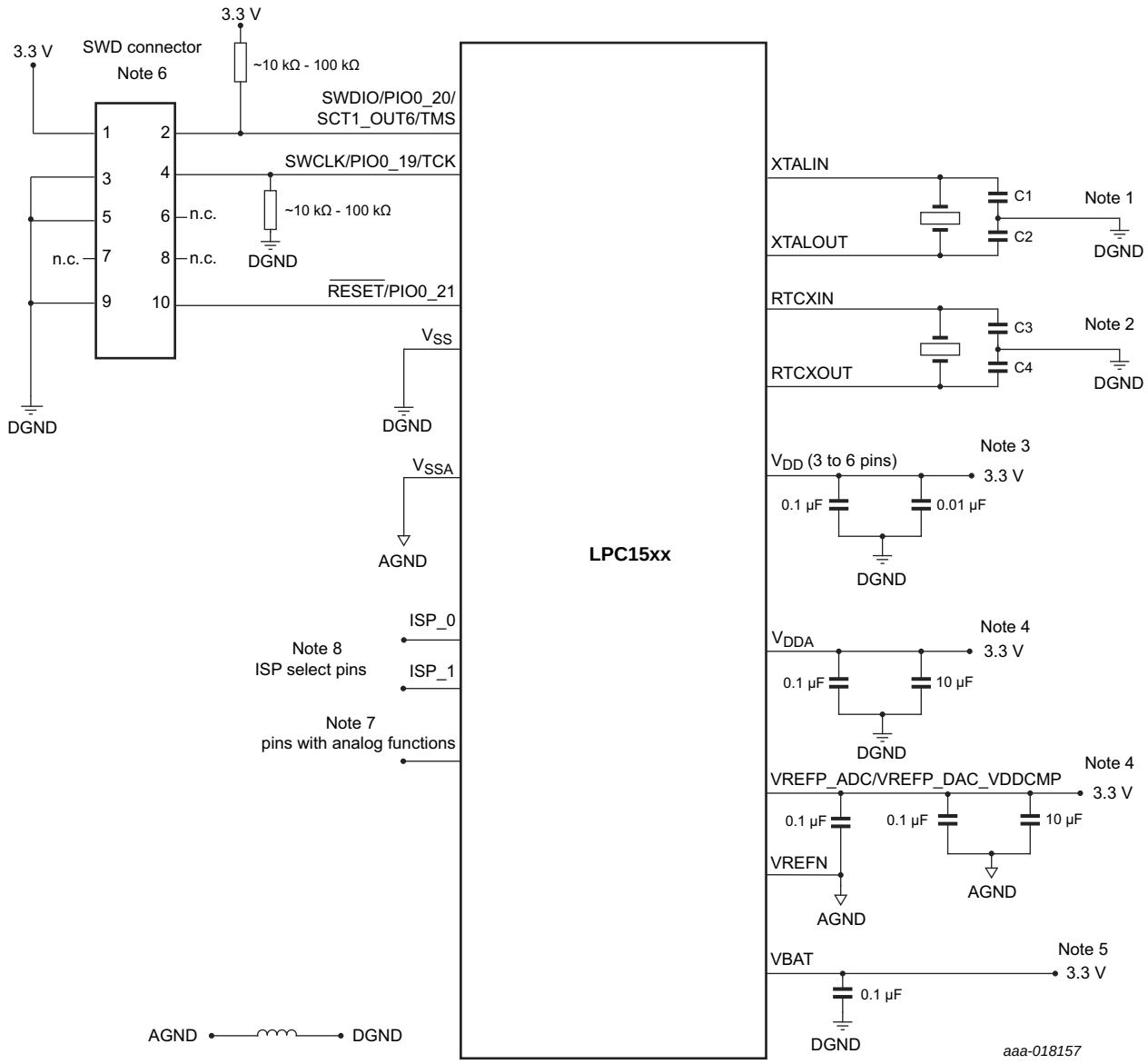
Remark: When a bus-powered circuit as shown in Figure 45 is used or, for a self-powered device, when the VBUS pin is not connected, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) in the IOCON block. This ties the VBUS signal HIGH internally.

14.2.1 USB Low-speed operation

The USB device controller can be used in low-speed mode supporting 1.5 Mbit/s data exchange with a USB host controller.

Remark: To operate in low-speed mode, change the board connections as follows:

1. Connect USB_DP to the D- pin of the connector.
2. Connect USB_DM to the D+ pin of the connector.



(1) See Section 14.3 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.5 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(8) ISP pin assignments is dependent on package type. See Table 7 “Pin assignments for ISP modes”.

Fig 49. Power, clock, and debug connections

14.7 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as GPIO (switch matrix default) and setto outputs driving LOW with their internal pull-up disabled. To drive the output LOW, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

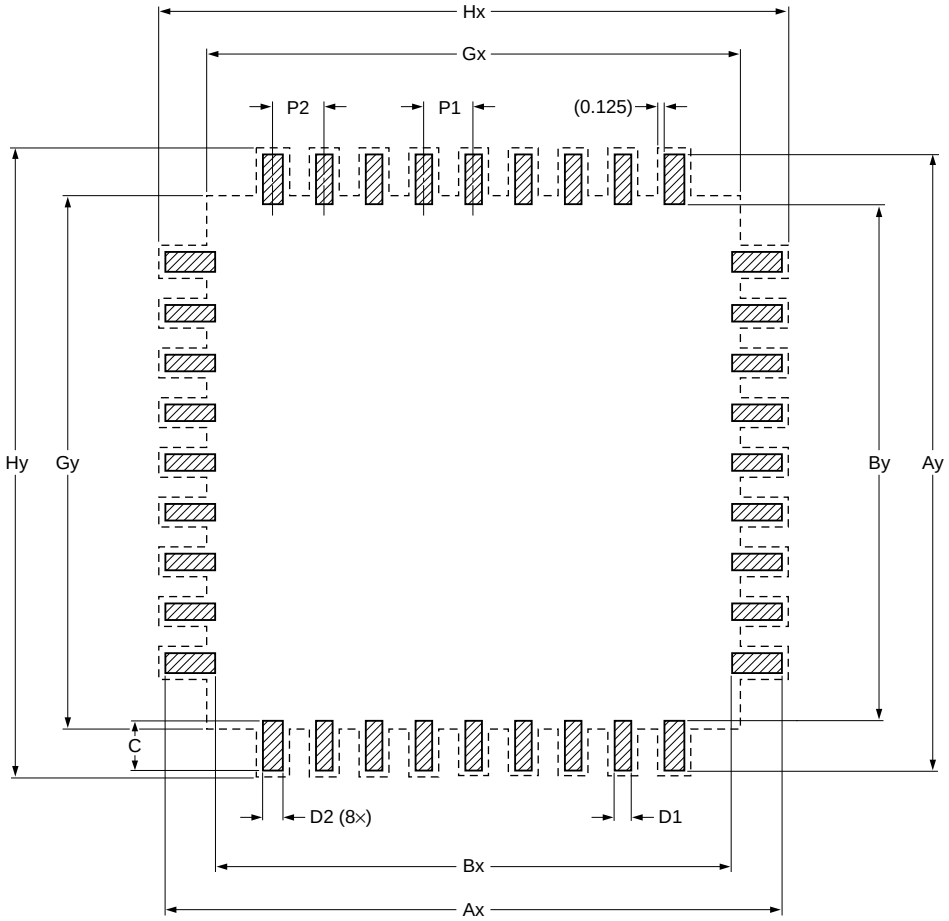
In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_21	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether Deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
USB_DP/USB_DM	F	Can be left unconnected. When the USP PHY is disabled, the pins are LOW.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP_DAC_VDDCMP	-	Tie to VDD.
VREFP_ADC		Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VBAT	-	Tie to VDD if no external battery connected.
VSSA	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 54. Reflow soldering for the LQFP64 package

17. References

[1] LPC15xx User manual UM10736:
http://www.nxp.com/documents/user_manual/UM10736.pdf

[2] LPC15xx Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC15XX.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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