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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	44
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1549jbd64ql

- Analog peripherals:
  - Two 12-bit ADC with up to 12 input channels per ADC and with multiple internal and external trigger inputs and sample rates of up to 2 Msamples/s. Each ADC supports two independent conversion sequences. ADC conversion clock can be the system clock or an asynchronous clock derived from one of the three PLLs.
  - One 12-bit DAC.
  - Integrated temperature sensor and band gap internal reference voltage.
  - Four comparators with external and internal voltage references (ACMP0 to 3). Comparator outputs are internally connected to the SCTimer/PWMs and ADCs and externally to pins. Each comparator output contains a programmable glitch filter.
- Serial interfaces:
  - Three USART interfaces with DMA, RS-485 support, autobaud, and with synchronous mode and 32 kHz mode for wake-up from Deep-sleep and Power-down modes. The USARTs share a fractional baud-rate generator.
  - Two SPI controllers.
  - One I^2C-bus interface supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode.
  - One C_CAN controller.
  - One USB 2.0 full-speed device controller with on-chip PHY.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Watchdog oscillator with a frequency range of 503 kHz.
  - 32 kHz low-power RTC oscillator with 32 kHz, 1 kHz, and 1 Hz outputs.
  - System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Two additional PLLs for generating the USB and SCTimer/PWM clocks.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - APIs provided for optimizing power consumption in active and sleep modes and for configuring Deep-sleep, Power-down, and Deep power-down modes.
  - Wake-up from Deep-sleep and Power-down modes on activity on USB, USART, SPI, and I2C peripherals.
  - Wake-up from Sleep, Deep-sleep, Power-down, and Deep power-down modes from the RTC alarm or wake-up interrupts.
  - Timer-controlled self wake-up from Deep power-down mode using the RTC high-resolution/wake-up 1 kHz timer.
  - Power-On Reset (POR).
  - BrownOut Detect BOD).
- JTAG boundary scan modes supported.
- Unique device serial number for identification.

- Single power supply 2.4 V to 3.6 V.
- Temperature range −40 °C to +105 °C.
- Available as LQFP100, LQFP64, and LQFP48 packages.

3. Applications

- Motor control
- Motion drives
- Digital power supplies
- Industrial and medical
- Solar inverters
- Home appliances
- Building and factory automation

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1549JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1549JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1549JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1548JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1548JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1519JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1519JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1518JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1518JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5. Marking

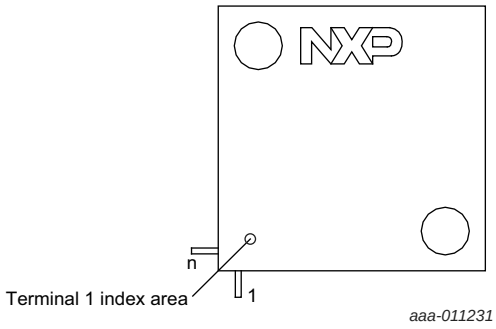


Fig 1. LQFP64/100 package marking

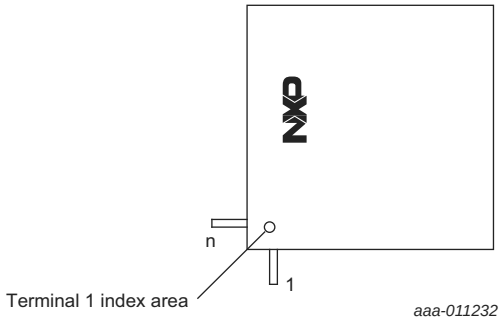


Fig 2. LQFP48 package marking

The LPC15xx devices typically have the following top-side marking for LQFP100 packages:

LPC15xxJxxx
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP64 packages:

LPC15xxJ
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP48 packages:

LPC15xxJ
Xxxxxx
Xxxyy
wwxxx

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

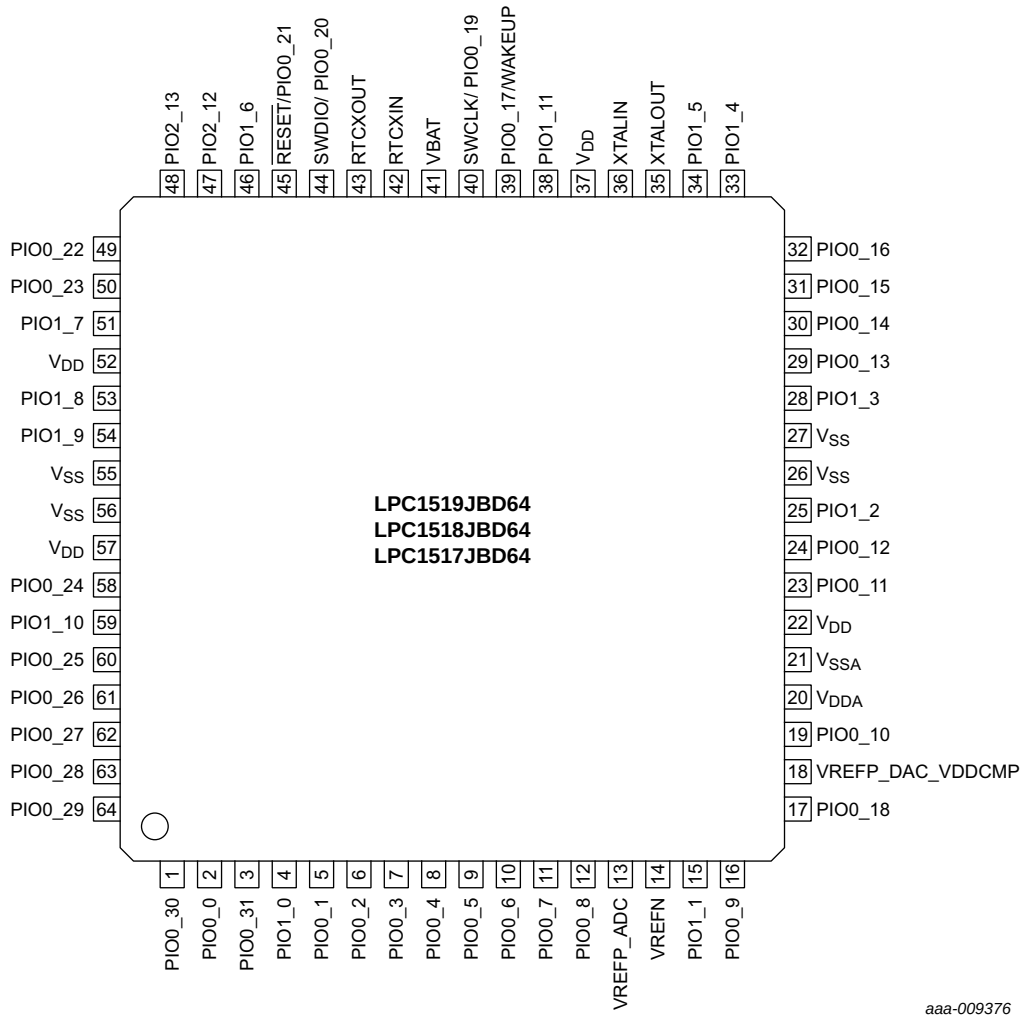


Fig 7. LQFP64 pin configuration (without USB)

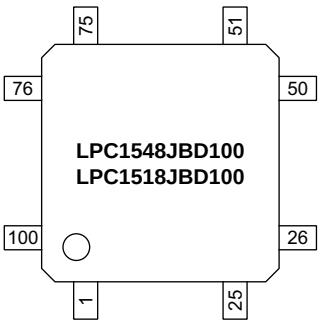


Fig 8. LQFP100 pin configuration

7.2 Pin description

Most pins are configurable for multiple functions, which can be analog or digital. Digital inputs can be connected to several peripherals at once, however only one digital output or one analog function can be assigned to any on pin. The pin's connections to internal peripheral blocks are configured by the switch matrix (SWM), the input multiplexer (INPUT MUX), and the SCT Input Pre-processor Unit (SCTIPU).

The switch matrix enables certain fixed-pin functions that can only reside on specific pins (see Table 3) and assigns all other pin functions (movable functions) to any available pin (see Table 4), so that the pinout can be optimized for a given application.

The input multiplexer provides many choices (pins and internal signals) for selecting the inputs of the SCTimer/PWMs and the frequency measure block. Pins that are connected to the input multiplexer are listed in Table 5. If a pin is selected in the input multiplexer, it is directly connected to the peripheral input without being routed through the switch matrix. Independently of being selected in the input multiplexer, the same pin can also be assigned by the switch matrix to another peripheral input.

Four pins can also be connected directly to the SCTIPU and at the same time be inputs to the input multiplexer and the switch matrix (see Table 5).

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_0/ADC0_10/ SCT0_OUT3	1	2	2	[2]	I; PU	IO	**PIO0_0 —** General purpose port 0 input/output 0.
						A	**ADC0_10 —** ADC0 input 10.
						O	**SCT0_OUT3 —** SCTimer0/PWM output 3.
PIO0_1/ADC0_7/ SCT0_OUT4	2	5	6	[2]	I; PU	IO	**PIO0_1 —** General purpose port 0 input/output 1.
						A	**ADC0_7 —** ADC0 input 7.
						O	**SCT0_OUT4 —** SCTimer0/PWM output 4.
PIO0_2/ADC0_6/ SCT1_OUT3	3	6	8	[2]	I; PU	IO	**PIO0_2 —** General purpose port 0 input/output 2.
							ADC0_6 — ADC0 input 6.
						O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO0_3/ADC0_5/ SCT1_OUT4	4	7	10	[2]	I; PU	IO	**PIO0_3 —** General purpose port 0 input/output 3.
						A	**ADC0_5 —** ADC0 input 5.
						O	**SCT1_OUT4 —** SCTimer1/PWM output 4.
PIO0_4/ADC0_4	5	8	13	[2]	I; PU	IO	**PIO0_4 —** General purpose port 0 input/output 4. This is the ISP_0 boot pin for the LQFP48 package.
						A	**ADC0_4 —** ADC0 input 4.
PIO0_5/ADC0_3	6	9	14	[2]	I; PU	IO	**PIO0_5 —** General purpose port 0 input/output 5.
						A	**ADC0_3 —** ADC0 input 3.
PIO0_6/ADC0_2/ SCT2_OUT3	7	10	16	[2]	I; PU	IO	**PIO0_6 —** General purpose port 0 input/output 6.
						A	**ADC0_2 —** ADC0 input 2.
						O	**SCT2_OUT3 —** SCTimer2/PWM output 3.
PIO0_7/ADC0_1	8	11	17	[2]	I; PU	IO	**PIO0_7 —** General purpose port 0 input/output 7.
						A	**ADC0_1 —** ADC0 input 1.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_8/ADC0_0/TDO	9	12	19	[2]	I; PU	IO	**PIO0_8 —** General purpose port 0 input/output 8. In boundary scan mode: TDO (Test Data Out).
						A	**ADC0_0 —** ADC0 input 0.
PIO0_9/ADC1_1/TDI	12	16	24	[2]	I; PU	IO	**PIO0_9 —** General purpose port 0 input/output 9. In boundary scan mode: TDI (Test Data In).
						A	**ADC1_1 —** ADC1 input 1.
PIO0_10/ADC1_2	15	19	28	[2]	I; PU	IO	**PIO0_10 —** General purpose port 0 input/output 10.
						A	**ADC1_2 —** ADC1 input 2.
PIO0_11/ADC1_3	18	23	33	[2]	I; PU	IO	**PIO0_11 —** General purpose port 0 input/output 11. On the LQFP64 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_3 —** ADC1 input 3.
PIO0_12/DAC_OUT	19	24	35	[3]	I; PU	IO	**PIO0_12 —** General purpose port 0 input/output 12. If this pin is configured as a digital input, the input voltage level must not be higher than V_{DDA}.
						A	**DAC_OUT —** DAC analog output.
PIO0_13/ADC1_6	21	29	43	[2]	I; PU	IO	**PIO0_13 —** General purpose port 0 input/output 13. On the LQFP64 package, this pin is assigned to U0_RXD in ISP USART mode. On the LQFP48 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_6 —** ADC1 input 6.
PIO0_14/ADC1_7/ SCT1_OUT5	22	30	45	[2]	I; PU	IO	**PIO0_14 —** General purpose port 0 input/output 14. On the LQFP48 package, this pin is assigned to U0_RXD in ISP USART mode.
						A	**ADC1_7 —** ADC1 input 7.
						O	**SCT1_OUT5 —** SCTimer1/PWM output 5.
PIO0_15/ADC1_8	23	31	47	[2]	I; PU	IO	**PIO0_15 —** General purpose port 0 input/output 15. On the LQFP48 package, this pin is assigned to U0_TXD in ISP USART mode.
						A	**ADC1_8 —** ADC1 input 8.
PIO0_16/ADC1_9	24	32	49	[2]	I; PU	IO	**PIO0_16 —** General purpose port 0 input/output 16. On the LQFP48 package, this is the ISP_1 boot pin.
						A	**ADC1_9 —** ADC1 input 9.
PIO0_17/WAKEUP/ $\overline{\text{TRST}}$	28	39	61	[4]	I; PU	IO	**PIO0_17 —** General purpose port 0 input/output 17. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. For wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. Pull this pin HIGH externally while in Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO1_12	-	-	9	[5]	I; PU	IO	**PIO1_12 —** General purpose port 1 input/output 12.
PIO1_13	-	-	11	[5]	I; PU	IO	**PIO1_13 —** General purpose port 1 input/output 13.
PIO1_14/SCT0_OUT7	-	-	12	[5]	I; PU	IO	**PIO1_14 —** General purpose port 1 input/output 14.
						O	**SCT0_OUT7 —** SCTimer0/PWM output 7.
PIO1_15	-	-	15	[5]	I; PU	IO	**PIO1_15 —** General purpose port 1 input/output 15.
PIO1_16	-	-	18	[5]	I; PU	IO	**PIO1_16 —** General purpose port 1 input/output 16.
PIO1_17/SCT1_OUT7	-	-	20	[5]	I; PU	IO	**PIO1_17 —** General purpose port 1 input/output 17.
						O	**SCT1_OUT7 —** SCTimer1/PWM output 7.
PIO1_18	-	-	25	[5]	I; PU	IO	**PIO1_18 —** General purpose port 1 input/output 18.
PIO1_19	-	-	29	[5]	I; PU	IO	**PIO1_19 —** General purpose port 1 input/output 19.
PIO1_20/SCT2_OUT5	-	-	34	[5]	I; PU	IO	**PIO1_20 —** General purpose port 1 input/output 20.
						O	**SCT2_OUT5 —** SCTimer2/PWM output 5.
PIO1_21	-	-	37	[5]	I; PU	IO	**PIO1_21 —** General purpose port 1 input/output 21.
PIO1_22	-	-	38	[5]	I; PU	IO	**PIO1_22 —** General purpose port 1 input/output 22.
PIO1_23	-	-	42	[5]	I; PU	IO	**PIO1_23 —** General purpose port 1 input/output 23.
PIO1_24/SCT3_OUT5	-	-	44	[5]	I; PU	IO	**PIO1_24 —** General purpose port 1 input/output 24.
						O	**SCT3_OUT5 —** SCTimer3/PWM output 5.
PIO1_25	-	-	46	[5]	I; PU	IO	**PIO1_25 —** General purpose port 1 input/output 25.
PIO1_26	-	-	48	[5]	I; PU	IO	**PIO1_26 —** General purpose port 1 input/output 26.
PIO1_27	-	-	50	[5]	I; PU	IO	**PIO1_27 —** General purpose port 1 input/output 27.
PIO1_28	-	-	55	[5]	I; PU	IO	**PIO1_28 —** General purpose port 1 input/output 28.
PIO1_29	-	-	56	[5]	I; PU	IO	**PIO1_29 —** General purpose port 1 input/output 29.
PIO1_30	-	-	59	[5]	I; PU	IO	**PIO1_30 —** General purpose port 1 input/output 30.
PIO1_31	-	-	60	[5]	I; PU	IO	**PIO1_31 —** General purpose port 1 input/output 31.
PIO2_0	-	-	62	[5]	I; PU	IO	**PIO2_0 —** General purpose port 2 input/output 0.
PIO2_1	-	-	64	[5]	I; PU	IO	**PIO2_1 —** General purpose port 2 input/output 1.
PIO2_2	-	-	72	[5]	I; PU	IO	**PIO2_2 —** General purpose port 2 input/output 2.
PIO2_3	-	-	76	[5]	I; PU	IO	**PIO2_3 —** General purpose port 2 input/output 3.
PIO2_4	-	-	77	[5]	I; PU	IO	**PIO2_4 —** General purpose port 2 input/output 4. On the LQFP100 package, this is the ISP_1 boot pin.
PIO2_5	-	-	80	[5]	I; PU	IO	**PIO2_5 —** General purpose port 2 input/output 5. On the LQFP100 package, this is the ISP_0 boot pin.
PIO2_6	-	-	82	[5]	I; PU	IO	**PIO2_6 —** General purpose port 2 input/output 6. On the LQFP100 package, this pin is assigned to U0_TXD in ISP USART mode.
PIO2_7	-	-	86	[5]	I; PU	IO	**PIO2_7 —** General purpose port 2 input/output 7. On the LQFP100 package, this pin is assigned to U0_RXD in ISP USART mode.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
VREFP_ADC	10	13	21		-		ADC positive reference voltage. The voltage level on VREFP_ADC must be equal to or lower than the voltage applied to V_{DDA}. If the ADC is not used, tie VREFP_ADC to V_{DD}.
V_{SSA}	17	21	31		-		Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	41, 20, 40	56, 26, 27, 55	88, 7, 39, 40, 68, 87		-		Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[3] This pin is not 5 V tolerant due to special analog functionality. When configured for a digital function, this pin is 3 V tolerant and provides standard digital I/O functions with configurable internal pull-up and pull-down resistors and hysteresis. When configured for DAC_OUT, the digital section of the pin is disabled and this pin is a 3 V tolerant analog output. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, and configurable hysteresis. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on. This pin is powered in deep power-down mode and can wake up the part. The wake-up pin function can be disabled and the pin can be used for other purposes, if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[9] Special analog pin.

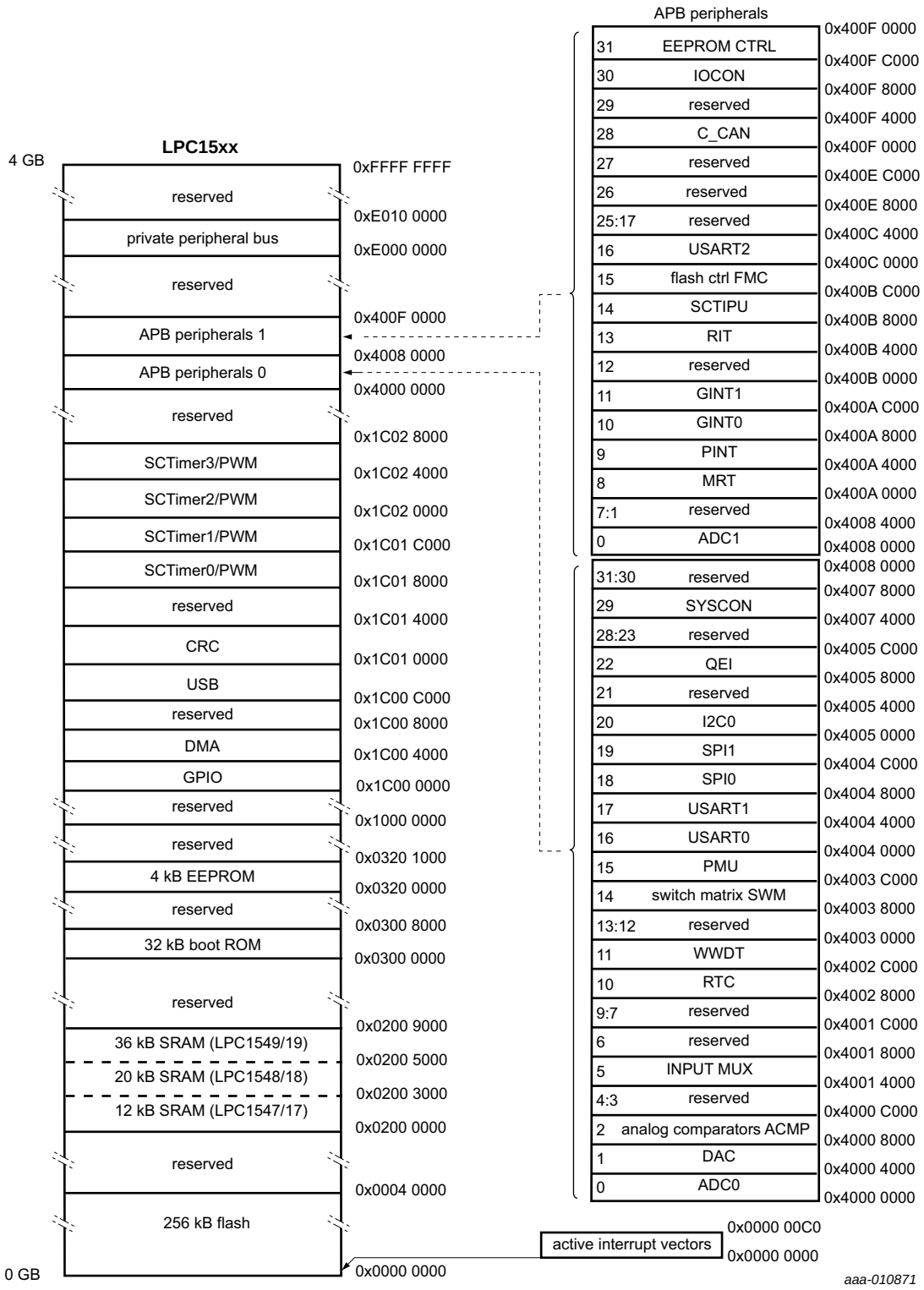
[10] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[11] When the main oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. Movable functions

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.

8.8 Memory map



See Section 8.5 “SRAM” for SRAM configuration.

Fig 10. Memory map

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter configurable on all pins
- Digital input: Input glitch filter enabled/disabled on select pins
- Analog input

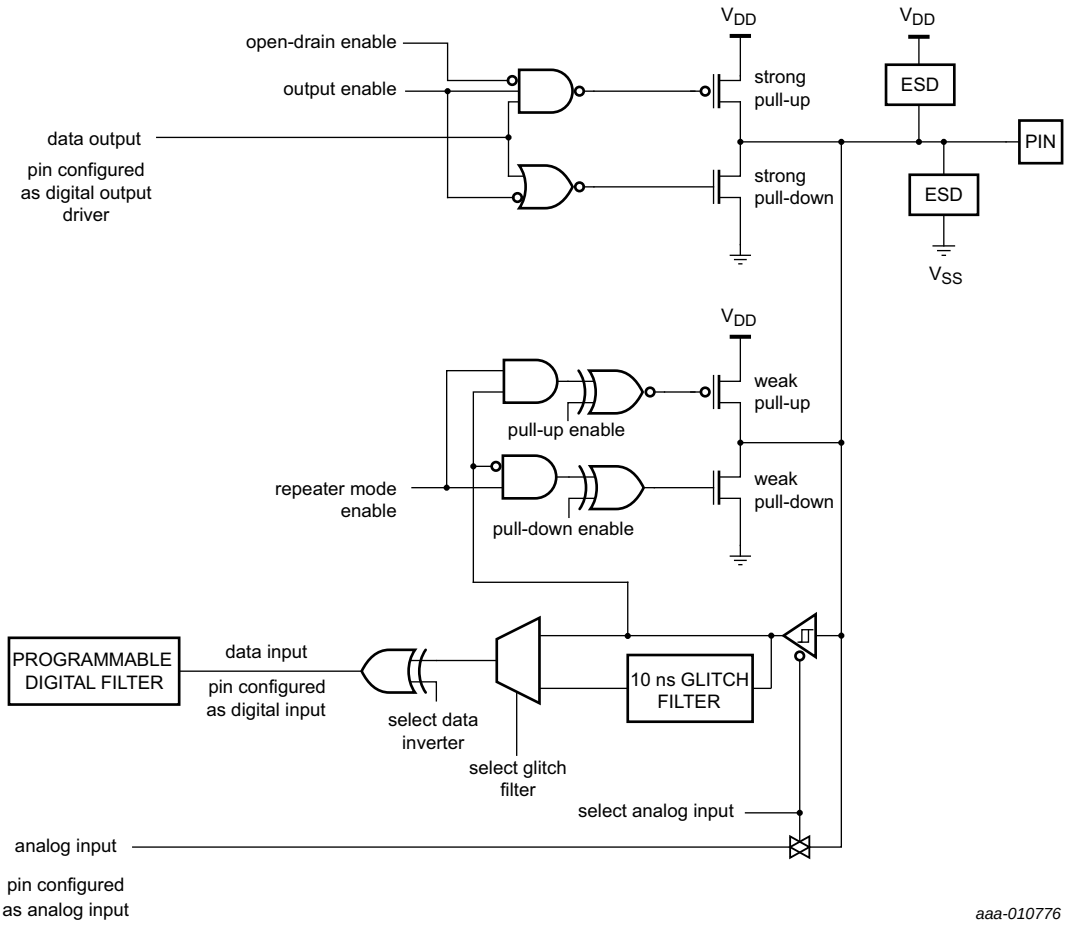


Fig 11. Standard I/O pin configuration

8.11 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the ADC or analog comparator inputs can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.21 C_CAN

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller can build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

The C_CAN functions are movable functions and are assigned to pins through the switch matrix. Do not connect C_CAN functions to the open-drain pins PIO0_22 and PIO0_23.

8.21.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

8.22 PWM/timer/motor control subsystem

The SCTimer/PWMs (State Configurable Timer/Pulse Width Modulators) and the analog peripherals support multiple ways of interconnecting their inputs and outputs and of interfacing to the pins and the DMA controller. Using the highly flexible and programmable connection scheme makes it easy to configure various subsystems for motor control and complex timing and tracking applications. Specifically, the inputs to the SCTs and the trigger inputs of the ADCs and DMA are selected through the input multiplexer which offers a choice of many possible sources for each input or trigger. SCT outputs are assigned to pins through the switch matrix allowing for many pinout solutions.

8.22.1 SCtimer/PWM subsystem

The SCTimer/PWMs can be configured to build a PWM controller with multiple outputs by programming the MATCH and MATCHRELOAD registers to control the base frequency and the duty cycle of each SCTimer/PWM output. More complex waveforms that span multiple counter cycles or change behavior across or within counter cycles can be generated using the state capability built into the SCTimer/PWMs.

Combining the PWM functions with the analog functions, the PWM output can react to control signals like comparator outputs or the ADC interrupts. The SCT IPU adds emergency shut-down functions and pre-processing of controlling events. For an overview of the PWM subsystem, see Figure 12 “PWM-Analog subsystem”.

For high-speed PWM functionality, use only outputs that are fixed-pin functions to minimize pin-to-pin differences in output skew. See also Table 22 “SCTimer/PWM output dynamic characteristics”. This reduces the number of PWM outputs to five for each large SCT.

8.35 Power domains

The LPC15xx provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power (V_{DD}) is used to operate the RTC whenever V_{DD} is present. Therefore, there is no power drain from the RTC battery when V_{DD} is and V_{DD} >= VBAT + 0.3 V.

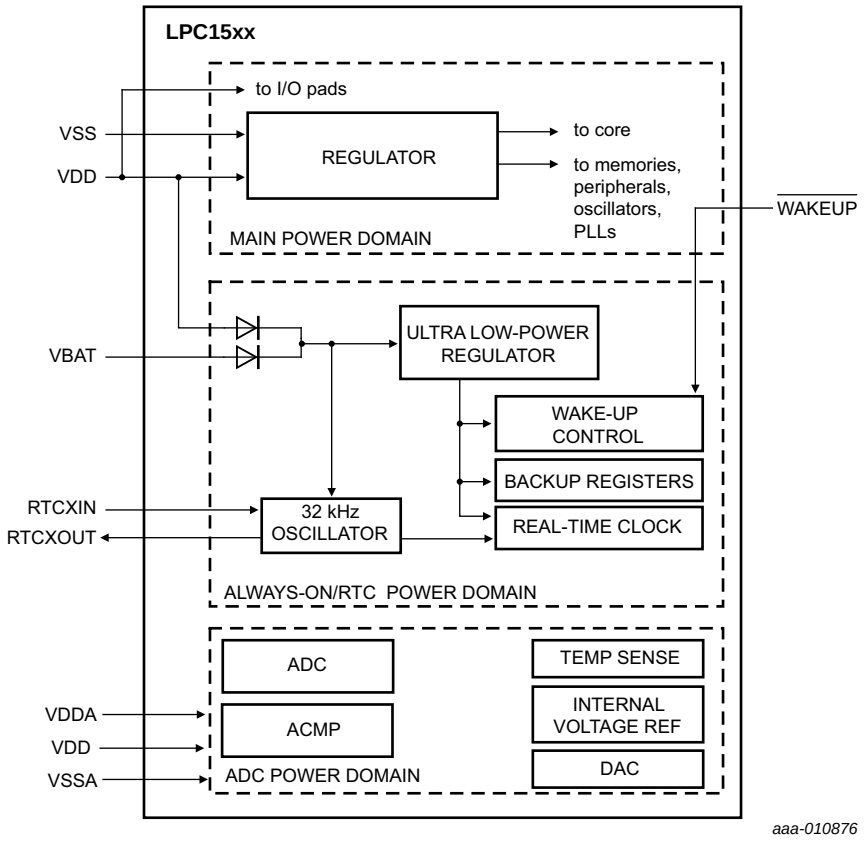


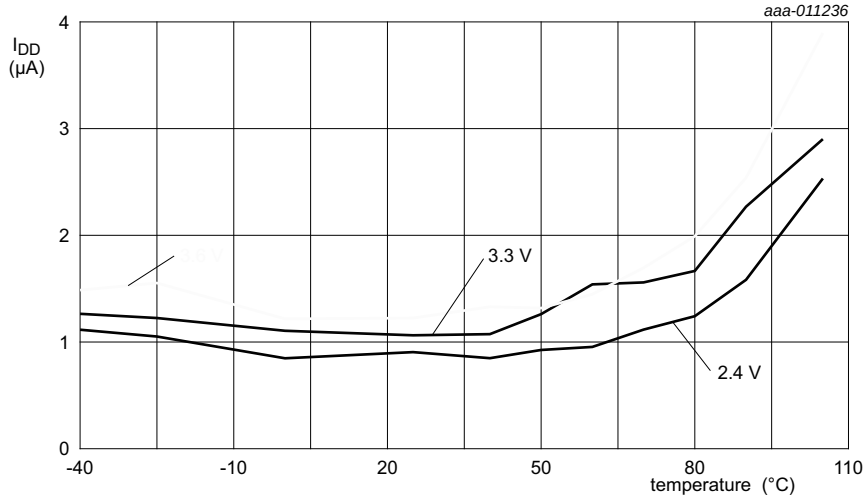
Fig 15. Power distribution

8.36 Integrated oscillators

The LPC15xx include the following independent oscillators: the system oscillator, the Internal RC oscillator (IRC), the watchdog oscillator, and the 32 kHz RTC oscillator. Each oscillator can be used for multiple purposes.

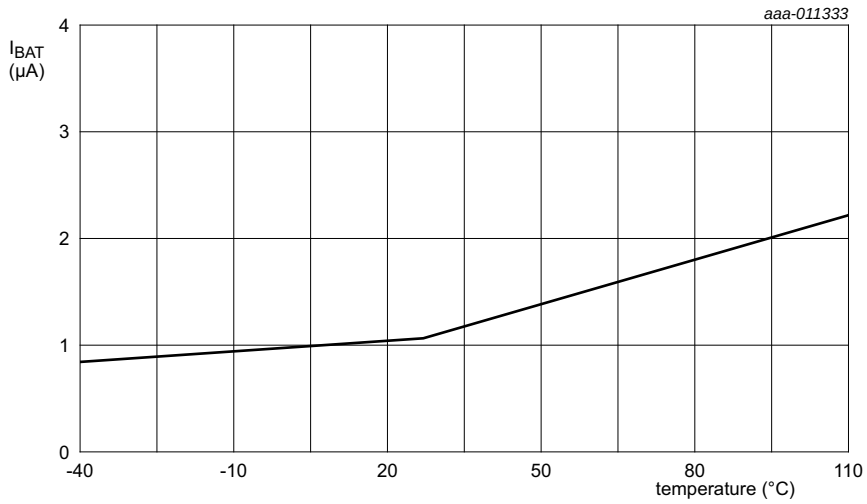
Following reset, the LPC15xx operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 14 for an overview of the LPC15xx clock generation.



VBAT = 0 V.

Fig 23. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



VBAT = 3.3 V; V_{DD} floating.

Fig 24. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

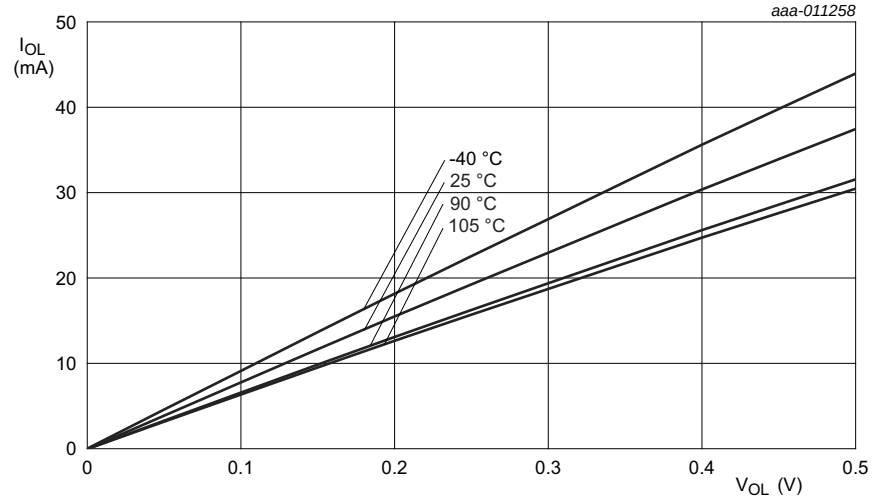
11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 72 MHz.

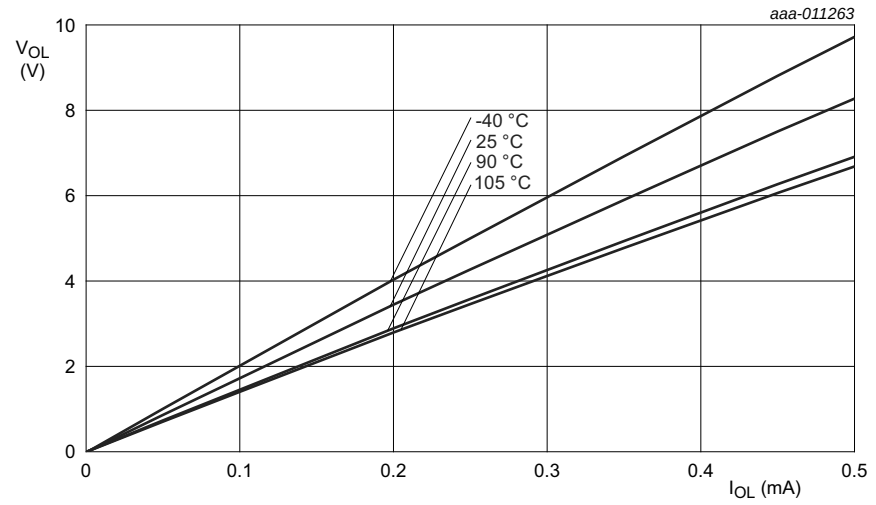
Table 12. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	72 MHz	
IRC	0.008	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.220	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator	0.002	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.045	-	-	Independent of main clock frequency.
Main PLL	-	0.085	-	-
USB PLL		0.100		
SCT PLL		0.110		
CLKOUT	-	0.005	0.01	Main clock divided by 4 in the CLKOUTDIV register.
ROM	-	0.015	0.02	-
GPIO + pin interrupt/pattern match	-	0.55	0.60	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	0.04	0.29	-
INPUT MUX		0.05	0.30	
IOCON	-	0.06	0.40	-
SCTimer0/PWM	-	0.18	1.10	-
SCTimer1/PWM	-	0.19	1.10	-
SCTimer2/PWM	-	0.13	0.70	-
SCTimer3/PWM	-	0.16	0.90	-
SCT IPU		0.02	0.1	
RTC	-	0.01	0.05	-
MRT	-	0.03	0.10	-
WWDT	-	0.01	0.10	Main clock selected as clock source for the WDT.
RIT		0.07	0.20	
QEI		0.12	0.80	
I2C0	-	0.02	0.12	-
SPI0	-	0.03	0.3	-
SPI1	-	0.01	0.28	-



Conditions: V_{DD} = 3.3 V; on pins PIO0_22 and PIO0_23.

Fig 28. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_24.

Fig 29. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

12.7 USART interface

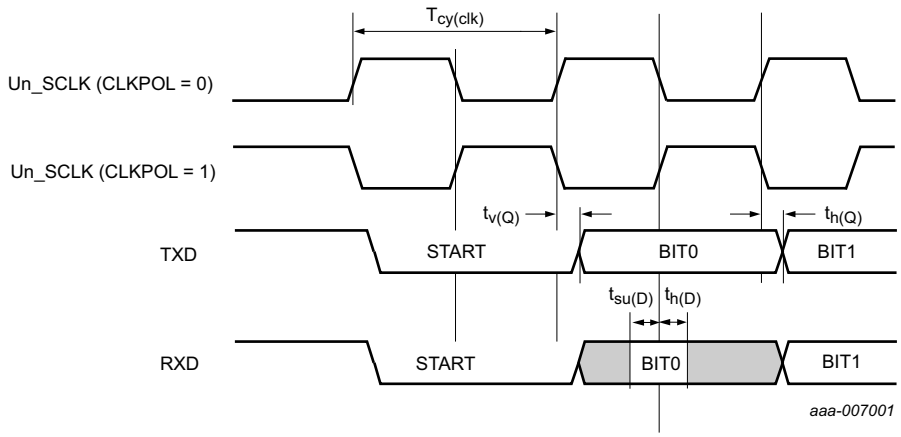
The maximum USART bit rate is 15 Mbit/s in synchronous mode master mode and 18 Mbit/s in synchronous slave mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_22 and PIO0_23.

Table 21. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	33	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	7	ns
$t_{h(Q)}$	data output hold time	2	-	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	13	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	28	ns
$t_{h(Q)}$	data output hold time	12	-	ns



In master mode, $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the LPC15xx *User manual UM10736*.

Fig 38. USART timing

Table 30. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	-	-	20	µs

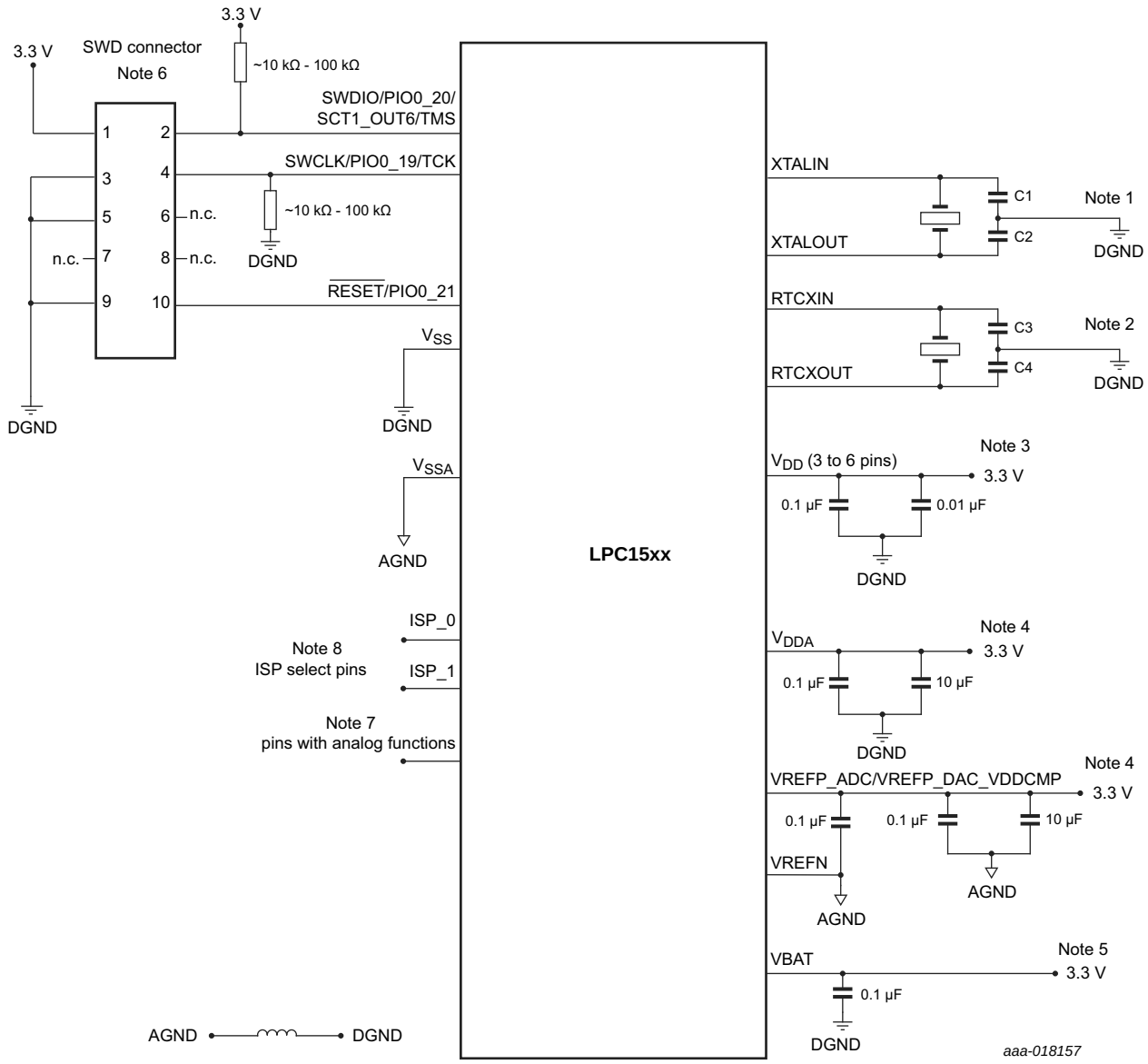
Table 31. Comparator voltage ladder reference static characteristics

V_{DDA} = 3.3 V; T_{amb} = -40 °C to + 105 °C; external or internal reference.

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	decimal code = 00 [2]	-	0	3	mV
		decimal code = 08	-1.5	0	+1.5	%
		decimal code = 16	-1.5	0	+1.5	%
		decimal code = 24	-1.5	0	+1.5	%
		decimal code = 30	-1.5	0	+1.5	%
		decimal code = 31	-1.5	0	+1.5	%

[1] Measured over a polyresistor matrix lot with a 2 kHz input signal and overdrive < 100 µV.

[2] All peripherals except comparator, temperature sensor, and IRC turned off.



(1) See Section 14.3 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.5 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(8) ISP pin assignments is dependent on package type. See Table 7 “Pin assignments for ISP modes”.

Fig 49. Power, clock, and debug connections

14.9 ElectroMagnetic Compatibility (EMC)

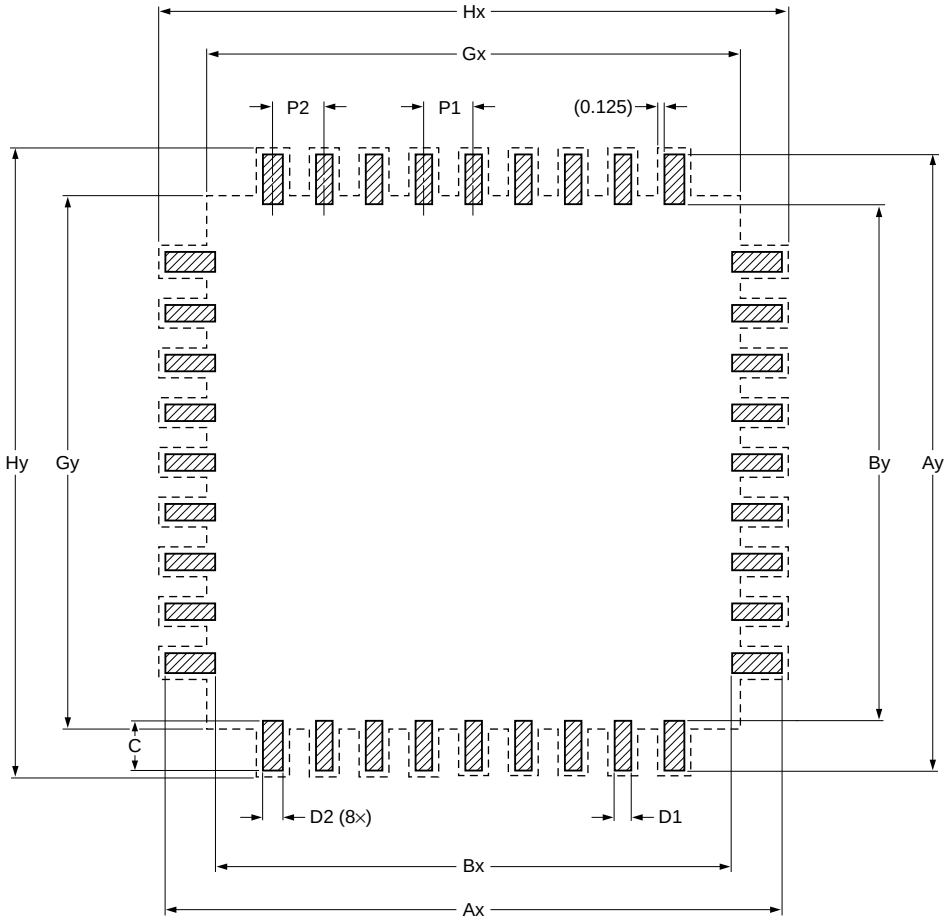
Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1549JBD100.

Table 36. ElectroMagnetic Compatibility (EMC) for part LPC1549 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =						Unit
		12 MHz	24 MHz	36 MHz	48 MHz	60 MHz	72 MHz	
Input clock: IRC (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-5	-1	-5	-4	-3	0	dBμV
	30 MHz to 150 MHz	-1	+3	+6	+8	+11	+14	dBμV
	150 MHz to 1 GHz	-1	+2	+5	+10	+9	+11	dBμV
IEC level[1]	-	O	O	O	N	N	M	-
Input clock: crystal oscillator (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-2	0	-5	-2	-2	2	dBμV
	30 MHz to 150 MHz	0	+3	+6	+8	+12	+14	dBμV
	150 MHz to 1 GHz	-1	+3	+5	+10	+10	+11	dBμV
IEC level[1]	-	O	O	O	N	N	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 55. Reflow soldering for the LQFP100 package