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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	EC000
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc000fn16r2

Table 2-2. Instruction Set Summary (Sheet 1 of 4)

Opcode	Operation	Syntax
ABCD	$Source_{10}$ + $Destination_{10}$ + X ® Destination	ABCD Dy,Dx ABCD Ð(Ay), Ð(Ax)
ADD	Source + Destination ® Destination	ADD <ea>,Dn ADD Dn,<ea>
ADDA	Source + Destination ® Destination	ADDA <ea>,An
ADDI	Immediate Data + Destination ® Destination	ADDI # <data>,<ea>
ADDQ	Immediate Data + Destination ® Destination	ADDQ # <data>,<ea>
ADDX	Source + Destination + X ® Destination	ADDX Dy, Dx ADDX Ð(Ay), Ð(Ax)
AND	Source L Destination ® Destination	AND <ea>,Dn AND Dn,<ea>
ANDI	Immediate Data L Destination ® Destination	ANDI # <data>, <ea>
ANDI to CCR	Source L CCR ® CCR	ANDI # <data>, CCR
ANDI to SR	If supervisor state then Source L SR ® SR else TRAP	ANDI # <data>, SR
ASL, ASR	Destination Shifted by <count> ® Destination	ASd Dx,Dy ASd # <data>,Dy ASd <ea>
Bcc	If (condition true) then PC + d ® PC	Bcc <label>
BCHG	~ (<number> of Destination) ® Z; ~ (<number> of Destination) ® <bit number> of Destination	BCHG Dn,<ea> BCHG # <data>,<ea>
BCLR	~ (<bit number> of Destination) ® Z; 0 ® <bit number> of Destination	BCLR Dn,<ea> BCLR # <data>,<ea>
BKPT	Run breakpoint acknowledge cycle; TRAP as illegal instruction	BKPT # <data>
BRA	PC + d ® PC	BRA <label>
BSET	~ (<bit number> of Destination) ® Z; 1 ® <bit number> of Destination	BSET Dn,<ea> BSET # <data>,<ea>
BSR	SP Ð 4® SP; PC ® (SP); PC + d ® PC	BSR <label>
BTST	Ð(<bit number> of Destination) ® Z;	BTST Dn,<ea> BTST # <data>,<ea>
CHK	If Dn < 0 or Dn > Source then TRAP	CHK <ea>,Dn
CLR	0 ® Destination	CLR <ea>
CMP	DestinationÑSource ® cc	CMP <ea>,Dn
CMPA	DestinationÑSource	CMPA <ea>,An
CMPI	Destination ÑImmediate Data	CMPI # <data>,<ea>
CMPM	DestinationÑSource ® cc	CMPM (Ay)+, (Ax)+
DBcc	If condition false then (Dn Ð 1® Dn; If Dn ¹ Ð1 then PC + d® PC)	DBcc Dn,<label>

For More Information On This Product,
Go to: www.freescale.com

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