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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5643af0mlu2r

- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.4.10 eMIOS

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels
- 3 channels' internal timebases can be shared between channels
- 1 Timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)

Each channel (0–23) supports the following functions:

- General-purpose input/output (GPIO)
- Single-action input capture (SAIC)
- Single-action output compare (SAOC)
- Output pulse-width modulation buffered (OPWMB)
- Input period measurement (IPM)
- Input pulse-width measurement (IPWM)
- Double-action output compare (DAOC)
- Modulus counter buffered (MCB)
- Output pulse width and frequency modulation buffered (OPWFMB)

1.4.11 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

MPC5644A devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the MPC5644A MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHZ for SOUT and SCK pins for DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI Module can generate and check parity in a serial frame

1.4.15 eSCI

Three enhanced serial communications interface (eSCI) modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.4.16 FlexCAN

The MPC5644A MCU includes three controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to

- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.4.20 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC features:

- Support for CRC-16-CCITT (x25 protocol):
  — $X^{16} + X^{12} + X^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.4.21 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the MPC5644A.

The sources of the ECC errors are:

- Flash
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 Parameter RAM)

1.4.22 External bus interface (EBI)

The MPC5644A device features an external bus interface that is available in 324 TEPBGA and calibration packages.

The EBI supports operation at frequencies of system clock /1, /2 and /4, with a maximum frequency support of 80 MHz. Customers running the device at 120 MHz or 132 MHz will use the /2 divider, giving an EBI frequency of 60 MHz or 66 MHz. Customers running the device at 80 MHz will be able to use the /1 divider to have the EBI run at the full 80 MHz frequency.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller with support for various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing included to support 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
BOOTCFG[1] IRQ[3] ETRIG3 GPIO[212]	Boot Config. Input External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	212	I I I I/O	VDDEH6 Slow	— / Down	BOOTCFG[1] / Down	85	M15	U21
WKPCFG NMI DSPI_B_SOUT GPIO[213]	Weak Pull Config. Input Non-Maskable Interrupt DSPI D data output GPIO	P A1 A2 G	001 010 100 000	213	I I O I/O	VDDEH6 Medium	— / Up	WKPCFG / Up	86	L15	AA20
External Bus Interface											
CS[0] ADDR[8] GPIO[0]	External chip selects External address bus GPIO	P A1 G	01 10 00	0	O I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	G1
CS[1] ADDR9 GPIO[1]	External chip selects External address bus GPIO	P A1 G	01 10 00	1	O I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H1
CS[2] ADDR10 WE[2]/BE[2] CAL_WE[2]/BE[2] GPIO[2]	External chip selects External address bus Write/byte enable Cal. bus write/byte enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	2	O I/O O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H2
CS[3] ADDR11 WE[3]/BE[3] CAL_WE[3]/BE[3] GPIO[3]	External chip selects External address bus Write/byte enable Cal bus write/byte enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	3	O I/O O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H4
ADDR12 GPIO[8]	External address bus GPIO	P G	01 00	8	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	N2
ADDR13 WE[2] GPIO[9]	External address bus Write/byte enable GPIO	P A2 G	001 100 000	9	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	N1
ADDR14 WE[3] GPIO[10]	External address bus Write/byte enables GPIO	P A2 G	001 100 000	10	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	P1
ADDR15 GPIO[11]	External address bus GPIO	P G	01 00	11	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	P2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_ADDR[17] CAL_DATA[17]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[18] CAL_DATA[18]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[19] CAL_DATA[19]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[20] CAL_DATA[20]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[21] CAL_DATA[21]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[22] CAL_DATA[22]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[23] CAL_DATA[23]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[24] CAL_DATA[24]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[25] CAL_DATA[25]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[26] CAL_DATA[26]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[27] CAL_DATA[27]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[28] CAL_DATA[28]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[29] CAL_DATA[29]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[30] CAL_DATA[30]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_DATA[0]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[1]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_DATA[2]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[3]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[4]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[5]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[6]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[7]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[8]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[9]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration read/write enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{WE}$[0]/$\overline{BE}$[0]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA0 ETPUA12_O[8] ETPUA19_O[8] GPIO[114]	eTPU A channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	114	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	61	N3	Y12
ETPUA1 ETPUA13_O[8] GPIO[115]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	115	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	60	M3	W12
ETPUA2 ETPUA14_O[8] GPIO[116]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	116	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	59	P2	AA11
ETPUA3 ETPUA15_O[8] GPIO[117]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	117	I/O O I/O	VDDEH4 Slow	— / WKPCFG	GPIO / WKPCFG	58	P1	Y11
ETPUA4 ETPUA16_O[8] FR_B_TX GPIO[118]	eTPU A channel eTPU A channel (output only) Flexray TX data channel B GPIO	P A1 A3 G	0001 0010 1000 0000	118	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	56	N2	W11
ETPUA5 ETPUA17_O[8] DSPI_B_SCK_LVDS- FR_B_TX_EN GPIO[119]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI clock Flexray TX data enable for ch. B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	119	I/O O O O I/O	VDDEH4 Slow + LVDS	— / WKPCFG	— / WKPCFG	54	M4	AB11
ETPUA6 ETPUA18_O[8] DSPI_B_SCK_LVDS+ FR_B_RX GPIO[120]	eTPU A channel eTPU A channel (output only) LVDS positive DSPI clock Flexray RX data channel B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	120	I/O O O I I/O	VDDEH4 Medium + LVDS	— / WKPCFG	— / WKPCFG	53	L3	AB10
ETPUA7 ETPUA19_O[8] DSPI_B_SOUT_LVDS- ETPUA6_O[8] GPIO[121]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI data out eTPU A channel (output only) GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	121	I/O O O O I/O	VDDEH4 Slow + LVDS	— / WKPCFG	— / WKPCFG	52	K3	AA10

- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.4 EMI (electromagnetic interference) characteristics

Table 12. EMI Testing Specifications[1]

Symbol	Parameter	Conditions	Clocks	Frequency Range	Level (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DDREG} = 5.25 V; T_A = 25 °C 150 kHz – 30 MHz RBW 9 kHz, Step Size 5 kHz 30 MHz – 1 GHz - RBW 120 kHz, Step Size 80 kHz	16 MHz crystal 40 MHz bus No PLL frequency modulation	150 kHz – 50 MHz	20	dBμV
				50 – 150 MHz	20	
				150 – 500 MHz	26	
				500 – 1000 MHz	26	
				IEC Level	K	—
				SAE Level	3	—
			16 MHz crystal 40 MHz bus ±2% PLL frequency modulation	150 kHz– 50 MHz	13	dBμV
				50 – 150 MHz	13	
				150 – 500 MHz	11	
				500 – 1000 MHz	13	
				IEC Level	L	—
				SAE Level	2	—

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03 and IEC 61967-2.

3.5 Electrostatic discharge (ESD) characteristics

Table 13. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for field induced charge Model (FDCM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

3.6 Power management control (PMC) and power on reset (POR) electrical specifications

Table 14. PMC Operating Conditions and External Regulators Supply Voltage

ID	Name			Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage V_{DDREG}	4.75	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)[1]	1.26[2]	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum required DC output current	400	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)[3]	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

[1] An internal regulator controller can be used to regulate core supply.

[2] The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.

[3] An internal regulator can be used to regulate 3.3 V supply.

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{DDREG}	SR	—	Voltage regulator supply voltage	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium I/O pad input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDEH}	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDE}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDE}	
V_{IL_LS}	CC	C	Multi-voltage I/O pad input low voltage in Low-swing-mode[5,6,7,8]	Hysteresis enabled	V_{SS}-0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS}-0.3	—	1.1	
V_{IL_HS}	CC	C	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS}-0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.4 V_{DDEH}	
V_{IH_S}	CC	C	Slow/medium pad I/O input high voltage[9]	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{IH_F}	CC	C	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE}+0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE}+0.3	
V_{IH_LS}	CC	C	Multi-voltage pad I/O input high voltage in low-swing-mode[5,6,7,8]	Hysteresis enabled	2.5	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDEH}+0.3	
V_{IH_HS}	CC	C	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (5.0 V)[1]

Name		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11[8]
	N/A							10[9]
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow[7,10]	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11[8]
	N/A							10[9]
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV[11] (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11[8]
	N/A							10[9]
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11[8]
Fast[12]	N/A							
pad_i_hv[13]	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads

6 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

7 Output delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Can be used on the tester.

9 This drive select value is not supported. If selected, it will be approximately equal to 11.

10 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

11 Selectable high/low swing IO pad with selectable slew in high swing mode only.

12 Fast pads are 3.3 V pads.

[2] This parameter is supplied for reference and is not guaranteed by design and not tested.

[3] Delay and rise/fall are measured to 20% or 80% of the respective signal.

[4] This parameter is guaranteed by characterization before qualification rather than 100% tested.

[5] In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads

[6] Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

[7] Output delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.

[8] Can be used on the tester.

[9] This drive select value is not supported. If selected, it will be approximately equal to 11.

[10] Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

[11] Selectable high/low swing IO pad with selectable slew in high swing mode only.

[12] Stand alone input buffer. Also has weak pull-up/pull-down.

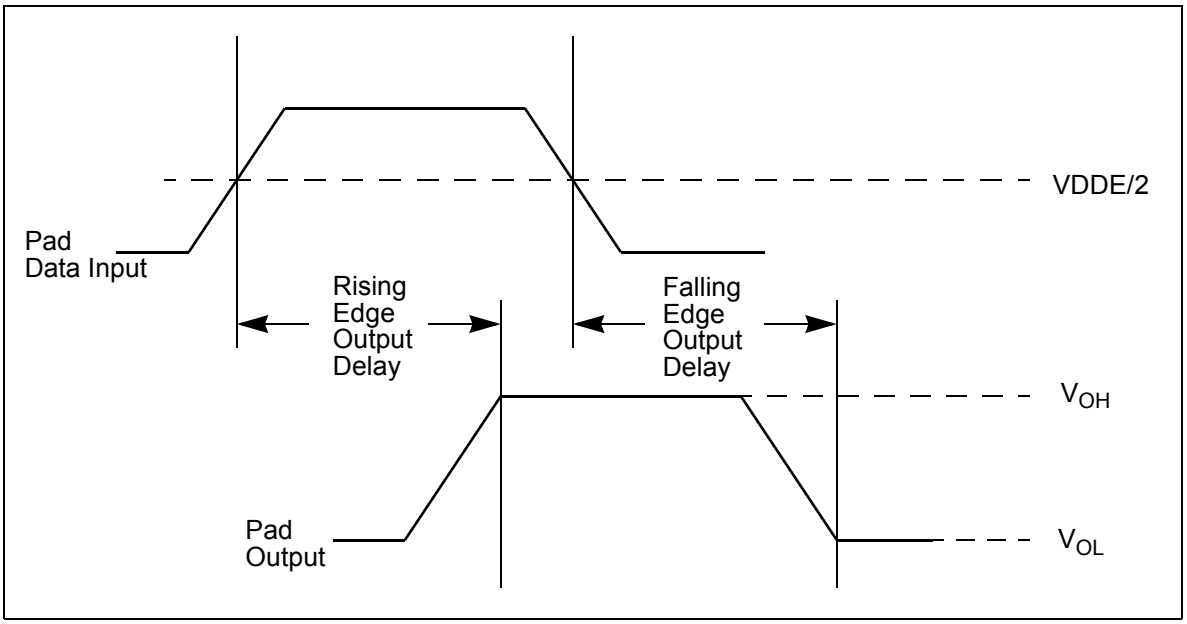


Figure 9. Pad output delay

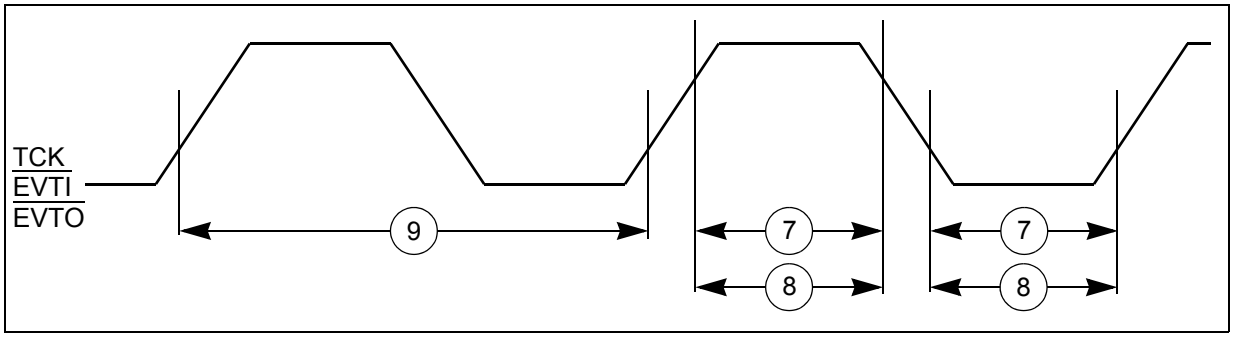


Figure 16. Nexus event trigger and test clock timings

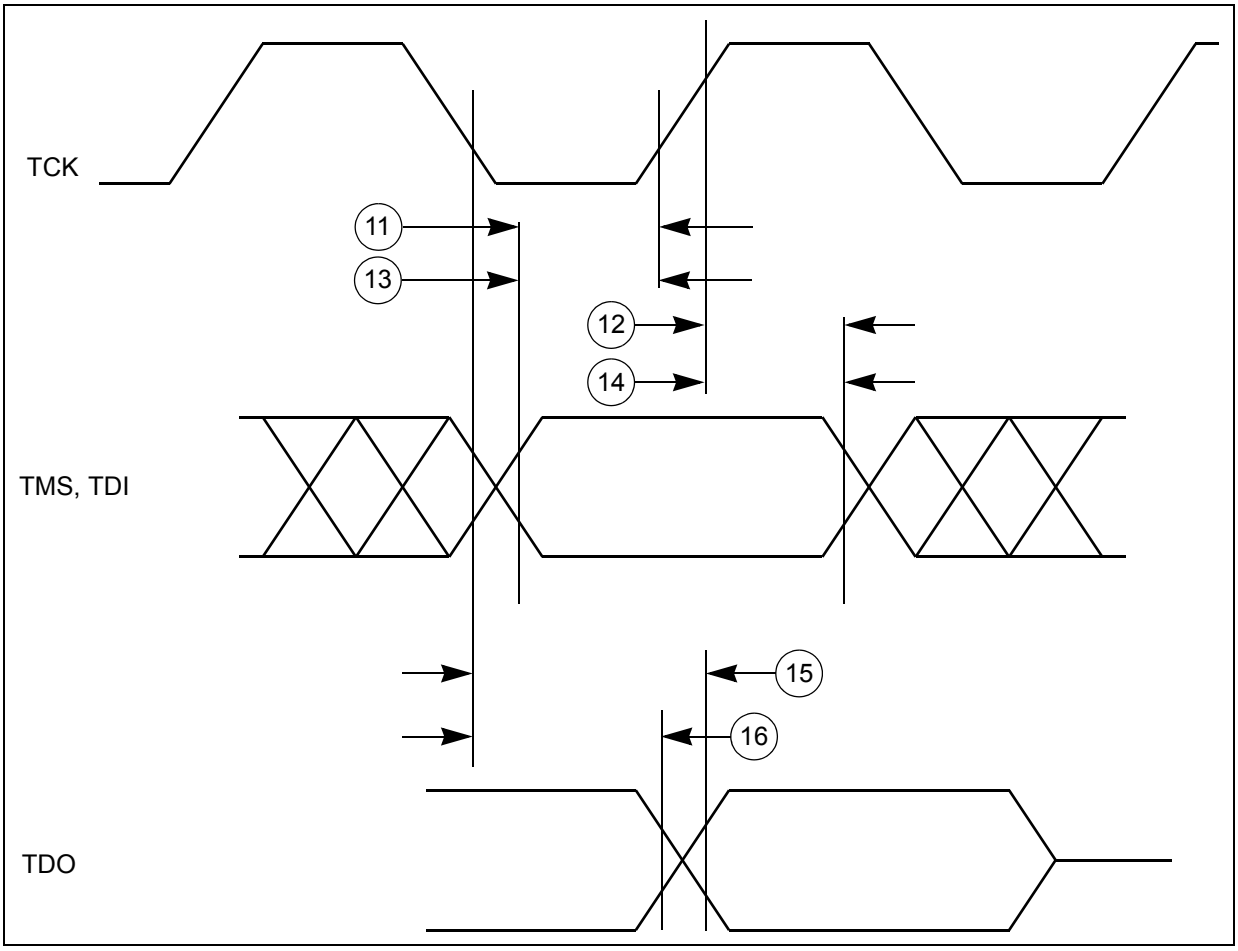


Figure 17. Nexus TDI, TMS, TDO timing

Table 40. Nexus debug port operating frequency

Package	Nexus Width	Nexus Routing	Nexus Pin Usage			Max. Operating Frequency
			MDO[0:3]	MDO[4:11]	CAL_MDO[4:11]	
176 LQFP 208 BGA 324 BGA	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
496 CSP	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
		Route to CAL_MDO[7]	Cal Nexus Data Out [0:3]	GPIO	Cal Nexus Data Out [4:11]	40 MHz[3]

1 NPC_PCR[FPM] = 0

2 NPC_PCR[NEXCFG] = 0

3 The Nexus AUX port runs up to 40 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 40 MHz.

4 NPC_PCR[FPM] = 1

5 Set the NPC_PCR[MCKO_DIV] to divide by two if the system frequency is between 40 MHz and 80 MHz inclusive. Set the NPC_PCR[MCKO_DIV] to divide by four if the system frequency is greater than 80 MHz.

6 Pad restrictions limit the Maximum Operation Frequency in these configurations

7 NPC_PCR[NEXCFG] = 1

3.17.4 External Bus Interface (EBI) and calibration bus interface timing

Table 41. External Bus Interface maximum operating frequency

Port Width	Multiplexed Mode	ADDR[12:15] Pin Usage	ADDR[16:31] Pin Usage	DATA[0:15] Pin Usage	Max. Operating Frequency
16-bit	Yes	ADDR[12:15]	GPIO	ADDR[16:31] DATA[0:15]	66 MHz[1]
16-bit	No	ADDR[12:15]	ADDR[16:31]	DATA[0:15]	33 MHz[2,3]
32-bit	Yes	ADDR[12:15]	ADDR[16:31] DATA[16:31]	DATA[0:15]	33 MHz[2,3]

1 Set SIU_ECCR[EBDF] to divide by two or divide by four if the system frequency is greater than 66 MHz.

2 System Frequency must be ≤132 MHz and SIU_ECCR[EBDF] set to divide by four.

3 Pad restrictions limit the maximum operating frequency.

Table 42. Calibration bus interface maximum operating frequency

Port Width	Multiplexed Mode	CAL_ADDR[12:15] Pin Usage	CAL_ADDR[16:30] Pin Usage	CAL_DATA[0:15] Pin Usage	Max. Operating Frequency
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz[1]
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz[1]
32-bit	Yes	CAL_WE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz[1]

1 Set SIU_ECCR[EBDF] to divide by two or divide by four if the system frequency is greater than 66 MHz

Table 43. External bus interface (EBI) and calibration bus operation timing [1]

#	Symbol		C	Characteristic	66 MHz (ext. bus)[2]		Unit	Notes
					Min	Max		
1	T_C	CC	P	CLKOUT Period	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	t_{CDC}	CC	D	CLKOUT duty cycle	45%	55%	T_C	
3	t_{CRT}	CC	D	CLKOUT rise time	—	[3]	ns	
4	t_{CFT}	CC	D	CLKOUT fall time	—	[3]	ns	
5	t_{COH}	CC	D	CLKOUT Posedge to Output Signal Invalid or High Z(Hold Time) • ADDR[8:31] • CS[0:3] • DATA[0:31] • OE • RD_WR • TS • WE[0:3]/BE[0:3]	1.3	—	ns	

3.17.5 External interrupt timing (IRQ pin)

Table 44. External interrupt timing[1]

#	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
3	IRQ Edge to Edge Time[2]	t_{ICYC}	6	—	t_{cyc}

1 IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

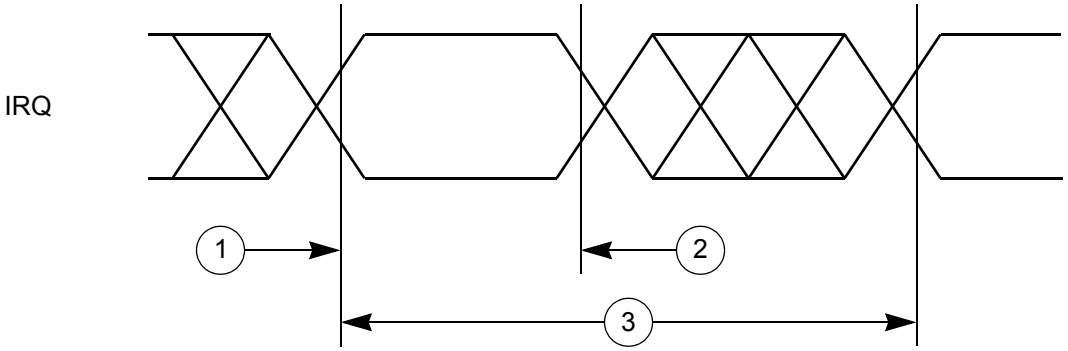


Figure 22. External Interrupt Timing

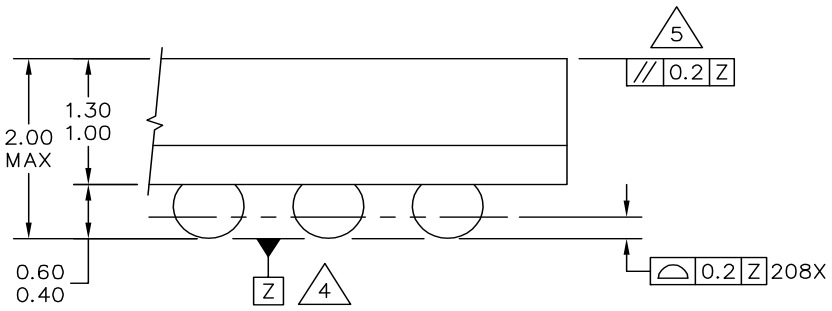
3.17.6 eTPU timing

Table 45. eTPU timing[1]

#	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}
2	eTPU Output Channel Pulse Width	t_{OCPW}	2[2]	—	t_{cyc}

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 2	11/2009	Maximum device speed is 145 MHz (was 150 MHz) 16-entry Memory Protection Unit (MPU). Was incorrectly listed as 8-entry. Feature details section added Changes to signal summary table: • Added ANY function to AN[10] • Added ANW function to AN[8] Changes to 208 ball BGA ballmap: • A12 is AN12-SDS (was AN12) • A15 is VRC33 (was VDD33) • B12 is AN13-SDO (was AN13) • C12 is AN14SDI (was AN14) • C13 is AN15-FCK (was AN15) • D1 is VRC33 (was VDD33) • F13 is VDDEH6AB (was VDDEH6) • H13 is GPIO99 (was PCSA3) • J15 is GPIO98 (was PCSA2) • K4 is now VDDEH1AB (was VDDEH1) • N6 is now VRC33 (was VDD33) • N9 is VDDEH4AB (was VDDEH4) • N12 is now VRC33 (was VDD33) • P6 is now NC • T13 is VDDE5 (was NC)
Rev. 2	11/2009 (cont.)	Recommended operating characteristics for power transistor updated Pad current specifications updated LVDS pad specifications updated. SRC does not apply to common mode voltage. Temperature sensor electrical characteristics added eQADC electrical characteristics updated with VGA gain specs Pad AC specifications updated Definition for RDY signal added to signal details V_{STBY} maximum is 5.5 V (was listed incorrectly as 6.0 V) I_{MAXA} maximum is 5 mA (was TBD) Analog differential input functions added to AN0–AN7 in signal summary

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 4 (cont)	08/2010	Change in signal name notation for DSPI, CAN and SCI signals: DSPI: PCS_x[n] is now DSPI_x_PCS[n] SOUT_x is now DSPI_x_SOUT SIN_x is now DSPI_x_SIN SCK_x is now DSPI_x_SCK CAN: CNTXx is now CAN_x_TX CNRXx is now CAN_x_RX SCI: RXDx is now SCI_x_RX TXDx is now SCI_x_TX Updates to DC electrical specifications: • Slew rate on power supply pins specification changed to 25 V/ms (was 50 V/ms) V_{OH_LS} min spec changed to 2.0 V at 0.5 mA (was 2.7 V at 0.5 mA) Updated I/O pad current specifications Updated I/O pad V_{RC33} current specifications Corrections to Nexus timing: • Maximum Nexus debug port operating frequency is 40 MHz in all configurations • To route Nexus to MDO, clear NPC_PCR[NEXCFG] (formerly this was documented as NPC_PCR[CAL] • To route Nexus to CAL_MDO, set NPC_PCR[NEXCFG]=1 (formerly this was documented as NPC_PCR[CAL]

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 5	2/2011	• Minor editorial updates. • Re-organized the first few subsections of the “Overview” section. • Added ECSM to the block diagram. • Added information on the REACM, SIU, and ECS modules to the “Block summary” section. • Added DATA[0:15] to V_{DDE5} in the “signal properties” table. • Updated VSTBY parameters in the “Power/ground segmentation” table. • Updated the parameter symbols and classifications throughout the document. • Updated footnote instances in the “Absolute maximum ratings” table. • Removed I_{MAXA} footnote in the “Absolute Maximum Ratings” table. • Updated the format of the “EMI (electromagnetic interference) characteristics” table. • Removed the footnote on V_{DDREG} in the “Power management control (PMC) and power on reset (POR) electrical specifications” table. • Updated values for Vbg, Idd3p3, Por3.3V_r, Por3.3V_f, Por5V_r, and Por5V_f in the “PMC electrical characteristics” table. • Updated “Bandgap reference supply voltage variation” in the “PMC Electrical Characteristics” table. • Updated VCE_{SAT} and V_{BE}in the “Recommended power transistors” operating characteristics” table. • Updated V_{IH_LS} in the “DC electrical specifications” table. • Updated the V_{OH_LS} min value in the “DC electrical specifications” table. • Updated I_{DDSTBY} and $I_{DDSTBY150}$ in the “DC electrical specifications” table. • Updated the I_{DDA}/I_{REF}/I_{DDREG} max value in the “DC electrical specifications” table. • Updated I_{ACT_F}, $I_{ACT\_MV\_PU}$, $I_{ACT\_MV\_PD}$, R_{PUPD5K}, $R_{PUPDMTCH}$, and footnotes in the “DC electrical specifications” table. • Updated Medium pad type I_{DD33} values in the “I/O pad V_{RC33} average I_{DDE} specifications” table. • Updated values for V_{OD} in the “DSPI LVDS pad specification” table. • Removed the footnotes from the “DSPI LVDS pad specifications” table. • Removed the redundant “XTAL Load Capacitance” parameter instance from the “PLLMRFM electrical specifications” table. • Updated footnotes in the “PLLMRFM electrical specifications” table. • Updated values for OFFNC and GAINNC in the “eQADC conversion specifications (operating)” table. • Added $DIFF_{max}$, $DIFF_{max2}$, $DIFF_{max4}$, and $DIFF_{cmv}$ parameters to the “eQADC conversion specifications (operating)” table. • Added the maximum operating frequency values in the “Cutoff frequency for additional SRAM wait state” table. • Updated multiple entries in the “APC, RWSC, WWSC settings vs. frequency of operation” table. • Removed footnote in the “APC, RWSC, WWSC settings vs. frequency of operation” table. • Changed the voltage in the “Pad AC specifications” table title from 4.5 V to 5.0 V. • Added the maximum LH/HL output delay values for pad type MultiV in the “Pad AC specifications (V_{DDE} = 3.3 V)” table.
Rev. 6	—	• Rev. 6 not published.