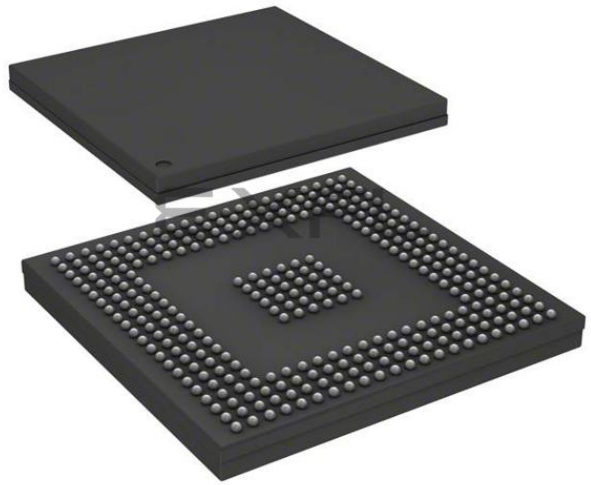

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643af0mvz2r

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The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of four semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU2 normal operation

- 1 receive FIFO per channel
- Up to 255 entries for each FIFO

- ECC support

1.4.18 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

1.4.18.1 Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system 'tick' signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

1.4.18.2 System timer module (STM)

The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR[1]. It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.4.19 Software watchdog timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock

1.AUTOSAR: AUTomotive Open System ARchitecture (see http://www.autosar.org)

1.4.23 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the VertiCal connector in the calibration address space. The Calibration EBI is only available in the VertiCal Calibration System.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.4.24 Power management controller (PMC)

The power management controller contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1) and the 5 V supply of the regulators (VDDREG).

1.4.25 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time Nexus Class3+ development support capabilities for the MPC5644A Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 and 2010 standards. MDO port widths of 4 pins and 12 pins are available in all packages.

1.4.26 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register

— 64-bit Censorship password register
— If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

1.4.27 Development Trigger Semaphore (DTS)

MPC5644A devices include a system development feature, the Development Trigger Semaphore (DTS) module, that enables software to signal an external tool by driving a persistent (affected only by reset or an external tool) signal on an external device pin. There is a variety of ways this module can be used, including as a component of an external real-time data acquisition system

1.5 MPC5644A series architecture

1.5.1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5644A series.

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
BOOTCFG[1] IRQ[3] ETRIG3 GPIO[212]	Boot Config. Input External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	212	I I I I/O	VDDEH6 Slow	— / Down	BOOTCFG[1] / Down	85	M15	U21
WKPCFG NMI DSPI_B_SOUT GPIO[213]	Weak Pull Config. Input Non-Maskable Interrupt DSPI D data output GPIO	P A1 A2 G	001 010 100 000	213	I I O I/O	VDDEH6 Medium	— / Up	WKPCFG / Up	86	L15	AA20
External Bus Interface											
CS[0] ADDR[8] GPIO[0]	External chip selects External address bus GPIO	P A1 G	01 10 00	0	O I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	G1
CS[1] ADDR9 GPIO[1]	External chip selects External address bus GPIO	P A1 G	01 10 00	1	O I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H1
CS[2] ADDR10 WE[2]/BE[2] CAL_WE[2]/BE[2] GPIO[2]	External chip selects External address bus Write/byte enable Cal. bus write/byte enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	2	O I/O O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H2
CS[3] ADDR11 WE[3]/BE[3] CAL_WE[3]/BE[3] GPIO[3]	External chip selects External address bus Write/byte enable Cal bus write/byte enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	3	O I/O O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H4
ADDR12 GPIO[8]	External address bus GPIO	P G	01 00	8	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	N2
ADDR13 WE[2] GPIO[9]	External address bus Write/byte enable GPIO	P A2 G	001 100 000	9	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	N1
ADDR14 WE[3] GPIO[10]	External address bus Write/byte enables GPIO	P A2 G	001 100 000	10	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	P1
ADDR15 GPIO[11]	External address bus GPIO	P G	01 00	11	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	P2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_$\overline{WE}$[1]/$\overline{BE}$[1]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A	01 10	343	O O	VDDE12 Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[11] / —	—	—	—
NEXUS											
$\overline{EVTI}$	Nexus event in	P	01	231	I	VDDEH7 MultiV[12,14]	— / Up	$\overline{EVTI}$ / Up	116	E15	H20
$\overline{EVTO}$	Nexus event out	P	01	227	O	VDDEH7 MultiV[12,14,15]	—	$\overline{EVTO}$ / —	120	D15	G20
MCKO	Nexus message clock out	P	—	219[11]	O	VRC33 Fast	—	MCKO / —	14	F15	F1
MDO0[16]	Nexus message data out	P	01	220	O	VRC33 Fast	—	MDO[0] / —	17	A14	F3
MDO1[16]	Nexus message data out	P	01	221	O	VRC33 Fast	—	MDO[1] / —	18	B14	G2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
TCK	JTAG test clock input	P	01	—	I	VDDEH7 MultiV[12]	TCK / Down	TCK / Down	128	C16	D21
TDI	JTAG test data input	P	01	232	I	VDDEH7 MultiV[12]	TDI / Up	TDI / Up	130	E14	D22
TDO	JTAG test data output	P	01	228	O	VDDEH7 MultiV[12]	TDO / Up	TDO / Up	123	F14	E21
TMS	JTAG test mode select input	P	01	—	I	VDDEH7 MultiV[12]	TMS / Up	TMS / Up	131	D14	E20
JCOMP	JTAG TAP controller enable	P	01	—	I	VDDEH7 MultiV[12]	JCOMP / Down	JCOMP / Down	121	F16	F20
FlexCAN											
CAN_A_TX SCI_A_TX GPIO[83]	FlexCAN A TX eSCI A TX GPIO	P A1 G	01 10 00	83	O O I/O	VDDEH6 Slow	— / Up	— / Up	81	P12	AB19
CAN_A_RX SCI_A_RX GPIO[84]	FlexCAN A RX eSCI A RX GPIO	P A1 G	01 10 00	84	I I I/O	VDDEH6 Slow	— / Up	— / Up	82	R12	Y19
CAN_B_TX DSPI_C_PCS[3] SCI_C_TX GPIO[85]	FlexCAN B TX DSPI C peripheral chip select eSCI C TX GPIO	P A1 A2 G	001 010 100 000	85	O O O I/O	VDDEH6 Slow	— / Up	— / Up	88	T12	Y22
CAN_B_RX DSPI_C_PCS[4] SCI_C_RX GPIO[86]	FlexCAN B RX DSPI C peripheral chip select eSCI C RX GPIO	P A1 A2 G	001 010 100 000	86	I O I I/O	VDDEH6 Slow	— / Up	— / Up	89	R13	W21
CAN_C_TX DSPI_D_PCS[3] GPIO[87]	FlexCAN C TX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	87	O O I/O	VDDEH6 Medium	— / Up	— / Up	101	K13	P19
CAN_C_RX DSPI_D_PCS[4] GPIO[88]	FlexCAN C RX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	88	I O I/O	VDDEH6 Slow	— / Up	— / Up	98	L14	V20
eSCI											

[6] All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

[7] AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

[8] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

[9] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[10] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[11] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Solder profile per IPC/JEDEC J-STD-020D.

[14] Moisture sensitivity per JEDEC test method A112.

3.3 Thermal characteristics

Table 9. Thermal characteristics for 176-pin QFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization.

[2] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[4] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage[9]		—	—	$0.2*V_{DDEH}$	V
V_{OL_F}	CC	P	Fast I/O output low voltage[9]		—	—	$0.2*V_{DDE}$	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[5,6,7,8,9]		—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode[9]		—	—	$0.2*V_{DDEH}$	V
V_{OH_S}	CC	P	Slow/medium pad I/O output high voltage[9]		0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage[9]		0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[5,6,7,8]	I_{OH_LS} = 0.5 mA	2.1	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[9]		0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	v
$I_{DD}+I_{DDPLL}$	CC	P	Operating current 1.2 V supplies	V_{DD} at 1.32 V at 80 MHz	—		380	mA
		P		V_{DD} at 1.32V at 120 MHz	—		400	mA
		P		V_{DD} at 1.32V at 150 MHz	—		400	mA

Table 25. DSPI LVDS pad specification (continued)

11	Delay, Z to Normal (High/Low)	T_{DZ}	CC	D	—		500		ns
12	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	CC	D	—			0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D	—	95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

3.10 Oscillator and PLLMRFM electrical characteristics

Table 26. PLLMRFM electrical specifications

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
$f_{ref\_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[1]		Crystal reference	4	40	MHz
		C			External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
f_{vco}	CC	P	VCO frequency range		—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]		—	16	150	MHz
f_{sys}	CC	T	System frequency in bypass mode[2]		Crystal reference	4	40	MHz
		P			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[3]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [4,5]		—	1.2	72.25	MHz
C_{JITTER}	CC	T	CLKOUT period jitter[6,7,8,9]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [10, 11]		—	—	10	ms

Table 26. PLLMRFM electrical specifications

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					min	max	
V_{IHEXT}	CC	T	EXTAL input high voltage	Crystal Mode[12]	Vxtal + 0.4	—	V
		T		External Reference[12, 13]	V_{RC33} /2 + 0.4	V_{RC33}	
V_{ILEXT}	CC	T	EXTAL input low voltage	Crystal Mode[12]	—	Vxtal - 0.4	V
		T		External Reference[12, 13]	0	V_{RC33} /2 - 0.4	
—	CC	T	XTAL load capacitance[10]	4 MHz	5	30	pF
				8 MHz	5	26	
				12 MHz	5	23	
				16 MHz	5	19	
				20 MHz	5	16	
				40 MHz	5	8	
t_{lpll}	CC	P	PLL lock time [10, 14]	—	—	200	µs
t_{dc}	CC	T	Duty cycle of reference	—	40	60	%
f_{LCK}	CC	T	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	T	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	CC	D	Modulation Depth	Center spread	±0.25	±4.0	% f_{sys}
		D		Down Spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency[15]	—	—	100	kHz

1 Considering operation with PLL not bypassed.

2 All internal registers retain data at 0 Hz.

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

5 f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

6 This value is determined by the crystal manufacturer and board design.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

Table 29. eQADC single ended conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
OFFNC	CC	C	Offset error without calibration	0	160	Counts
OFFWC	CC	C	Offset error with calibration	–4	4	Counts
GAINNC	CC	C	Full scale gain error without calibration	–160	0	Counts
GAINWC	CC	C	Full scale gain error with calibration	–4	4	Counts
I_{INJ}	CC	T	Disruptive input injection current [1, 2, 3, 4]	–3	3	mA
E_{INJ}	CC	T	Incremental error due to injection current[5,6]	–4	4	Counts
TUE8	CC	C	Total unadjusted error (TUE) at 8 MHz	–4	4[6]	Counts
TUE16	CC	C	Total unadjusted error at 16 MHz	–8	8	Counts

1 Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.

2 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.

4 Condition applies to two adjacent pins at injection limits.

5 Performance expected with production silicon.

6 All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}

Table 30. eQADC differential ended conversion specifications (operating)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA1[1]	CC	–	Variable gain amplifier accuracy (gain=1)[2]				
	CC	C	INL	8 MHz ADC	–4	4	Counts[3]
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3[4]	3[4]	Counts
	CC	C		16 MHz ADC	–3[4]	3[4]	Counts

[2] This parameter is supplied for reference and is not guaranteed by design and not tested.

[3] Delay and rise/fall are measured to 20% or 80% of the respective signal.

[4] This parameter is guaranteed by characterization before qualification rather than 100% tested.

[5] In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads

[6] Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

[7] Output delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.

[8] Can be used on the tester.

[9] This drive select value is not supported. If selected, it will be approximately equal to 11.

[10] Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

[11] Selectable high/low swing IO pad with selectable slew in high swing mode only.

[12] Stand alone input buffer. Also has weak pull-up/pull-down.

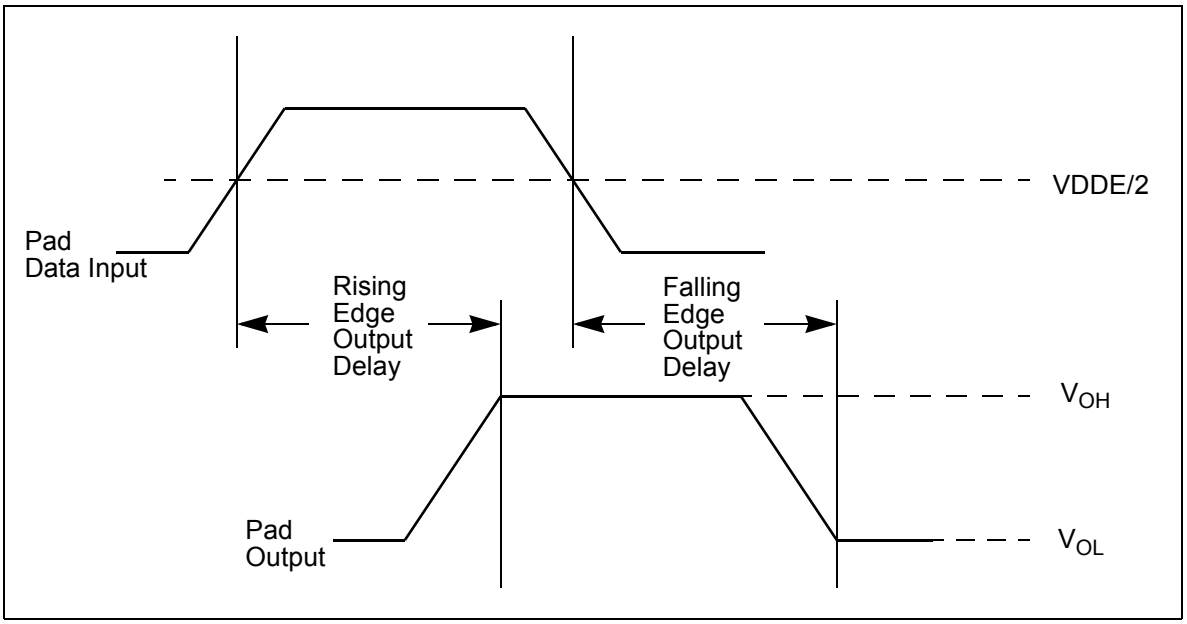

Figure 9. Pad output delay

The tool/debugger must provide at least one TCK clock for the EVTI signal to be recognized by the MCU. When using the RDY signal to indicate the end of a Nexus read/write access, ensure that TCK continues to run for at least 1 TCK after leaving the Update-DR state. This can be just a TCK with TMS low while in the Run-Test/Idle state or by continuing with the next Nexus/JTAG command. Expect the affect of EVTI and RDY to be delayed by edges of TCK. Note: RDY is not available in all packages of all devices.

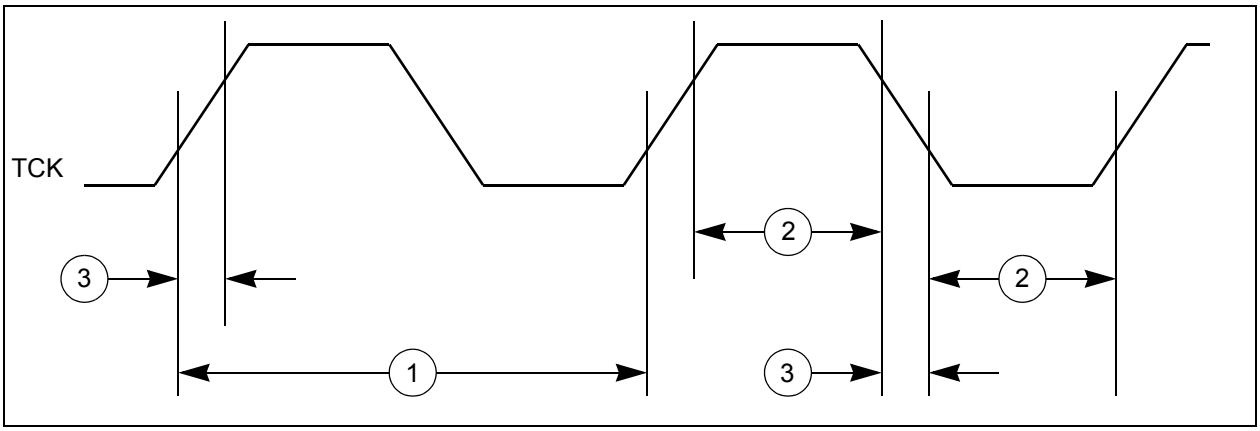

Figure 11. JTAG test clock input timing

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK	—	19.5	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	5.25	—	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.

3 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4 This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

5 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

6 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

8 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

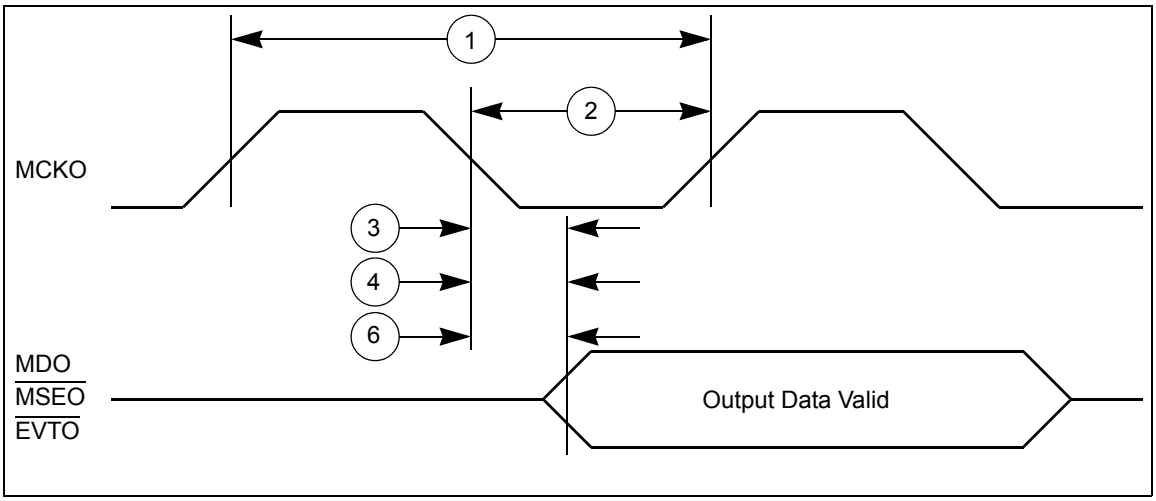

Figure 15. Nexus output timing

Table 40. Nexus debug port operating frequency

Package	Nexus Width	Nexus Routing	Nexus Pin Usage			Max. Operating Frequency
			MDO[0:3]	MDO[4:11]	CAL_MDO[4:11]	
176 LQFP 208 BGA 324 BGA	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
496 CSP	Reduced port mode[1]	Route to MDO[2]	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz[3]
	Full port mode[4]	Route to MDO[2]	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz[5,6]
		Route to CAL_MDO[7]	Cal Nexus Data Out [0:3]	GPIO	Cal Nexus Data Out [4:11]	40 MHz[3]

1 NPC_PCR[FPM] = 0

2 NPC_PCR[NEXCFG] = 0

3 The Nexus AUX port runs up to 40 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 40 MHz.

4 NPC_PCR[FPM] = 1

5 Set the NPC_PCR[MCKO_DIV] to divide by two if the system frequency is between 40 MHz and 80 MHz inclusive. Set the NPC_PCR[MCKO_DIV] to divide by four if the system frequency is greater than 80 MHz.

6 Pad restrictions limit the Maximum Operation Frequency in these configurations

7 NPC_PCR[NEXCFG] = 1

[4] The actual minimum SCK cycle time is limited by pad performance.

[5] For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.

[6] The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

[7] Timing met when pcssck = 3(01), and cssck =2 (0000).

[8] The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

[9] Timing met when ASC = 2 (0000), and PASC = 3 (01).

[10] Timing met when pcssck = 3.

[11] Timing met when ASC = 3.

[12] This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

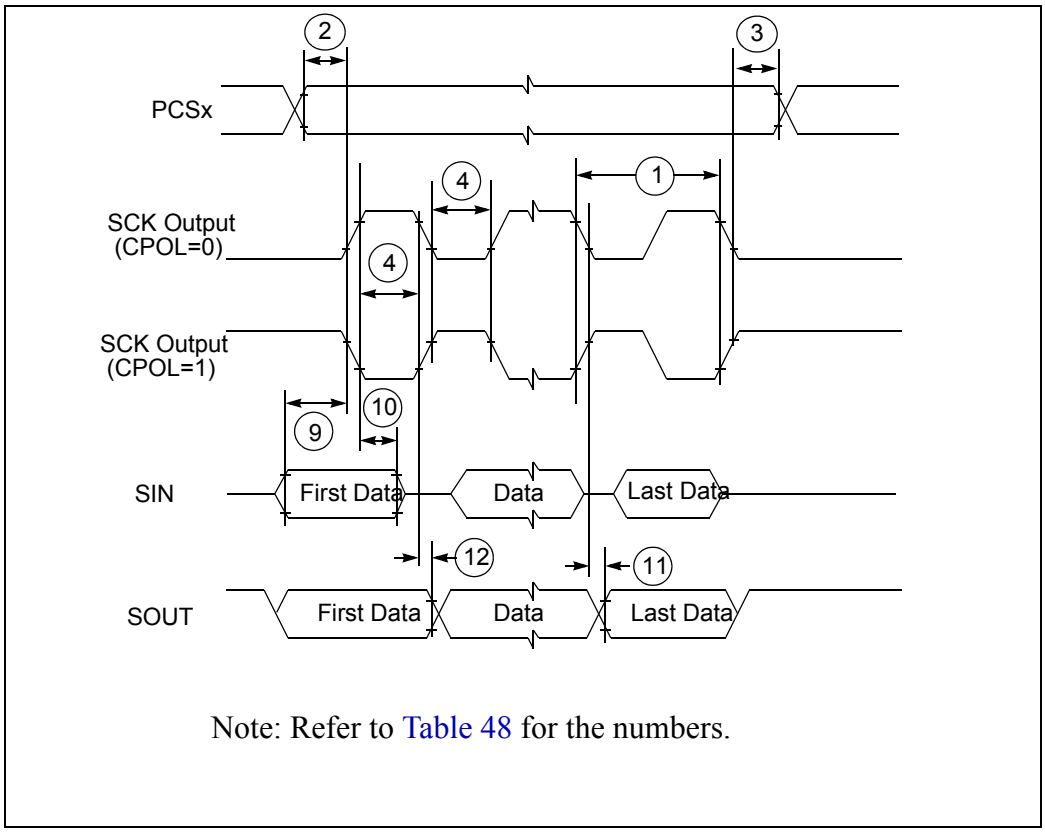

Figure 23. DSPI classic SPI timing — master, CPHA = 0

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 3	04/2010	Changes to Signal Properties table (changes apply to Revision 2 and later devices: EBI changes: • WE_BE[2] (A2) and CAL_WE_BE[2] (A3) signals added to CS[2] (PCR 2) • WE_BE[3] (A2) and CAL_WE_BE[3] (A3) signals added to CS[3] (PCR 3) Calibration bus changes: • CAL_WE[2]/BE[2] (A2) signal added to CAL_CS[2] (PCR 338) • CAL_WE[3]/BE[3] (A2) signal added to CAL_CS[3] (PCR 339) • CAL_ALE (A1) added to CAL_ADDR[15] (PCR 340) eQADC changes: • AN[8] and AN[38] pins swapped. AN[8] Is now on pins 9 (176-pin), B3 (208-ball) and E1 (324-ball). AN[8] was on D3 (324-ball) on previous devices. AN[38] Is now on D3 (324-ball). AN[38] was on pins 9 (176-pin), B3 (208-ball) and E1 (324-ball) on previous devices. • ANZ function added to AN11 pin Reaction channels added to eTPU2: • RCH0_A (A3) added to ETPU_A[14] (PCR 128) • RCH0_B (A2) added to ETPU_A[20] (PCR 134) • RCH0_C (A2) added to ETPU_A[21] (PCR 135) • RCH1_A (A2) added to ETPU_A[15] (PCR 129) • RCH1_B (A2) added to ETPU_A[9] (PCR 123) • RCH1_C (A2) added to ETPU_A[10] (PCR 124) • RCH2_A (A2) added to ETPU_A[16] (PCR 130) • RCH3_A (A2) added to ETPU_A[17] (PCR 131 • RCH4_A (A2) added to ETPU_A[18] (PCR 132)) • RCH4_B (A2) added to ETPU_A[11] (PCR 125) • RCH4_C (A2) added to ETPU_A[12] (PCR 126) • RCH5_A (A2) added to ETPU_A[19] (PCR 133) • RCH5_B (A2) added to ETPU_A[28] (PCR 142) • RCH5_C (A2) added to ETPU_A[29] (PCR 143) Reaction channels added to eMIOS: • RCH2_B (A2) added to EMIOS[2] (PCR 181) • RCH2_C (A2) added to EMIOS[4] (PCR 183) • RCH3_B (A2) added to EMIOS[10] (PCR 189) • RCH3_C (A2) added to EMIOS[11] (PCR 190) Pad changes: • ETPUA16 (PCR 130) has Medium (was Slow) pad • ETPUA17 (PCR 131) has Medium (was Slow) pad • ETPUA18 (PCR 132) has Medium (was Slow) pad • ETPUA19 (PCR 133) has Medium (was Slow) pad • ETPUA25 (PCR 139) has Slow+LVDS (was Medium+LVDS) pads Signal Details table updated: • Added eTPU2 reaction channels • Changed IRQ[0:15] to two ranges, excluding IRQ6, which does not exist on this device • Changed TCR_A to TCRCLKA (TCR_A is the pin name, not the signal name) • Changed WE_BE[0:1] to WE_BE[0:3] (2 new signals added to Rev. 2). Also changed notation from “WE_BE[n]” to “WE[n]/BE[n]” to be consistent.

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 7 (cont.)	01/12	• Added Table 17MPC5644A External network specification. • Updated Figure 8. • Changed External Network Parameter Ce min value to “3*2.35μF+5μF” from “2*2.35μF+5μF” in Table 17MPC5644A External network specification. • Changed Trans. Line (differential Zo) unit to Ω from W in Table 25DSPI LVDS pad specification.