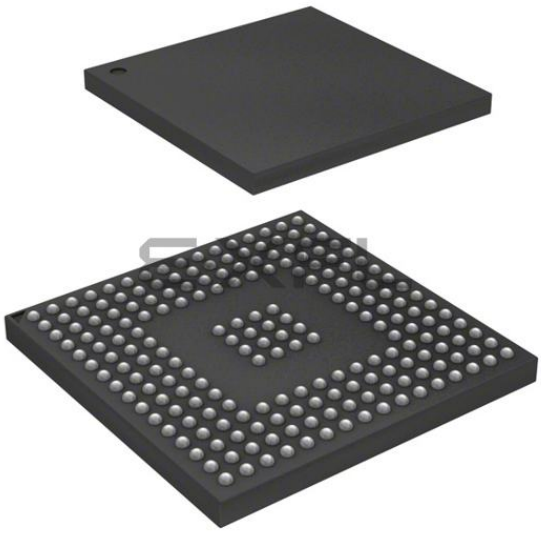

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	120
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644af0mmg2r

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Document Number: MPC5644A_AD
Rev. 1
12/2014

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of four semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU2 normal operation

- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.4.20 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC features:

- Support for CRC-16-CCITT (x25 protocol):
  — $X^{16} + X^{12} + X^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.4.21 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the MPC5644A.

The sources of the ECC errors are:

- Flash
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 Parameter RAM)

1.4.22 External bus interface (EBI)

The MPC5644A device features an external bus interface that is available in 324 TEPBGA and calibration packages.

The EBI supports operation at frequencies of system clock /1, /2 and /4, with a maximum frequency support of 80 MHz. Customers running the device at 120 MHz or 132 MHz will use the /2 divider, giving an EBI frequency of 60 MHz or 66 MHz. Customers running the device at 80 MHz will be able to use the /1 divider to have the EBI run at the full 80 MHz frequency.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller with support for various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing included to support 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

12	13	14	15	16	17	18	19	20	21	22	
VSS	VSS	VSS					VRC33	NC	NC	VDDEH6AB	M
VSS	VSS	VSS					NC	SCI_A_TX	VSS	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							NC	NC	NC	RESET	R
							VSS	BOOTCFG0	VSS[1]	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG1	EXTAL	U
							SCI_C_RX	CAN_C_RX	PLLREF	XTAL	V
ETPUA1	EMIOS1	VDDEH4AB	EMIOS8	EMIOS15	EMIOS16	EMIOS23	SCI_C_TX	VDD	CAN_B_RX	VDDPLL	W
ETPUA0	EMIOS2	EMIOS5	EMIOS9	EMIOS14	EMIOS17	EMIOS22	CAN_A_RX	VSS	VDD	CAN_B_TX	Y
EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS18	EMIOS21	VDDEH4AB	WKPCFG	VSS	VDD	AA
TCRCLKA	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS19	EMIOS20	CAN_A_TX	SCI_B_RX	SCI_B_TX	VSS	AB

1 This pin (T21) should be tied low.

Figure 7. 324-pin TEPBGA package ballmap (southeast, viewed from above)

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_ADDR[17] CAL_DATA[17]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[18] CAL_DATA[18]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[19] CAL_DATA[19]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[20] CAL_DATA[20]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[21] CAL_DATA[21]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[22] CAL_DATA[22]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[23] CAL_DATA[23]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[24] CAL_DATA[24]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[25] CAL_DATA[25]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[26] CAL_DATA[26]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[27] CAL_DATA[27]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[28] CAL_DATA[28]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[29] CAL_DATA[29]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[30] CAL_DATA[30]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_DATA[0]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[1]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
eQADC											
AN0[18] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[0] / —	172	B5	C6
AN1[18] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[1] / —	171	A6	C7
AN2[18] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[2] / —	170	D6	D7
AN3[18] DAN1-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[3] / —	169	C7	D8
AN4[18] DAN2+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[4] / —	168	B6	B7
AN5[18] DAN2-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[5] / —	167	A7	B8
AN6[18] DAN3+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[6] / —	166	D7	C8
AN7[18] DAN3-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[7] / —	165	C8	C9
AN8 ANW	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA Analog	I / —	AN[8] / —	9	B3	E1
AN9 ANX	Single-ended Analog Input External Multiplexed Analog Input	P	01	—	I I	VDDA Analog	I / —	AN[9] / —	5	A2	C2
AN10 ANY	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA Analog	I / —	AN[10] / —	—	—	D1
AN11 ANZ	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA Analog	I / —	AN[11] / —	4	A3	C1
AN12 - SDS MA0 ETPUA19_O[8] $\overline{SDS}$	Single-ended Analog Input MUX Address 0 eTPU A channel (output only) eQADC Serial Data Select	P A1 A2 G	001 010 100 000	215	I O O I/O	VDDEH7[19] Medium	I / —	AN[12] / —	148	A12	C13
AN13 - SDO MA1 ETPUA21_O[8] SDO	Single-ended Analog Input MUX Address 1 eTPU A channel (output only) eQADC Serial Data Out	P A1 A2 G	001 010 100 000	216	I O O O	VDDEH7[19] Medium	I / —	AN[13] / —	147	B12	B13

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
AN14 - SDI MA2 ETPUA27_O[8] SDI	Single-ended Analog Input MUX Address 2 eTPU A channel (output only) eQADC Serial Data In	P A1 A2 G	001 010 100 000	217	I O O I	VDDEH7[19] Medium	I / —	AN[14] / —	146	C12	A13
AN15 - FCK FCK ETPUA29_O[8]	Single-ended Analog Input eQADC Free Running Clock eTPU A channel (output only)	P A1 A2	001 010 100	218	I O O	VDDEH7[19] Medium	I / —	AN[15] / —	145	C13	A14
AN16	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[16] / —	3	C6	A3
AN17	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[17] / —	2	C4	A4
AN18	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[18] / —	1	D5	B4
AN19	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[19] / —	—	—	D6
AN20	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[20] / —	—	—	C5
AN21	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[21] / —	173	B4	B6
AN22	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[22] / —	161	B8	D9
AN23	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[23] / —	160	C9	A8
AN24	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[24] / —	159	D8	B9
AN25	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[25] / —	158	B9	A9
AN26	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[26] / —	—	—	D10
AN27	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[27] / —	157	A10	C10
AN28	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[28] / —	156	B10	D11

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
AN29	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[29] / —	—	—	C11
AN30	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[30] / —	155	D9	B11
AN31	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[31] / —	154	D10	D12
AN32	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[32] / —	153	C10	C12
AN33	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[33] / —	152	C11	B12
AN34	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[34] / —	151	C5	A12
AN35	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[35] / —	150	D11	D13
AN36	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[36] / —	174	F4	B5
AN37	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[37] / —	175	E3	A5
AN38	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[38] / —	—	—	D3
AN39	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[39] / —	8	D2	D2
VRH	Voltage Reference High	P	—	—	I	VDDA —	I / —	VRH	163	A8	A10
VRL	Voltage Reference Low	P	—	—	I	VDDA —	I / —	VRL	162	A9	A11
REFBYBC	Reference Bypass Capacitor Input	P	—	—	I	VDDA Analog	I / —	REFBYPC	164	B7	B10
eTPU2											
TCRCLKA IRQ[7] GPIO[113]	eTPU A TCR clock External interrupt request GPIO	P A1 G	01 10 00	113	I I I/O	VDDEH4 Slow	— / Up	— / Up	—	L4	AB12

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA0 ETPUA12_O[8] ETPUA19_O[8] GPIO[114]	eTPU A channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	114	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	61	N3	Y12
ETPUA1 ETPUA13_O[8] GPIO[115]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	115	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	60	M3	W12
ETPUA2 ETPUA14_O[8] GPIO[116]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	116	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	59	P2	AA11
ETPUA3 ETPUA15_O[8] GPIO[117]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	117	I/O O I/O	VDDEH4 Slow	— / WKPCFG	GPIO / WKPCFG	58	P1	Y11
ETPUA4 ETPUA16_O[8] FR_B_TX GPIO[118]	eTPU A channel eTPU A channel (output only) Flexray TX data channel B GPIO	P A1 A3 G	0001 0010 1000 0000	118	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	56	N2	W11
ETPUA5 ETPUA17_O[8] DSPI_B_SCK_LVDS- FR_B_TX_EN GPIO[119]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI clock Flexray TX data enable for ch. B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	119	I/O O O O I/O	VDDEH4 Slow + LVDS	— / WKPCFG	— / WKPCFG	54	M4	AB11
ETPUA6 ETPUA18_O[8] DSPI_B_SCK_LVDS+ FR_B_RX GPIO[120]	eTPU A channel eTPU A channel (output only) LVDS positive DSPI clock Flexray RX data channel B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	120	I/O O O I I/O	VDDEH4 Medium + LVDS	— / WKPCFG	— / WKPCFG	53	L3	AB10
ETPUA7 ETPUA19_O[8] DSPI_B_SOUT_LVDS- ETPUA6_O[8] GPIO[121]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI data out eTPU A channel (output only) GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	121	I/O O O O I/O	VDDEH4 Slow + LVDS	— / WKPCFG	— / WKPCFG	52	K3	AA10

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA25 IRQ[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU A channel External interrupt request LVDS positive DSPI clock GPIO	P A1 A2 G	001 010 100 000	139	I/O I O I/O	VDDEH1 Medium + LVDS	— / WKPCFG	— / WKPCFG	27	G3	M3
ETPUA26 IRQ[14] DSPI_C_SOUT_LVDS- GPIO[140]	eTPU A channel External interrupt request LVDS negative DSPI data out GPIO	P A1 A2 G	001 010 100 000	140	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	26	F3	L2
ETPUA27 IRQ[15] DSPI_C_SOUT_LVDS+ DSPI_B_SOUT GPIO[141]	eTPU A channel External interrupt request LVDS positive DSPI data out DSPI data out GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	141	I/O I O O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	25	G2	L1
ETPUA28 DSPI_C_PCS[1] RCH5_B GPIO[142]	eTPU A channel DSPI C peripheral chip select Reaction channel 5B GPIO	P A1 A2 G	001 010 100 000	142	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	24	F1	M4
ETPUA29 DSPI_C_PCS[2] RCH5_C GPIO[143]	eTPU A channel DSPI C peripheral chip select Reaction channel 5C GPIO	P A1 A2 G	001 010 100 000	143	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	23	F2	L3
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	L4
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	K1
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AA12

Table 5. Signal details (continued)

Signal	Module or Function	Description
$\overline{TA}$	EBI	$\overline{TA}$ is asserted to indicate that the slave has received the data (and completed the access) for a write cycle, or returned data for a read cycle. If the transaction is a burst read, $\overline{TA}$ is asserted for each one of the transaction beats. For write transactions, $\overline{TA}$ is only asserted once at access completion, even if more than one write data beat is transferred.
$\overline{TS}$	EBI	The Transfer Start signal ($\overline{TS}$) is asserted by the MPC5644A to indicate the start of a transfer.
$\overline{WE}$[2:3]	EBI	Write enables are used to enable program operations to a particular memory. $\overline{WE}$[2:3] are only asserted for write accesses
$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	EBI	Write enables are used to enable program operations to a particular memory. These signals can also be used as byte enables for read and write operation by setting the WEBS bit in the appropriate EBI Base Register (EBI_BR*n*). $\overline{WE}$[0:3] are only asserted for write accesses. $\overline{BE}$[0:3] are asserted for both read and write accesses
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
FCK	eQADC	eQADC free running clock for eQADC SSI.
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX SCI_C_RX	eSCI_A - eSCI_C	eSCI receive
SCI_A_TX SCI_B_TX SCI_C_TX	eSCI_A - eSCI_C	eSCI transmit
ETPU_A[0:31]	eTPU	eTPU I/O channel
RCH0_[A:C] RCH1_[A:C] RCH2_[A:C] RCH3_[A:C] RCH4_[A:C] RCH5_[A:C]	eTPU2 Reaction Module	eTPU2 reaction channels. Used to control external actuators, e.g., solenoid control for direct injection systems and valve control in automatic transmissions
TCRCLKA	eTPU2	Input clock for TCR time base

[6] All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

[7] AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

[8] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

[9] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[10] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[11] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Solder profile per IPC/JEDEC J-STD-020D.

[14] Moisture sensitivity per JEDEC test method A112.

3.3 Thermal characteristics

Table 9. Thermal characteristics for 176-pin QFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization.

[2] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[4] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 10. Thermal characteristics for 208-pin MAPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2,3]	One layer board - 1s	39	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2,4]	Four layer board - 2s2p	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2,4]	at 200 ft./min., one layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2,4]	at 200 ft./min., four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 324-pin TEPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	29	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	19	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., single layer board	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., four layer board 2s2p	16	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		10	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		7	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Table 20. Power sequence pin states (medium, slow, and multi-voltage pads)

V_{DDEH}	V_{DD}	Pad State
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

3.8 DC electrical specifications

Table 21. DC electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14		1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62		3.6	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{DDE-EH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{RC33}	SR	—	3.3 V regulated voltage[1]	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75[2]	—	5.25	V
V_{INDC}	SR	—	Analog input voltage	—	V_{SSA}-0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	VRL differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA}-0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage[3]	—	1.14	—	1.32	V
V_{FLASH}[4]	SR	—	Flash read voltage	—	3.0	—	3.6	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
			Keep-out Range: 1.2V–2V	Regulated mode	2.0	—	5.5	

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from Table 23 based on the voltage, frequency, and load on all fast pad pins. The input pin V_{RC33} current can be calculated from Table 23 based on the voltage, frequency, and load on all medium-speed pads. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 23.

Table 23. I/O pad V_{RC33} average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[3] (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV[4] (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	34.9

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3 Average current is for pad configured as output only.

4 In low swing mode, multi-voltage pads must operate in highest slew rate setting.

Table 33. Flash program and erase specifications[1]

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max[2]	Max[3]	Unit
6	$T_{128kpperase}$	CC	P	128 KB Block Pre-program and Erase Time	—	1500	2600	7500	ms
7	$T_{256kpperase}$	CC	P	256 KB Block Pre-program and Erase Time	—	3000	5200	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate[5]	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate [6]	10				ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Page size is 128 bits (4 words).

5 Time between program suspend resume and the next program suspend request.

6 Time between erase suspend resume and the next erase suspend request.

Table 34. Flash module life

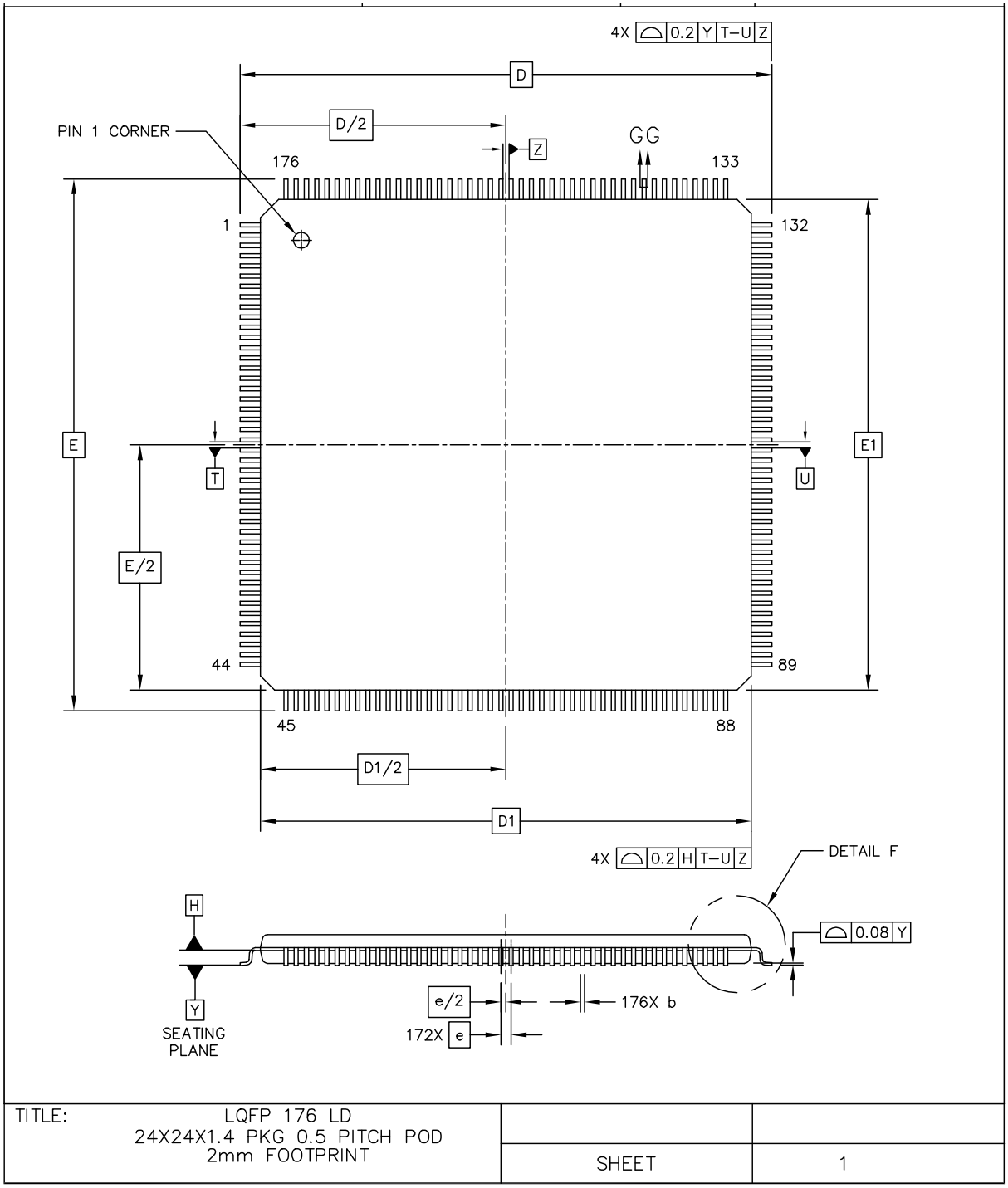
Symbol		C	Parameter	Conditions	Value		Unit
					min	typ	
P/E	CC	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	P/E cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte and 256 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	P/E cycles
Data Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0 – 1,000 P/E cycles	20	—	years
				Blocks with 1,001 – 10,000 P/E cycles	10	—	years
				Blocks with 10,001 – 100,000 P/E cycles	5	—	years

1 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

4 Packages

4.1 Package mechanical data

4.1.1 176 LQFP



NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.6	L1		1 REF					
A1	0.05		0.15	R1	0.08		---				
A2	1.35	1.4	1.45	R2	0.08		0.2				
b	0.17	0.22	0.27	S		0.2 REF					
b1	0.17	0.2	0.23	θ	0°	3.5°	7°				
c	0.09		0.2	θ1	0°		---				
c1	0.09		0.16	θ2	11°	12°	13°				
D		26 BSC		θ3	11°	12°	13°				
D1		24 BSC									
e		0.5 BSC									
E		26 BSC									
E1		24 BSC									
L	0.45	0.6	0.75								

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:		
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT		
	SHEET	3

Figure 35. 176 LQFP package mechanical drawing (part 3)

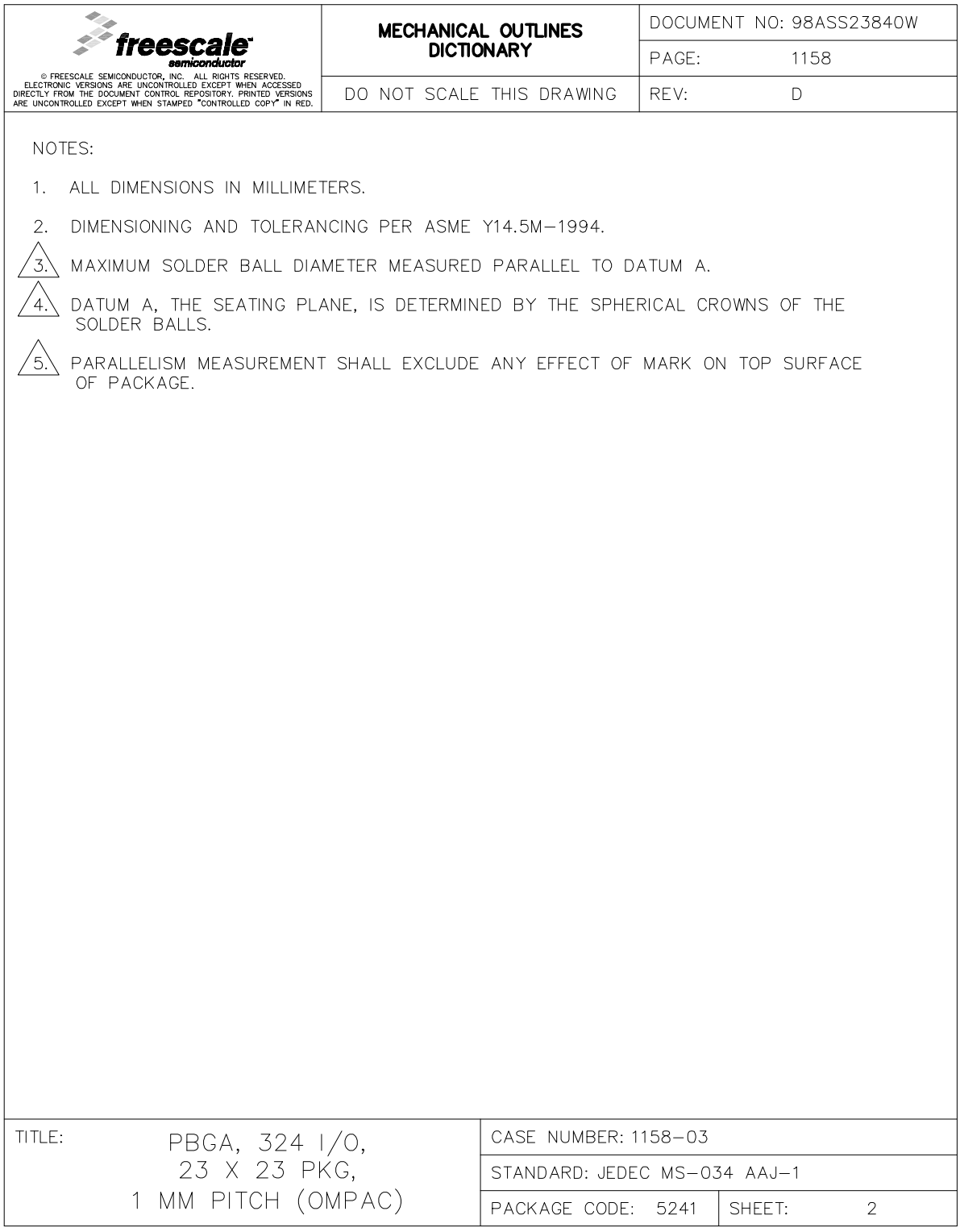


Figure 39. 324 BGA package mechanical drawing (part 2)

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