# STMicroelectronics - STM32F072C8T6 Datasheet

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072c8t6 |

threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

### 3.5.4 Low-power modes

The STM32F072x8/xB microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1, USART2, USB, COMPx, $V_{DDIO2}$ supply comparator or the CEC.

  The CEC, USART1, USART2 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.
- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 4. Internal voltage reference calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA}$= 3.3 V (± 10 mV) | 0x1FFF F7BA - 0x1FFF F7BB |

### 3.10.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the $V_{BAT}$ battery voltage using the internal ADC channel ADC_IN18. As the $V_{BAT}$ voltage may be higher than $V_{DDA}$, and thus outside the ADC input range, the $V_{BAT}$ pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the $V_{BAT}$ voltage.

## 3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

## 3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).Refer to *Table 28: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

### Table 13. STM32F072x8/xB pin definitions (continued)

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | LQFP48/UFQFPN48 | WLCSP49 | | | | | Alternate functions | Additional functions |
| K5 | 33 | H5 | 24 | - | - | PC4 | I/O | TTa | - | EVENTOUT, USART3_TX | ADC_IN14 |
| L5 | 34 | H6 | 25 | - | - | PC5 | I/O | TTa | - | TSC_G3_IO1, USART3_RX | ADC_IN15, WKUP5 |
| M5 | 35 | F5 | 26 | 18 | G5 | PB0 | I/O | TTa | - | TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK | ADC_IN8 |
| M6 | 36 | G5 | 27 | 19 | G4 | PB1 | I/O | TTa | - | TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3 | ADC_IN9 |
| L6 | 37 | G6 | 28 | 20 | G3 | PB2 | I/O | FT | - | TSC_G3_IO4 | - |
| M7 | 38 | - | - | - | - | PE7 | I/O | FT | - | TIM1_ETR | - |
| L7 | 39 | - | - | - | - | PE8 | I/O | FT | - | TIM1_CH1N | - |
| M8 | 40 | - | - | - | - | PE9 | I/O | FT | - | TIM1_CH1 | - |
| L8 | 41 | - | - | - | - | PE10 | I/O | FT | - | TIM1_CH2N | - |
| M9 | 42 | - | - | - | - | PE11 | I/O | FT | - | TIM1_CH2 | - |
| L9 | 43 | - | - | - | - | PE12 | I/O | FT | - | SPI1_NSS, I2S1_WS, TIM1_CH3N | - |
| M10 | 44 | - | - | - | - | PE13 | I/O | FT | - | SPI1_SCK, I2S1_CK, TIM1_CH3 | - |
| M11 | 45 | - | - | - | - | PE14 | I/O | FT | - | SPI1_MISO, I2S1_MCK, TIM1_CH4 | - |
| M12 | 46 | - | - | - | - | PE15 | I/O | FT | - | SPI1_MOSI, I2S1_SD, TIM1_BKIN | - |
| L10 | 47 | G7 | 29 | 21 | E3 | PB10 | I/O | FT | - | SPI2_SCK, I2C2_SCL, USART3_TX, CEC, TSC_SYNC, TIM2_CH3 | - |
| L11 | 48 | H7 | 30 | 22 | G2 | PB11 | I/O | FT | - | USART3_RX, TIM2_CH4, EVENTOUT, TSC_G6_IO1, I2C2_SDA | - |
| F12 | 49 | D5 | 31 | 23 | D3 | VSS | S | - | - | Ground | |

### Table 13. STM32F072x8/xB pin definitions (continued)

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | LQFP48/UFQFPN48 | WLCSP49 | | | | | Alternate functions | Additional functions |
| C10 | 79 | B6 | 52 | - | - | PC11 | I/O | FT | (3) | USART3_RX, USART4_RX | - |
| B10 | 80 | C5 | 53 | - | - | PC12 | I/O | FT | (3) | USART3_CK, USART4_CK | - |
| C9 | 81 | - | - | - | - | PD0 | I/O | FT | (3) | SPI2_NSS, I2S2_WS, CAN_RX | - |
| B9 | 82 | - | - | - | - | PD1 | I/O | FT | (3) | SPI2_SCK, I2S2_CK, CAN_TX | - |
| C8 | 83 | B5 | 54 | - | - | PD2 | I/O | FT | (3) | USART3_RTS, TIM3_ETR | - |
| B8 | 84 | - | - | - | - | PD3 | I/O | FT | - | SPI2_MISO, I2S2_MCK, USART2_CTS | - |
| B7 | 85 | - | - | - | - | PD4 | I/O | FT | - | SPI2_MOSI, I2S2_SD, USART2_RTS | - |
| A6 | 86 | - | - | - | - | PD5 | I/O | FT | - | USART2_TX | - |
| B6 | 87 | - | - | - | - | PD6 | I/O | FT | - | USART2_RX | - |
| A5 | 88 | - | - | - | - | PD7 | I/O | FT | - | USART2_CK | - |
| A8 | 89 | A5 | 55 | 39 | A3 | PB3 | I/O | FT | - | SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT | - |
| A7 | 90 | A4 | 56 | 40 | A4 | PB4 | I/O | FT | - | SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT | - |
| C5 | 91 | C4 | 57 | 41 | B4 | PB5 | I/O | FT | - | SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2 | WKUP6 |
| B5 | 92 | D3 | 58 | 42 | C4 | PB6 | I/O | FTf | - | I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03 | - |

# 5 Memory mapping

To the difference of STM32F072xB memory map in *Figure 10*, the two bottom code memory spaces of STM32F072x8 end at 0x0000 FFFF and 0x0800 FFFF, respectively.

Figure 10. STM32F072xB memory map

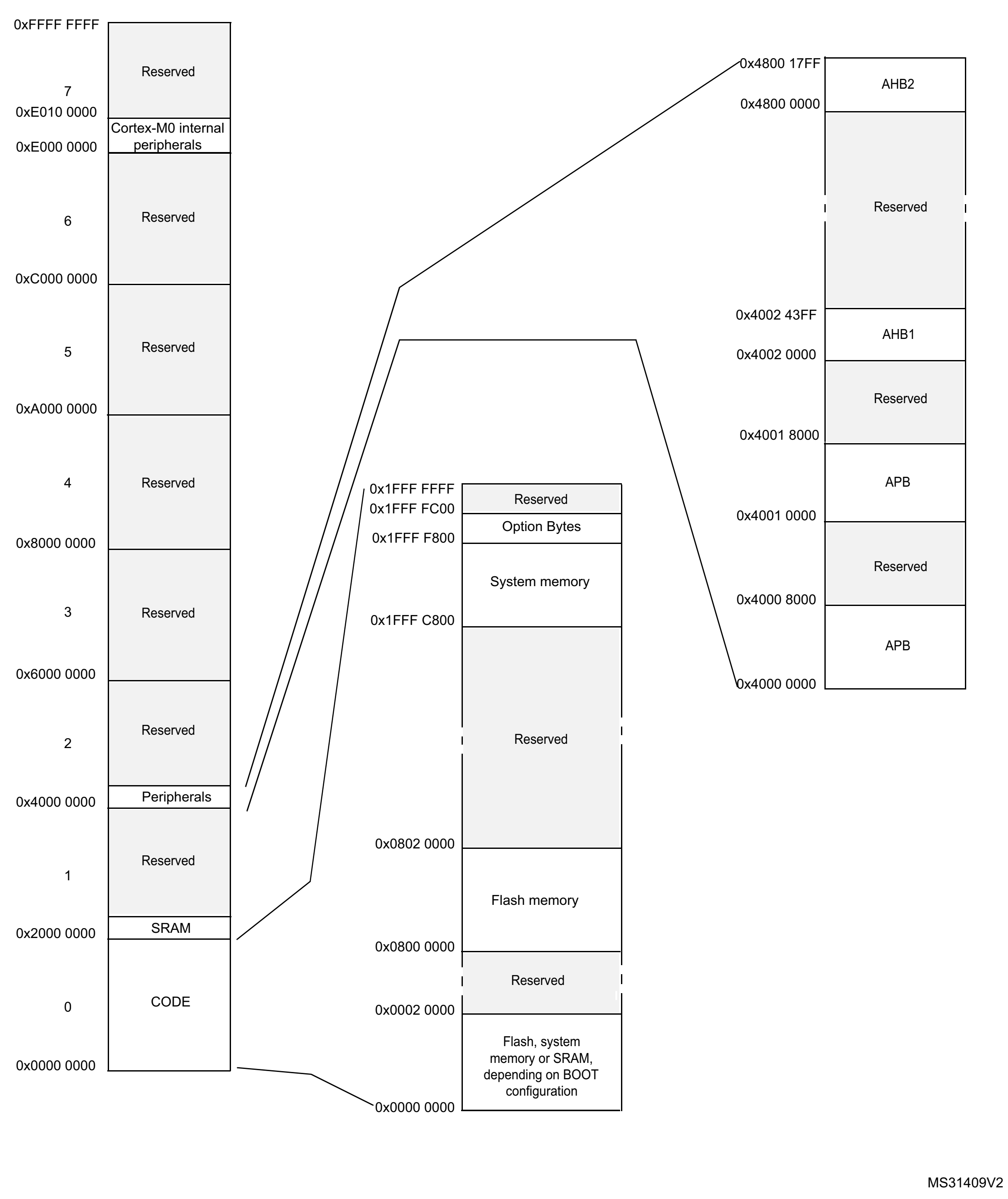


Table 20. STM32F072x8/xB peripheral register boundary addresses

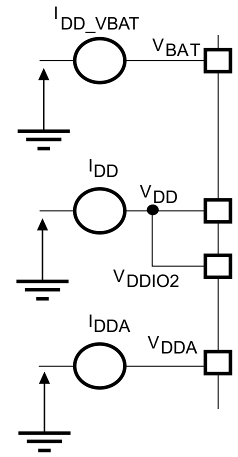
| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| | 0x4800 1800 - 0x5FFF FFFF | ~384 MB | Reserved |
| AHB2 | 0x4800 1400 - 0x4800 17FF | 1 KB | GPIOF |
| | 0x4800 1000 - 0x4800 13FF | 1 KB | GPIOE |
| | 0x4800 0C00 - 0x4800 0FFF | 1 KB | GPIOD |
| | 0x4800 0800 - 0x4800 0BFF | 1 KB | GPIOC |
| | 0x4800 0400 - 0x4800 07FF | 1 KB | GPIOB |
| | 0x4800 0000 - 0x4800 03FF | 1 KB | GPIOA |
| | 0x4002 4400 - 0x47FF FFFF | ~128 MB | Reserved |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 KB | TSC |
| | 0x4002 3400 - 0x4002 3FFF | 3 KB | Reserved |
| | 0x4002 3000 - 0x4002 33FF | 1 KB | CRC |
| | 0x4002 2400 - 0x4002 2FFF | 3 KB | Reserved |
| | 0x4002 2000 - 0x4002 23FF | 1 KB | Flash memory interface |
| | 0x4002 1400 - 0x4002 1FFF | 3 KB | Reserved |
| | 0x4002 1000 - 0x4002 13FF | 1 KB | RCC |
| | 0x4002 0400 - 0x4002 0FFF | 3 KB | Reserved |
| | 0x4002 0000 - 0x4002 03FF | 1 KB | DMA |
| | 0x4001 8000 - 0x4001 FFFF | 32 KB | Reserved |
| APB | 0x4001 5C00 - 0x4001 7FFF | 9 KB | Reserved |
| | 0x4001 5800 - 0x4001 5BFF | 1 KB | DBGMCU |
| | 0x4001 4C00 - 0x4001 57FF | 3 KB | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | 1 KB | TIM17 |
| | 0x4001 4400 - 0x4001 47FF | 1 KB | TIM16 |
| | 0x4001 4000 - 0x4001 43FF | 1 KB | TIM15 |
| | 0x4001 3C00 - 0x4001 3FFF | 1 KB | Reserved |
| | 0x4001 3800 - 0x4001 3BFF | 1 KB | USART1 |
| | 0x4001 3400 - 0x4001 37FF | 1 KB | Reserved |
| | 0x4001 3000 - 0x4001 33FF | 1 KB | SPI1/I2S1 |
| | 0x4001 2C00 - 0x4001 2FFF | 1 KB | TIM1 |
| | 0x4001 2800 - 0x4001 2BFF | 1 KB | Reserved |
| | 0x4001 2400 - 0x4001 27FF | 1 KB | ADC |
| | 0x4001 0800 - 0x4001 23FF | 7 KB | Reserved |
| | 0x4001 0400 - 0x4001 07FF | 1 KB | EXTI |
| | 0x4001 0000 - 0x4001 03FF | 1 KB | SYSCFG + COMP |
| | 0x4000 8000 - 0x4000 FFFF | 32 KB | Reserved |

**Table 20. STM32F072x8/xB peripheral register boundary addresses (continued)**

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| APB | 0x4000 7C00 - 0x4000 7FFF | 1 KB | Reserved |
| | 0x4000 7800 - 0x4000 7BFF | 1 KB | CEC |
| | 0x4000 7400 - 0x4000 77FF | 1 KB | DAC |
| | 0x4000 7000 - 0x4000 73FF | 1 KB | PWR |
| | 0x4000 6C00 - 0x4000 6FFF | 1 KB | CRS |
| | 0x4000 6800 - 0x4000 6BFF | 1 KB | Reserved |
| | 0x4000 6400 - 0x4000 67FF | 1 KB | BxCAN |
| | 0x4000 6000 - 0x4000 63FF | 1 KB | USB/CAN RAM |
| | 0x4000 5C00 - 0x4000 5FFF | 1 KB | USB |
| | 0x4000 5800 - 0x4000 5BFF | 1 KB | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | 1 KB | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | 1 KB | Reserved |
| | 0x4000 4C00 - 0x4000 4FFF | 1 KB | USART4 |
| | 0x4000 4800 - 0x4000 4BFF | 1 KB | USART3 |
| | 0x4000 4400 - 0x4000 47FF | 1 KB | USART2 |
| | 0x4000 3C00 - 0x4000 43FF | 2 KB | Reserved |
| | 0x4000 3800 - 0x4000 3BFF | 1 KB | SPI2 |
| | 0x4000 3400 - 0x4000 37FF | 1 KB | Reserved |
| | 0x4000 3000 - 0x4000 33FF | 1 KB | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 KB | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 KB | RTC |
| | 0x4000 2400 - 0x4000 27FF | 1 KB | Reserved |
| | 0x4000 2000 - 0x4000 23FF | 1 KB | TIM14 |
| | 0x4000 1800 - 0x4000 1FFF | 2 KB | Reserved |
| | 0x4000 1400 - 0x4000 17FF | 1 KB | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6 |
| | 0x4000 0800 - 0x4000 0FFF | 2 KB | Reserved |
| | 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | 1 KB | TIM2 |

### 6.1.7 Current consumption measurement

**Figure 14. Current consumption measurement scheme**



MS31999V2

**Table 33. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal**

| Symbol | Parameter | $f_{HCLK}$ | Typical consumption in Run mode | | Typical consumption in Sleep mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Peripherals enabled | Peripherals disabled | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Current consumption from $V_{DD}$ supply | 48 MHz | 24.1 | 13.5 | 14.6 | 3.5 | mA |
| | | 36 MHz | 18.3 | 10.5 | 11.1 | 2.9 | |
| | | 32 MHz | 16.5 | 9.6 | 10.0 | 2.7 | |
| | | 24 MHz | 12.9 | 7.6 | 7.8 | 2.2 | |
| | | 16 MHz | 8.9 | 5.3 | 5.5 | 1.7 | |
| | | 8 MHz | 4.8 | 3.1 | 3.1 | 1.2 | |
| | | 4 MHz | 3.1 | 2.1 | 2.2 | 1.1 | |
| | | 2 MHz | 2.1 | 1.6 | 1.6 | 1.0 | |
| | | 1 MHz | 1.6 | 1.3 | 1.4 | 1.0 | |
| | | 500 kHz | 1.3 | 1.2 | 1.2 | 1.0 | |
| $I_{DDA}$ | Current consumption from $V_{DDA}$ supply | 48 MHz | 163.3 | | | | µA |
| | | 36 MHz | 124.3 | | | | |
| | | 32 MHz | 111.9 | | | | |
| | | 24 MHz | 87.1 | | | | |
| | | 16 MHz | 62.5 | | | | |
| | | 8 MHz | 2.5 | | | | |
| | | 4 MHz | 2.5 | | | | |
| | | 2 MHz | 2.5 | | | | |
| | | 1 MHz | 2.5 | | | | |
| | | 500 kHz | 2.5 | | | | |

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

#### I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 53: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

### On-chip peripheral current consumption

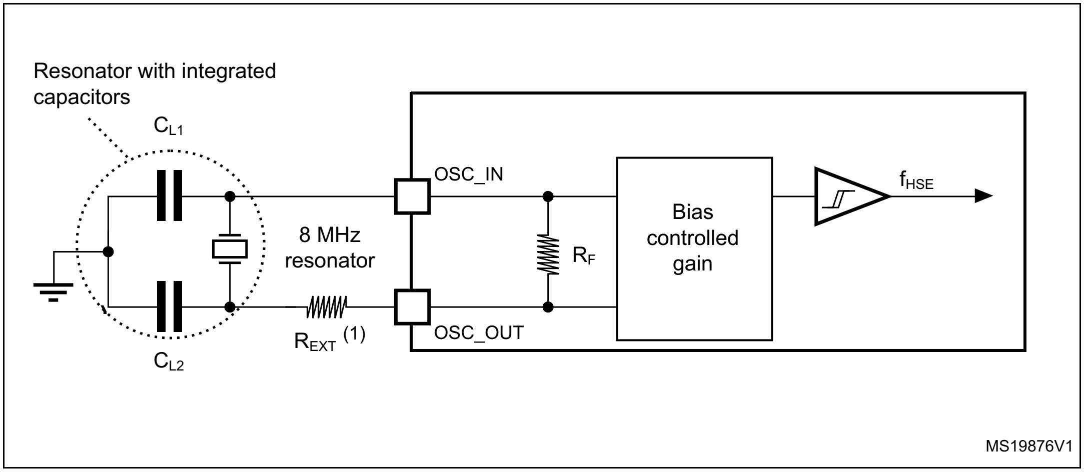
The current consumption of the on-chip peripherals is given in *Table 35*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 21: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 35*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

**Table 35. Peripheral current consumption**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| AHB | BusMatrix[1] | 2.2 | µA/MHz |
| | CRC | 1.6 | |
| | DMA | 5.7 | |
| | Flash memory interface | 13.0 | |
| | GPIOA | 8.2 | |
| | GPIOB | 8.5 | |
| | GPIOC | 2.3 | |
| | GPIOD | 1.9 | |
| | GPIOE | 2.2 | |
| | GPIOF | 1.2 | |
| | SRAM | 0.9 | |
| | TSC | 5.0 | |
| | **All AHB peripherals** | **52.6** | |

Figure 17. Typical application with an 8 MHz crystal



1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | low drive capability | - | 0.5 | 0.9 | µA |
| | | medium-low drive capability | - | - | 1 | |
| | | medium-high drive capability | - | - | 1.3 | |
| | | high drive capability | - | - | 1.6 | |
| $g_m$ | Oscillator transconductance | low drive capability | 5 | - | - | µA/V |
| | | medium-low drive capability | 8 | - | - | |
| | | medium-high drive capability | 15 | - | - | |
| | | high drive capability | 25 | - | - | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DDIOx}$ is stabilized | - | 2 | - | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

### Table 47. Flash memory endurance and data retention

| Symbol | Parameter | Conditions | Min[1] | Unit |
|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = –40 to +105 °C | 10 | kcycle |
| $t_{RET}$ | Data retention | 1 kcycle[2] at $T_A$ = 85 °C | 30 | Year |
| | | 1 kcycle[2] at $T_A$ = 105 °C | 10 | |
| | | 10 kcycle[2] at $T_A$ = 55 °C | 20 | |

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

## 6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

### Table 48. EMS characteristics

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 48 MHz, conforming to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25°C, $f_{HCLK}$ = 48 MHz, conforming to IEC 61000-4-4 | 4B |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 49. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/48 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | -2 | dBµV |
| | | | 30 to 130 MHz | 27 | |
| | | | 130 MHz to 1 GHz | 17 | |
| | | | EMI Level | 4 | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 50. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Packages | Class | Maximum value[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A114 | All | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1 | WLCSP49 | C3 | 250 | V |
| | | | All others | C4 | 500 | |

1. Data based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 51. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DDIOx}$ (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 52*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

**Table 57. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 14 MHz,<br>12-bit resolution | - | - | 823 | kHz |
| | | 12-bit resolution | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | - | 0 | - | $V_{DDA}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* and *Table 58* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2) | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$(2)(3) | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | - | 83 | | | $1/f_{ADC}$ |
| $W_{LATENCY}$(2)(4) | ADC_DR register ready latency | ADC clock = HSI14 | 1.5 ADC cycles + 2 $f_{PCLK}$ cycles | - | 1.5 ADC cycles + 3 $f_{PCLK}$ cycles | - |
| | | ADC clock = PCLK/2 | - | 4.5 | - | $f_{PCLK}$ cycle |
| | | ADC clock = PCLK/4 | - | 8.5 | - | $f_{PCLK}$ cycle |
| $t_{latr}$(2) | Trigger conversion latency | $f_{ADC} = f_{PCLK}/2$ = 14 MHz | 0.196 | | | µs |
| | | $f_{ADC} = f_{PCLK}/2$ | 5.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{PCLK}/4$ = 12 MHz | 0.219 | | | µs |
| | | $f_{ADC} = f_{PCLK}/4$ | 10.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{HSI14}$ = 14 MHz | 0.179 | - | 0.250 | µs |
| $Jitter_{ADC}$ | ADC jitter on trigger conversion | $f_{ADC} = f_{HSI14}$ | - | 1 | - | $1/f_{HSI14}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | - | 17.1 | µs |
| | | - | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Stabilization time | - | 14 | | | $1/f_{ADC}$ |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz,<br>12-bit resolution | 1 | - | 18 | µs |
| | | 12-bit resolution | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on $I_{DDA}$ and 60 µA on $I_{DD}$ should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Figure 30. SPI timing diagram - slave mode and CPHA = 0

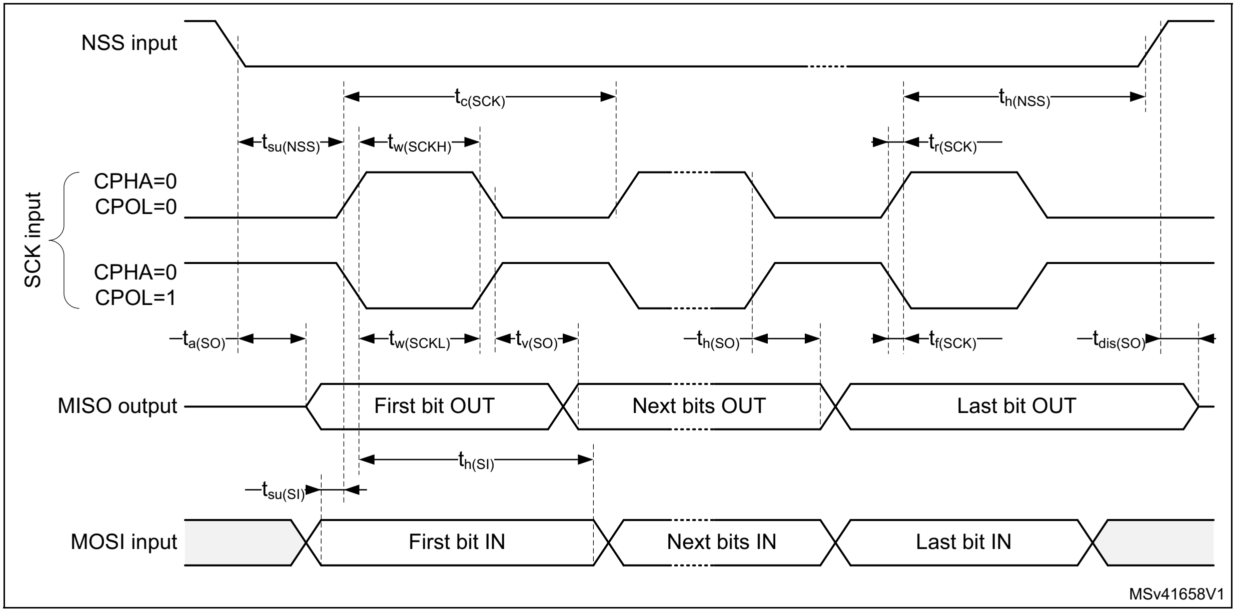
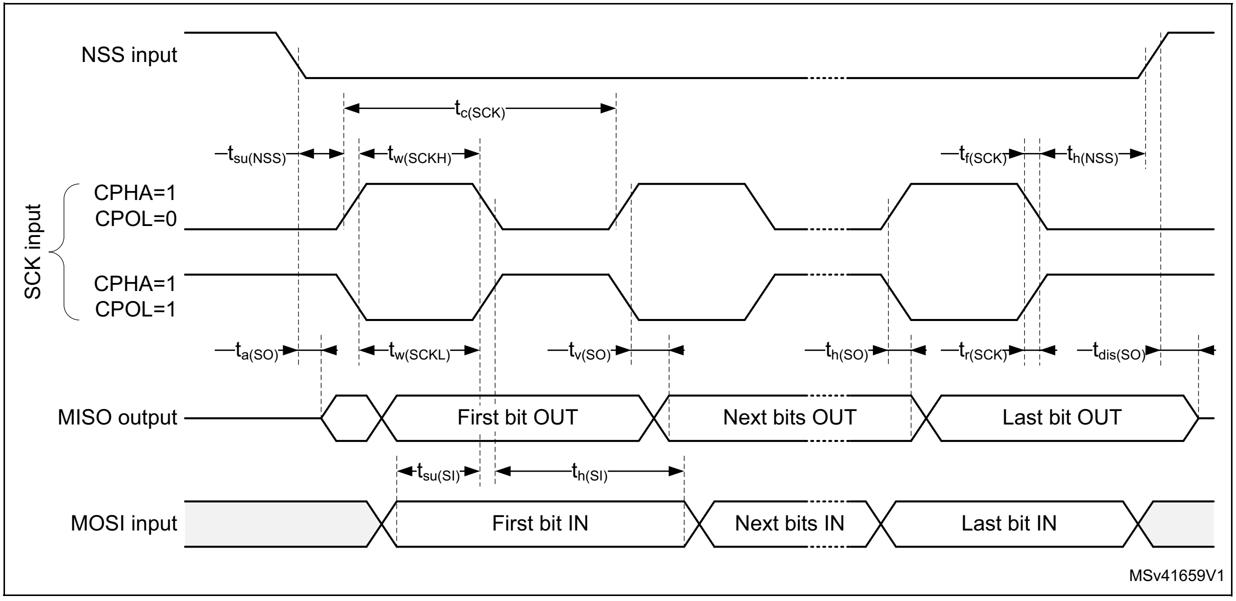


Figure 31. SPI timing diagram - slave mode and CPHA = 1



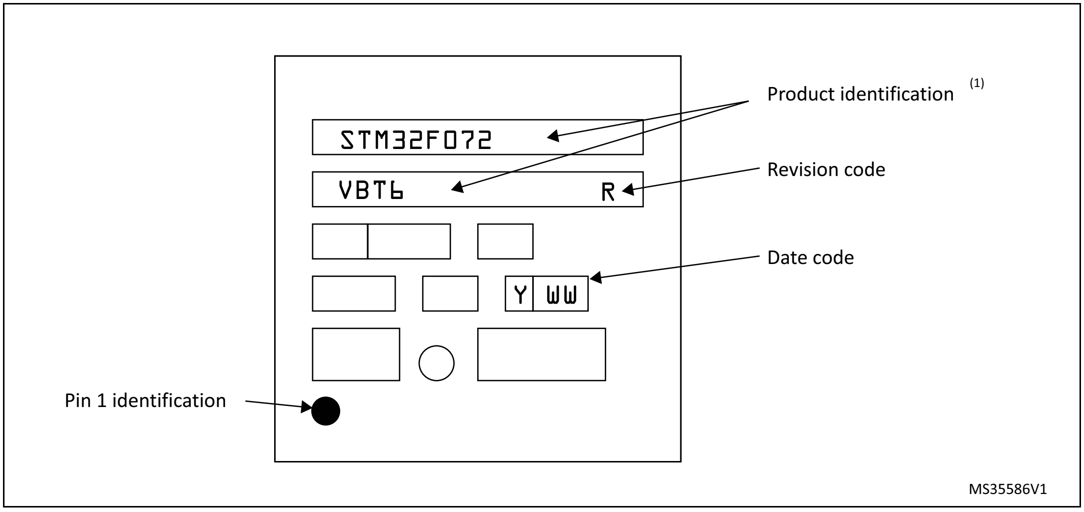
1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 40. LQFP100 package marking example**



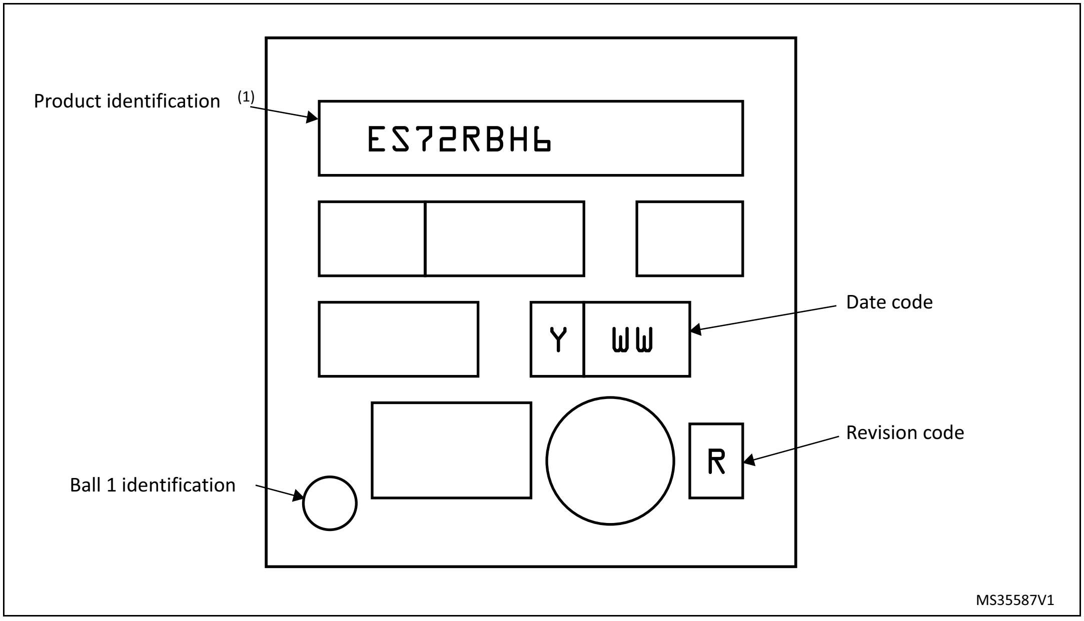
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

### Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 43. UFBGA64 package marking example**



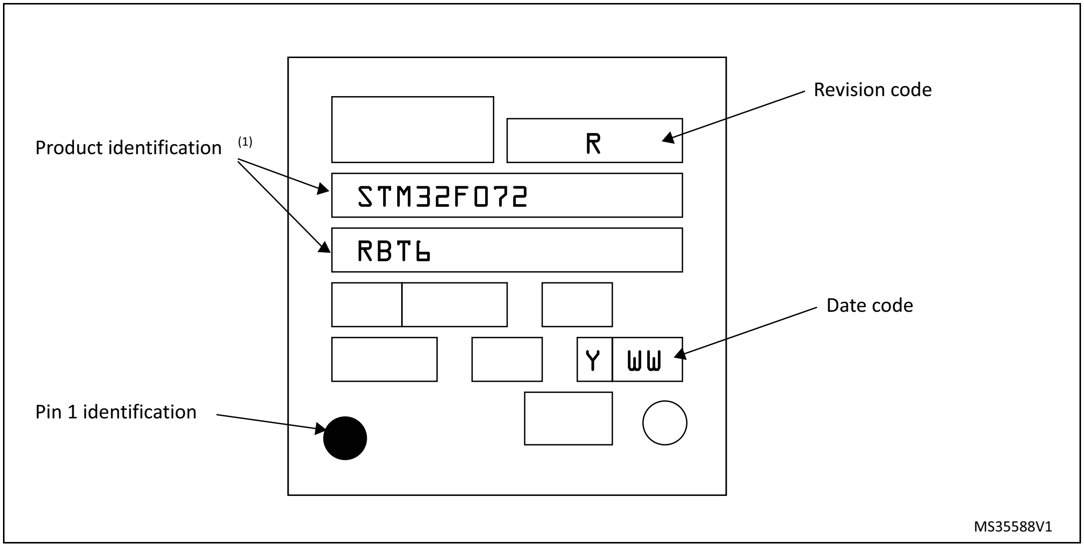
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 46. LQFP64 package marking example**

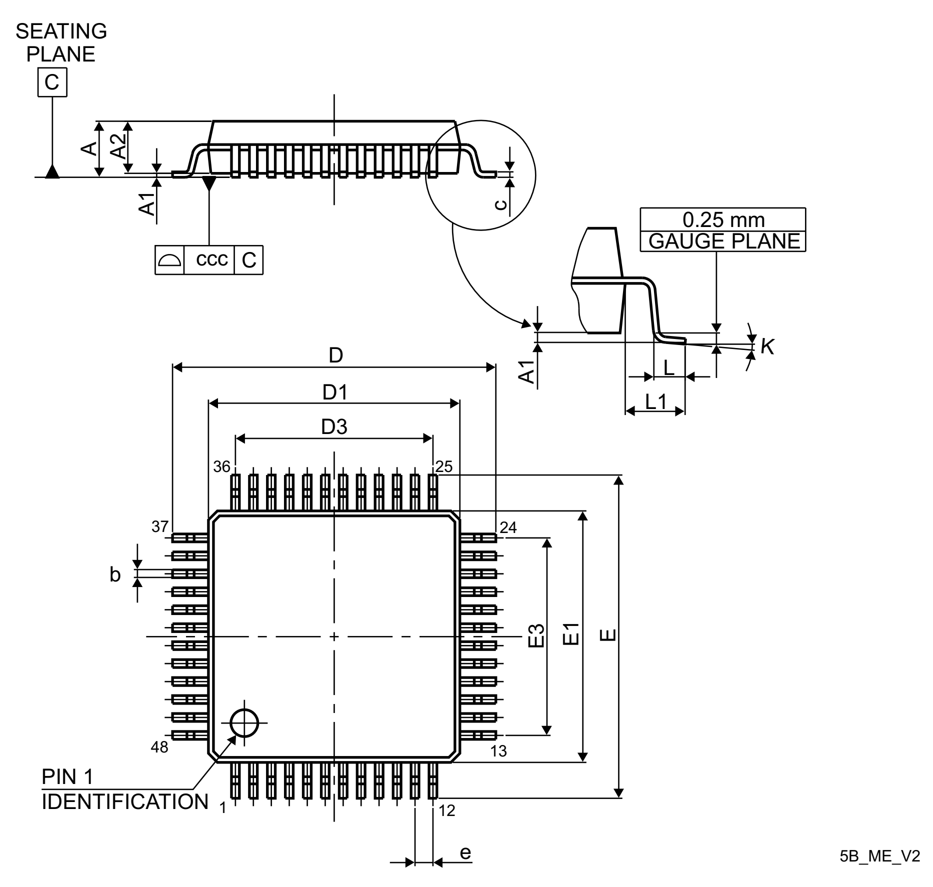


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.6 LQFP48 package information

**LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.**

**Figure 49. LQFP48 package outline**



1. Drawing is not to scale.