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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072c8u6tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F072x8/xB devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
	TSC_G1_IO1	PA0		TSC_G5_IO1	PB3
1	TSC_G1_IO2	PA1	5	TSC_G5_IO2	PB4
1	TSC_G1_IO3	PA2	5	TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
	TSC_G2_IO1	PA4		TSC_G6_IO1	PB11
2	TSC_G2_IO2	PA5	6	TSC_G6_IO2	PB12
2	TSC_G2_IO3	PA6	0	TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
a	TSC_G3_IO1	PC5		TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0	7	TSC_G7_IO2	PE3
5	TSC_G3_IO3	PB1	/	TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9		TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10	8	TSC_G8_IO2	PD13
	TSC_G4_IO3	PA11	0	TSC_G8_IO3	PD14
	TSC_G4_IO4	PA12		TSC_G8_IO4	PD15

Table 5. Capacitive sensing GPIOs available on STM32F072x8/xB devices

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TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.



USART modes/features ⁽¹⁾	USART1 and USART2	USART3 and USART4
IrDA SIR ENDEC block	Х	-
LIN mode	Х	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	Х	-
Auto baud rate detection	Х	-
Driver Enable	X	Х

Table 10. STM32F072x8/xB USART ir	mplementation (continued)

1. X = supported.

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I²S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F0	72x8/xB SPI/I ² S	implementation
-------------------	------------------------------	----------------

SPI features ⁽¹⁾	SPI1 and SPI2
Hardware CRC calculation	Х
Rx/Tx FIFO	Х
NSS pulse mode	Х
I ² S mode	Х
TI mode	Х

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory



Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	-
PE8	TIM1_CH1N	-
PE9	TIM1_CH1	-
PE10	TIM1_CH2N	-
PE11	TIM1_CH2	-
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Table 19. Alternate functions available on port F

	•
Pin name	AF
PF0	CRS_SYNC
PF1	-
PF2	EVENTOUT
PF3	EVENTOUT
PF6	-
PF9	TIM15_CH1
PF10	TIM15_CH2



5 Memory mapping

To the difference of STM32F072xB memory map in *Figure 10*, the two bottom code memory spaces of STM32F072x8 end at 0x0000 FFFF and 0x0800 FFFF, respectively.



Figure 10. STM32F072xB memory map



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Symbol	Ratings	Max.	Unit
ΣI _{VDD}	Total current into sum of all VDD power lines (source) ⁽¹⁾	120	
ΣI _{VSS}	Total current out of sum of all VSS ground lines (sink) ⁽¹⁾	-120	
I _{VDD(PIN)}	Maximum current into each VDD power pin (source) ⁽¹⁾	100	
I _{VSS(PIN)}	Maximum current out of each VSS ground pin (sink) ⁽¹⁾	-100	
	Output current sunk by any I/O and control pin	25	
I _{IO(PIN)}	Output current source by any I/O and control pin	-25	
	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	80	
ΣΙ _{ΙΟ(ΡΙΝ)}	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-80	mA
	Total output current sourced by sum of all I/Os supplied by VDDIO2	-40	
I _{INJ(PIN)} ⁽³⁾	Injected current on B, FT and FTf pins	-5/+0 ⁽⁴⁾	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins ⁽⁵⁾	± 5	
ΣI _{INJ(PIN)}	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	1

Table 22. Current characteristics

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.

A positive injection is induced by V_{IN} > V_{DDIOx} while a negative injection is induced by V_{IN} < V_{SS}. I_{INJ(PIN)} must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.

4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below *Table 59: ADC accuracy*.

6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	–65 to +150	°C
TJ	Maximum junction temperature	150	°C



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 35*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 21: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 35.* The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Peripheral		Typical consumption at 25 °C	Unit
	BusMatrix ⁽¹⁾	2.2	
	CRC	1.6	
	DMA	5.7	
	Flash memory interface	13.0	
	GPIOA GPIOB	8.2	
AHB		8.5	
	GPIOC	2.3	µA/MHz
	GPIOD	1.9	
	GPIOE	2.2	
	GPIOF	1.2	
	SRAM	0.9	
	TSC	5.0	
	All AHB peripherals	52.6	

Table 35. Peripheral current consumption



	Peripheral	Typical consumption at 25 °C	Unit
	APB-Bridge ⁽²⁾	2.8	
	ADC ⁽³⁾	4.1	
	CAN	12.4	
	CEC	1.5	
	CRS	0.8	
	DAC ⁽³⁾	4.7	
	DEBUG (MCU debug feature)	0.1	
	I2C1	3.9	
	I2C2	4.0	
	PWR	1.3	
	SPI1	8.7	
	SPI2	8.5	
	SYSCFG & COMP	1.7	
	TIM1	14.9	
	TIM2	15.5	
APB	TIM3	11.4	µA/MHz
	TIM6	2.5	
	TIM7	2.3	
	TIM14	5.3	
	TIM15	9.1	
	TIM16	6.6	
	TIM17	6.8	
	USART1	17.0	
	USART2	16.7	
	USART3	5.4	
	USART4	5.4	
	USB	7.2	
	WWDG	1.4	
	All APB peripherals	182	

Table 35. Peripheral current consumption (continued)

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).

2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.

 The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, is not included. Refer to the tables of characteristics in the subsequent sections.



······································								
Symbol	Ratings	Conditions	Packages	Class	Maximum value ⁽¹⁾	Unit		
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V		
V.	Electrostatic discharge voltage	$T_A = +25 ^{\circ}C$, conforming	WLCSP49	C3	250	V		
VESD(CDM)	(charge device model)	to ANSI/ESD STM5.3.1	All others	C4	500			

 Table 50. ESD absolute maximum ratings

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 51	Electrical	sensitivities
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Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105 \text{ °C conforming to JESD78A}$	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μ A/+0 μ A range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 52*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.



Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
l _{ikg} i		TC, FT and FTf I/O TTa in digital mode V _{SS} ≤ V _{IN} ≤ V _{DDIOx}	-	-	± 0.1	
	Input leakage	TTa in digital mode V _{DDIOx} ≤ V _{IN} ≤ V _{DDA}	-	-	1	μA
		TTa in analog mode V _{SS} ≤ V _{IN} ≤ V _{DDA}	-	-	± 0.2	
		FT and FTf I/O V _{DDIOx} ≤ V _{IN} ≤ 5 V	-	-	10	
R _{PU}	Weak pull-up equivalent resistor (3)	V _{IN} = V _{SS}	25	40	55	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽³⁾	V _{IN} = - V _{DDIOx}	25	40	55	kΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

Table 53. I/O static characteristics (continued)
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1. Data based on design simulation only. Not tested in production.

2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 52: I/O current injection susceptibility.*

 Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.



OSPEEDRy [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	2	MHz
Fm+	t _{f(IO)out}	Output fall time	$C_L = 50 \text{ pF}, V_{DDIOx} \ge 2 \text{ V}$	-	12	
	t _{r(IO)out}	Output rise time			34	115
(4)	f _{max(IO)out}	Maximum frequency ⁽³⁾		-	0.5	MHz
	t _{f(IO)out}	Output fall time	C _L = 50 pF, V _{DDIOx} < 2 V	-	16	200
	t _{r(IO)out}	Output rise time		-	44	115
-	t _{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

Table 55. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

 The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.

2. Guaranteed by design, not tested in production.

- 3. The maximum frequency is defined in *Figure 24*.
- 4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.



Figure 24. I/O AC characteristics definition

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, $\mathsf{R}_{\mathsf{PU}}.$

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{IL(NRST)}	NRST input low level voltage	-	-	-	0.3 V _{DD} +0.07 ⁽¹⁾	V
V _{IH(NRST)}	NRST input high level voltage	-	0.445 V _{DD} +0.398 ⁽¹⁾	-	-	v

Table 56. NRST pin characteristics



Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_{S}}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 58. RAIN max for fADC = 14 MHz					
T _s (cycles)	t _S (μs)	R _{AIN} max (kΩ) ⁽¹⁾			
1.5	0.11	0.4			
7.5	0.54	5.9			
13.5	0.96	11.4			
28.5	2.04	25.2			
41.5	2.96	37.2			
55.5	3.96	50			
71.5	5.11	NA			
239.5	17.1	NA			

1. Guaranteed by design, not tested in production.

Table 59. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Test conditions	Тур	Max ⁽⁴⁾	Unit
ET	Total unadjusted error		±1.3	±2	
EO	Offset error	f _{PCLK} = 48 MHz,	±1	±1.5	
EG	Gain error	$T_{ADC} = 14 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega$	±0.5	±1.5	LSB
ED	Differential linearity error	$T_A = 25 \text{ °C}$	±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error		±3.3	±4	
EO	Offset error	f _{PCLK} = 48 MHz,	±1.9	±2.8	
EG	Gain error	$f_{ADC} = 14 \text{ MHZ}, R_{AIN} < 10 \text{ k}\Omega$	±2.8	±3	LSB
ED	Differential linearity error	$T_A = -40$ to 105 °C	±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error		±3.3	±4	
EO	Offset error	f _{PCLK} = 48 MHz,	±1.9	±2.8	
EG	Gain error	$T_{ADC} = 14 \text{ MHz}, R_{AIN} < 10 \text{ k}\Omega$	±2.8	±3	LSB
ED	Differential linearity error	$T_A = 25 \text{°C}$	±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.



6.3.18 Comparator characteristics

Symbol	Parameter	Conditio	ons	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
V _{DDA}	Analog supply voltage	-		V _{DD}	-	3.6	V
V _{IN}	Comparator input voltage range	-		0	-	V _{DDA}	-
V _{SC}	V _{REFINT} scaler offset voltage	-			±5	±10	mV
ts sc	V _{REFINT} scaler startup	First V _{REFINT} scaler activation after device power on		-	-	1000 (2)	ms
0_00	time from power down	Next activations		-	-	0.2	
t _{START}	Comparator startup time	Startup time to reach pro specification	pagation delay	-	-	60	μs
		Ultra-low power mode		-	2	4.5	
	Propagation delay for 200 mV step with 100 mV overdrive	Low power mode		-	0.7	1.5	μs
		Medium power mode		-	0.3	0.6	
		High speed mode	V _{DDA} ≥2.7 V	-	50	100	- ns
+			V _{DDA} < 2.7 V	-	100	240	
۲D		Ultra-low power mode		-	2	7	
	Propagation delay for	Low power mode		-	0.7	2.1	μs
	full range step with	Medium power mode		-	0.3	1.2	
	100 mV overdrive	High speed mode	V _{DDA} ≥ 2.7 V	-	90	180	
		nigh speed mode	V _{DDA} < 2.7 V	-	110	300	115
V _{offset}	Comparator offset error	-		-	±4	±10	mV
dV _{offset} /dT	Offset error temperature coefficient	-		-	18	-	µV/°C
		Ultra-low power mode		-	1.2	1.5	
	COMP current	Low power mode		-	3	5	114
יDD(COMP)	consumption	Medium power mode		-	10	15	μΑ
		High speed mode		-	75	100	

Table 61. Comparator characteristics



Symbol	Parameter	Min	Max	Unit
t _{AF}	Maximum width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

Table 67. I²C analog filter characteristics⁽¹⁾

1. Guaranteed by design, not tested in production.

- 2. Spikes with widths below $t_{AF(min)}$ are filtered.
- 3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 68* for SPI or in *Table 69* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*.

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Symbol	Parameter	Conditions	Min	Мах	Unit
f _{SCK}	SDI clock froguency	Master mode	-	18	
1/t _{c(SCK)}	SPI Clock frequency	Slave mode	-	18	
t _{r(SCK)} t _{f(SCK)}	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
t _{su(NSS)}	NSS setup time	Slave mode	4Tpclk	-	
t _{h(NSS)}	NSS hold time	Slave mode	2Tpclk + 10	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode, f _{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
t _{su(MI)}	Data input satur timo	Master mode	4	-	
t _{su(SI)}	Data input setup time	Slave mode	5	-	
t _{h(MI)}	Data input hold time	Master mode	4	-	
t _{h(SI)}		Slave mode	5	-	ns
t _{a(SO)} ⁽²⁾	Data output access time	Slave mode, f _{PCLK} = 20 MHz	0	3Tpclk	
t _{dis(SO)} ⁽³⁾	Data output disable time	Slave mode	0	18	
t _{v(SO)}	Data output valid time	Slave mode Slave mode, f _{PCLK} = 20 MHz Slave mode Slave mode Slave mode (after enable edge) Master mode (after enable edge)		22.5	
t _{v(MO)}	Data output valid time	Master mode (after enable edge)	-	6	
t _{h(SO)}	Data output hold time	Slave mode (after enable edge)	11.5	-	
t _{h(MO)}		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle Slave mode		25	75	%

Table 68. SPI characteristics ^{(*}

1. Data based on characterization results, not tested in production.

2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z





Figure 30. SPI timing diagram - slave mode and CPHA = 0





1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

7.1 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.



Figure 35. UFBGA100 package outline

1. Drawing is not to scale.

Table 71. UFBGA100	package mechanical data
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Symbol	millimeters			inches ⁽¹⁾		
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-



7.4 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.



Figure 44. LQFP64 package outline

1. Drawing is not to scale.

Fable 76. LQF	P64 package	mechanical	data
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Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-



7.6 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.





1. Drawing is not to scale.



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.



Figure 54. UFQFPN48 package marking example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

