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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072cbt6tr

Contents

1	Introduction	9
2	Description	10
3	Functional overview	13
3.1	ARM®-Cortex®-M0 core	13
3.2	Memories	13
3.3	Boot modes	13
3.4	Cyclic redundancy check calculation unit (CRC)	14
3.5	Power management	14
3.5.1	Power supply schemes	14
3.5.2	Power supply supervisors	14
3.5.3	Voltage regulator	15
3.5.4	Low-power modes	15
3.6	Clocks and startup	15
3.7	General-purpose inputs/outputs (GPIOs)	17
3.8	Direct memory access controller (DMA)	17
3.9	Interrupts and events	17
3.9.1	Nested vectored interrupt controller (NVIC)	17
3.9.2	Extended interrupt/event controller (EXTI)	18
3.10	Analog-to-digital converter (ADC)	18
3.10.1	Temperature sensor	18
3.10.2	Internal voltage reference (V_{REFINT})	18
3.10.3	V_{BAT} battery voltage monitoring	19
3.11	Digital-to-analog converter (DAC)	19
3.12	Comparators (COMP)	19
3.13	Touch sensing controller (TSC)	20
3.14	Timers and watchdogs	21
3.14.1	Advanced-control timer (TIM1)	22
3.14.2	General-purpose timers (TIM2, 3, 14, 15, 16, 17)	22
3.14.3	Basic timers TIM6 and TIM7	23
3.14.4	Independent watchdog (IWDG)	23
3.14.5	System window watchdog (WWDG)	23

6.3.10	Memory characteristics	74
6.3.11	EMC characteristics	75
6.3.12	Electrical sensitivity characteristics	76
6.3.13	I/O current injection characteristics	77
6.3.14	I/O port characteristics	78
6.3.15	NRST pin characteristics	83
6.3.16	12-bit ADC characteristics	84
6.3.17	DAC electrical specifications	88
6.3.18	Comparator characteristics	90
6.3.19	Temperature sensor characteristics	92
6.3.20	V _{BAT} monitoring characteristics	92
6.3.21	Timer characteristics	92
6.3.22	Communication interfaces	93
7	Package information	100
7.1	UFBGA100 package information	100
7.2	LQFP100 package information	103
7.3	UFBGA64 package information	106
7.4	LQFP64 package information	109
7.5	WLCSP49 package information	112
7.6	LQFP48 package information	115
7.7	UFQFPN48 package information	118
7.8	Thermal characteristics	121
7.8.1	Reference document	121
7.8.2	Selecting the product temperature range	121
8	Ordering information	124
9	Revision history	125

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 7-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

Table 6. Number of capacitive sensing channels available on STM32F072x8/xB devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F072Vx	STM32F072Rx	STM32F072Cx
G1	3	3	3
G2	3	3	3
G3	3	3	2
G4	3	3	3
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	24	18	17

3.14 Timers and watchdogs

The STM32F072x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

[Table 7](#) compares the features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

Table 13. STM32F072x8/xB pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	LQFP48/UFQFPN48	WLCSP49					Alternate functions	Additional functions
D11	67	D7	41	29	D1	PA8	I/O	FT	(3)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC	-
D10	68	C7	42	30	D2	PA9	I/O	FT	(3)	USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	-
C12	69	C6	43	31	C2	PA10	I/O	FT	(3)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	-
B12	70	C8	44	32	C1	PA11	I/O	FT	(3)	CAN_RX, USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	USB_DM
A12	71	B8	45	33	C3	PA12	I/O	FT	(3)	CAN_TX, USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT	USB_DP
A11	72	A8	46	34	B3	PA13	I/O	FT	(3) (4)	IR_OUT, SWDIO, USB_NOE	-
C11	73	-	-	-	-	PF6	I/O	FT	(3)	-	-
F11	74	D6	47	35	B1	VSS	S	-	-	Ground	
G11	75	E6	48	36	B2	VDDIO2	S	-	-	Digital power supply	
A10	76	A7	49	37	A1	PA14	I/O	FT	(3) (4)	USART2_TX, SWCLK	-
A9	77	A6	50	38	A2	PA15	I/O	FT	(3)	SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT	-
B11	78	B7	51	-	-	PC10	I/O	FT	(3)	USART3_TX, USART4_TX	-



Table 15. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	USART3_CK	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	USART3_RTS	-
PB2	-	-	-	TSC_G3_IO4	-	-
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	-	-
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	-	TIM17_BKIN
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	USART4_CTS	-
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC	CAN_RX	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS, I2S2_WS
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC	USART3_TX	SPI2_SCK, I2S2_CK
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1	USART3_RX	-
PB12	SPI2_NSS, I2S2_WS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2	USART3_CK	TIM15_BKIN
PB13	SPI2_SCK, I2S2_CK	-	TIM1_CH1N	TSC_G6_IO3	USART3_CTS	I2C2_SCL
PB14	SPI2_MISO, I2S2_MCK	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI, I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

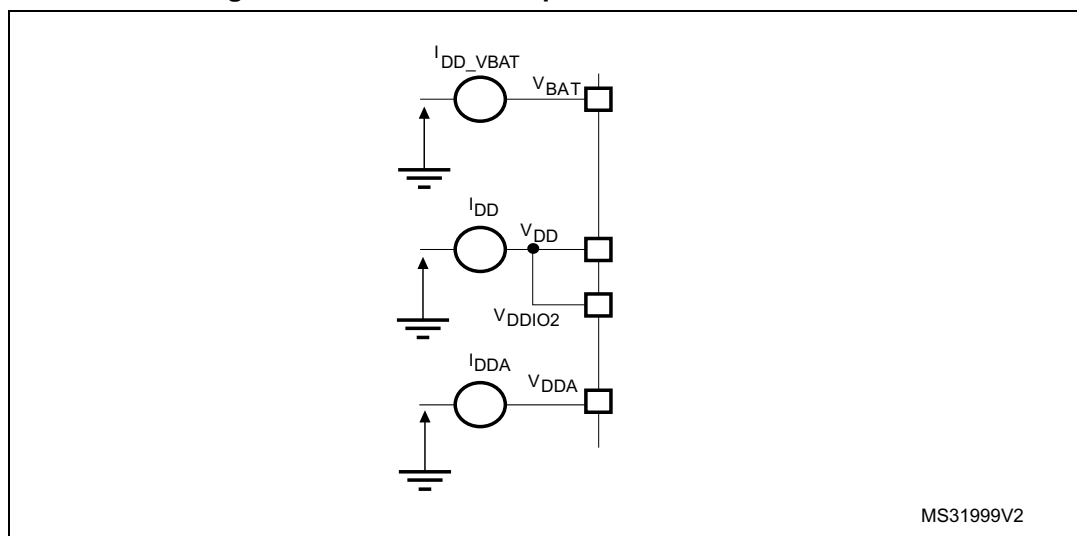
Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	-
PE8	TIM1_CH1N	-
PE9	TIM1_CH1	-
PE10	TIM1_CH2N	-
PE11	TIM1_CH2	-
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 19. Alternate functions available on port F

Pin name	AF
PF0	CRS_SYNC
PF1	-
PF2	EVENTOUT
PF3	EVENTOUT
PF6	-
PF9	TIM15_CH1
PF10	TIM15_CH2

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.3 Operating conditions

6.3.1 General operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.0	3.6	V
V_{DDIO2}	I/O supply voltage	Must not be supplied if V_{DD} is not present	1.65	3.6	V
V_{DDA}	Analog operating voltage (ADC and DAC not used)	Must have a potential equal to or higher than V_{DD}	V_{DD}	3.6	V
	Analog operating voltage (ADC and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	$V_{DDIOx}+0.3$	V
		TTa I/O	-0.3	$V_{DDA}+0.3^{(1)}$	
		FT and FTf I/O	-0.3	$5.5^{(1)}$	
		BOOT0	0	5.5	
P_D	Power dissipation at $T_A = 85\text{ }^{\circ}\text{C}$ for suffix 6 or $T_A = 105\text{ }^{\circ}\text{C}$ for suffix 7 ⁽²⁾	UFBGA100	-	364	mW
		LQFP100	-	476	
		UFBGA64	-	308	
		LQFP64	-	455	
		LQFP48	-	370	
		UFQFPN48	-	625	
		WLCSP49	-	408	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	$^{\circ}\text{C}$
		Low power dissipation ⁽³⁾	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	$^{\circ}\text{C}$
		Low power dissipation ⁽³⁾	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	$^{\circ}\text{C}$
		Suffix 7 version	-40	125	

- For operation with a voltage higher than $V_{DDIOx} + 0.3\text{ V}$, the internal pull-up resistor must be disabled.
- If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} . See [Section 7.8: Thermal characteristics](#).
- In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see [Section 7.8: Thermal characteristics](#)).

Table 29. Typical and maximum current consumption from V_{DD} supply at $V_{DD} = 3.6\text{ V}$ (continued)

Symbol	Parameter	Conditions	f _{HCLK}	All peripherals enabled ⁽¹⁾				All peripherals disabled				Unit
				Typ	Max @ T _A ⁽²⁾			Typ	Max @ T _A ⁽²⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DD}	Supply current in Run mode, code executing from RAM	HSI48	48 MHz	23.1	25.4	25.8	26.6	12.8	13.5	13.7	13.9	mA
		HSE bypass, PLL on	48 MHz	23.0	25.3 ⁽³⁾	25.7	26.5 ⁽³⁾	12.6	13.3 ⁽³⁾	13.5	13.8 ⁽³⁾	
			32 MHz	15.4	17.3	17.8	18.3	7.96	8.92	9.17	9.73	
			24 MHz	11.4	12.9	13.5	13.7	6.48	8.04	8.23	8.41	
		HSE bypass, PLL off	8 MHz	4.21	4.6	4.89	5.25	2.07	2.3	2.35	2.94	
			1 MHz	0.78	0.9	0.92	1.15	0.36	0.48	0.59	0.82	
		HSI clock, PLL on	48 MHz	23.1	24.5	25.0	25.2	12.6	13.7	13.9	14.0	
			32 MHz	15.4	17.4	17.7	18.2	8.05	8.85	9.16	9.94	
			24 MHz	11.5	13.0	13.6	13.9	6.49	8.06	8.21	8.47	
		HSI clock, PLL off	8 MHz	4.34	4.75	5.03	5.41	2.11	2.36	2.38	2.98	
	Supply current in Sleep mode	HSI48	48 MHz	15.1	16.6	16.8	17.5	3.08	3.43	3.56	3.61	
		HSE bypass, PLL on	48 MHz	15.0	16.5 ⁽³⁾	16.7	17.3 ⁽³⁾	2.93	3.28 ⁽³⁾	3.41	3.46 ⁽³⁾	
			32 MHz	9.9	11.4	11.6	11.9	2.0	2.24	2.32	2.49	
			24 MHz	7.43	8.17	8.71	8.82	1.63	1.82	1.88	1.9	
		HSE bypass, PLL off	8 MHz	2.83	3.09	3.26	3.66	0.76	0.88	0.91	0.93	
			1 MHz	0.42	0.54	0.55	0.67	0.28	0.39	0.41	0.43	
		HSI clock, PLL on	48 MHz	15.0	17.2	17.3	17.9	3.04	3.37	3.41	3.46	
			32 MHz	9.93	11.3	11.6	11.7	2.11	2.35	2.44	2.65	
			24 MHz	7.53	8.45	8.87	8.95	1.64	1.83	1.9	1.93	
		HSI clock, PLL off	8 MHz	2.95	3.24	3.41	3.8	0.8	0.92	0.94	0.97	

1. USB is kept disabled as this IP functions only with a 48 MHz clock.

2. Data based on characterization results, not tested in production unless otherwise specified.

3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

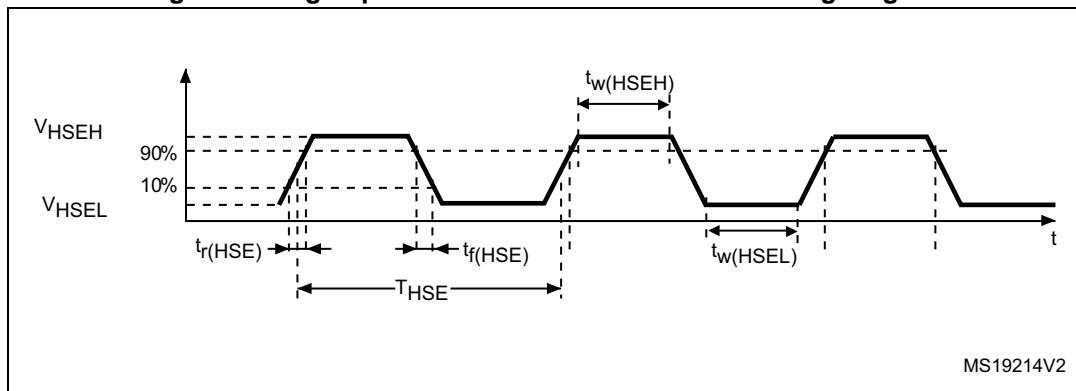
Table 34. Switching output I/O current consumption

Symbol	Parameter	Conditions ⁽¹⁾	I/O toggling frequency (f _{SW})	Typ	Unit
I _{sw}	I/O current consumption	V _{DDIOx} = 3.3 V C = C _{INT}	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V _{DDIOx} = 3.3 V C _{EXT} = 0 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V _{DDIOx} = 3.3 V C _{EXT} = 10 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V _{DDIOx} = 3.3 V C _{EXT} = 22 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V _{DDIOx} = 3.3 V C _{EXT} = 33 pF C = C _{INT} + C _{EXT} + C _S	4 MHz	0.64	
			8 MHz	1.25	
			16 MHz	3.24	
			24 MHz	5.02	
		V _{DDIOx} = 3.3 V C _{EXT} = 47 pF C = C _{INT} + C _{EXT} + C _S C = C _{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	
		V _{DDIOx} = 2.4 V C _{EXT} = 47 pF C = C _{INT} + C _{EXT} + C _S C = C _{int}	4 MHz	0.66	
			8 MHz	1.43	
			16 MHz	2.45	
			24 MHz	4.97	

1. C_S = 7 pF (estimated value).

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

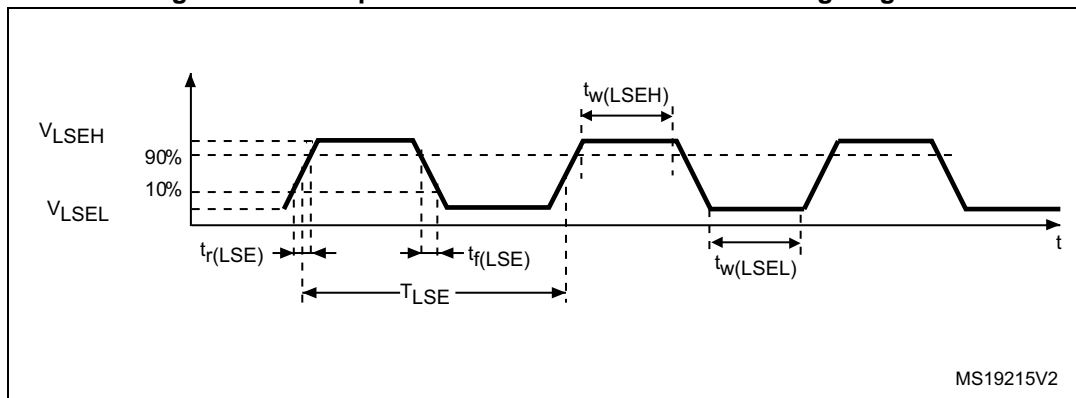
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 16](#).

Table 38. Low-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7 V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	$0.3 V_{DDIOx}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram



2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 6.3.14](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA} , frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 26. ADC accuracy characteristics

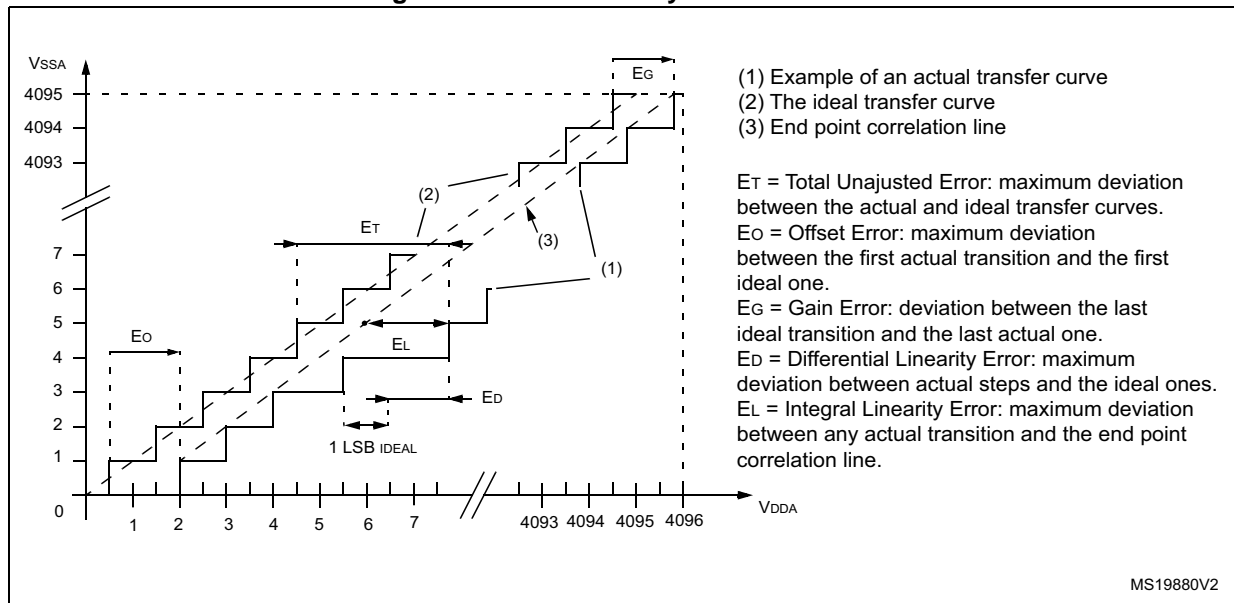
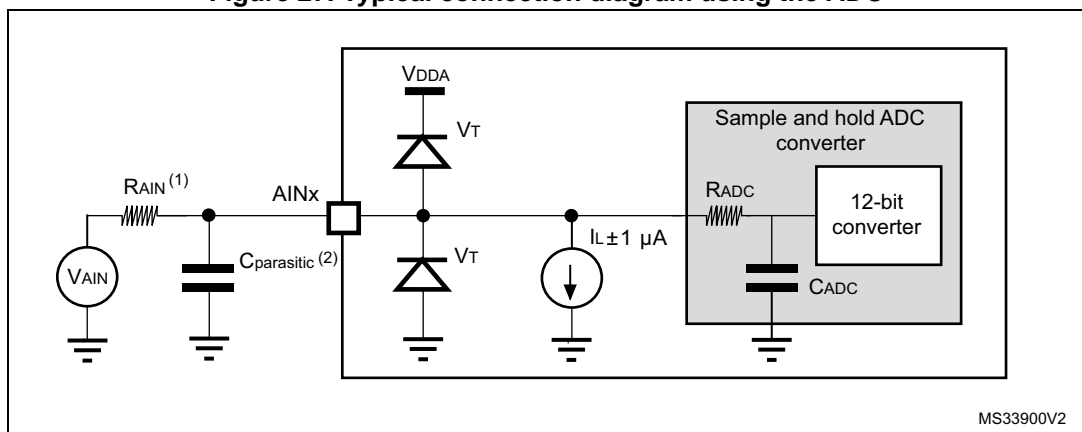


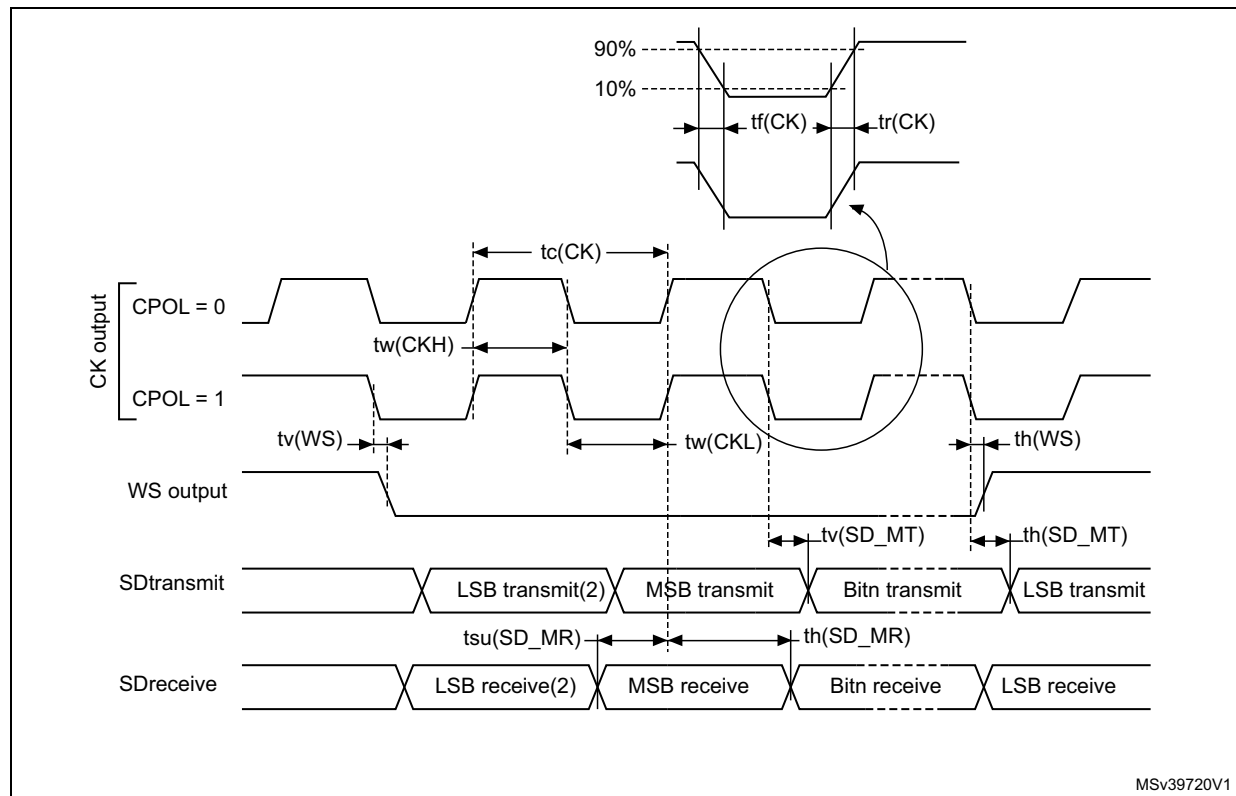
Figure 27. Typical connection diagram using the ADC



1. Refer to [Table 57: ADC characteristics](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 13: Power supply scheme](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Figure 34. I²S master timing diagram (Philips protocol)

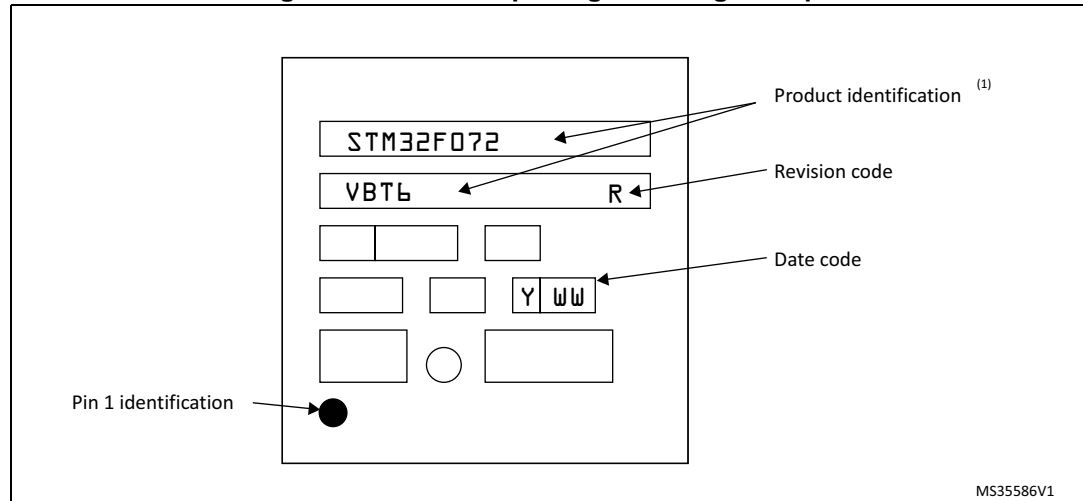
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 40. LQFP100 package marking example



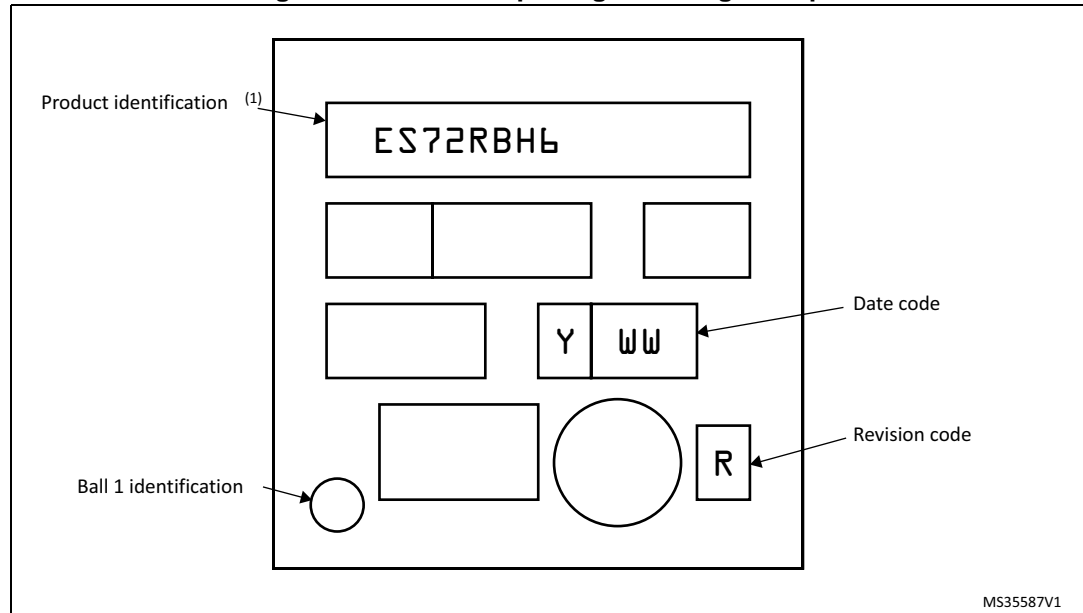
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 43. UFBGA64 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.8 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 24: General operating conditions](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and P_{IO} max ($P_D \text{ max} = P_{INT} \text{ max} + P_{IO} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

P_{IO} max represents the maximum power dissipation on output pins where:

$$P_{IO} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 80. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	49	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Ordering information](#).

Table 82. Document revision history (continued)

Date	Revision	Changes
18-Sep-2015	3 (continued)	<ul style="list-style-type: none"> – Table 42: HSI14 oscillator characteristics: changed the min value for ACC_{HSI14} – Table 46: Flash memory characteristics: removed V_{prog} – Table 49: EMI characteristics updated – Table 50: ESD absolute maximum ratings updated – Table 57: ADC characteristics - updated some parameter values, test conditions and added footnotes ⁽³⁾ and ⁽⁴⁾ – Table 60: DAC characteristics - I_{DDA} max value (DAC DC current consumption) updated – Table 61: Comparator characteristics: changed the description and values for t_{S_SC} parameter – Table 62: TS characteristics: changed the min value for t_{S_temp} – Table 63: VBAT monitoring characteristics: changed the typical value for R parameter – Table 69: I^2S characteristics: updated the min value for data input hold time (master and slave receiver) <p>Section 7: Package information:</p> <ul style="list-style-type: none"> – information generally updated, UFBGA64 added <p>Section 8: Part numbering: UFBGA64 added</p>
17-Dec-2015	4	<p>Section 2: Description:</p> <ul style="list-style-type: none"> – Figure 1: Block diagram updated <p>Section 3: Functional overview:</p> <ul style="list-style-type: none"> – Figure 2: Clock tree updated <p>Section 4: Pinouts and pin descriptions</p> <ul style="list-style-type: none"> – Package pinout figures updated (look and feel) – Figure 9: WLCSP49 package pinout - now presented in top view <p>Section 5: Memory mapping:</p> <ul style="list-style-type: none"> – added information on STM32F072x8 difference versus STM32F072xB map in Figure 10 – Table 28: Embedded internal reference voltage: removed -40°-to-85° condition for V_{REFINT} and associated note <p>Section 6: Electrical characteristics:</p> <ul style="list-style-type: none"> – Table 61: Comparator characteristics - min value for V_{DDA} replaced with V_{DD} – Figure 29: Maximum V_{REFINT} scaler startup time from power down added – Table 53: I/O static characteristics - note removed – Table 69: I^2S characteristics: table reorganized <p>Section 8: Ordering information:</p> <ul style="list-style-type: none"> – added tray packing to options

Table 82. Document revision history (continued)

Date	Revision	Changes
10-Jan-2017	5	<p>Section 6: Electrical characteristics:</p> <ul style="list-style-type: none"> – <i>Table 40: LSE oscillator characteristics ($f_{LSE} = 32.768\text{ kHz}$)</i> - information on configuring different drive capabilities removed. See the corresponding reference manual. – <i>Table 28: Embedded internal reference voltage</i> - V_{REFINT} values – <i>Table 60: DAC characteristics</i> - min. R_{LOAD} to V_{DDA} defined – <i>Figure 30: SPI timing diagram - slave mode and CPHA = 0</i> and <i>Figure 31: SPI timing diagram - slave mode and CPHA = 1</i> enhanced and corrected <p>Section 8: Ordering information:</p> <ul style="list-style-type: none"> – The name of the section changed from the previous “Part numbering”