**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

## Details

| | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072cbt7 |

# List of figures

**Table 6. Number of capacitive sensing channels available**
**on STM32F072x8/xB devices**

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
| | STM32F072Vx | STM32F072Rx | STM32F072Cx |
| G1 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 |
| G3 | 3 | 3 | 2 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 3 | 3 | 3 |
| G7 | 3 | 0 | 0 |
| G8 | 3 | 0 | 0 |
| Number of capacitive sensing channels | 24 | 18 | 17 |

## 3.14 Timers and watchdogs

The STM32F072x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 7 compares the features of the different timers.

**Table 7. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | 3 |
| General purpose | TIM2 | 32-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM3 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM14 | 16-bit | Up | integer from 1 to 65536 | No | 1 | - |
| | TIM15 | 16-bit | Up | integer from 1 to 65536 | Yes | 2 | 1 |
| | TIM16 TIM17 | 16-bit | Up | integer from 1 to 65536 | Yes | 1 | 1 |
| Basic | TIM6 TIM7 | 16-bit | Up | integer from 1 to 65536 | Yes | - | - |

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate withTIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

### 3.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

### 3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:
- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

## 3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on $V_{DD}$ supply when present or through the $V_{BAT}$ pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when $V_{DD}$ power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- Periodic wakeup unit with programmable resolution and period.
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

## 3.16 Inter-integrated circuit interface (I$^2$C)

Up to two I$^2$C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on most of the associated I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

### Table 8. Comparison of I$^2$C analog and digital filters

| Aspect | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2Cx peripheral clocks |
| Benefits | Available in Stop mode | –Extra filtering capability vs. standard requirements<br>–Stable length |
| Drawbacks | Variations depending on temperature, voltage, process | Wakeup from Stop on address match is not available when digital filter is enabled. |

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts

# 4        Pinouts and pin descriptions

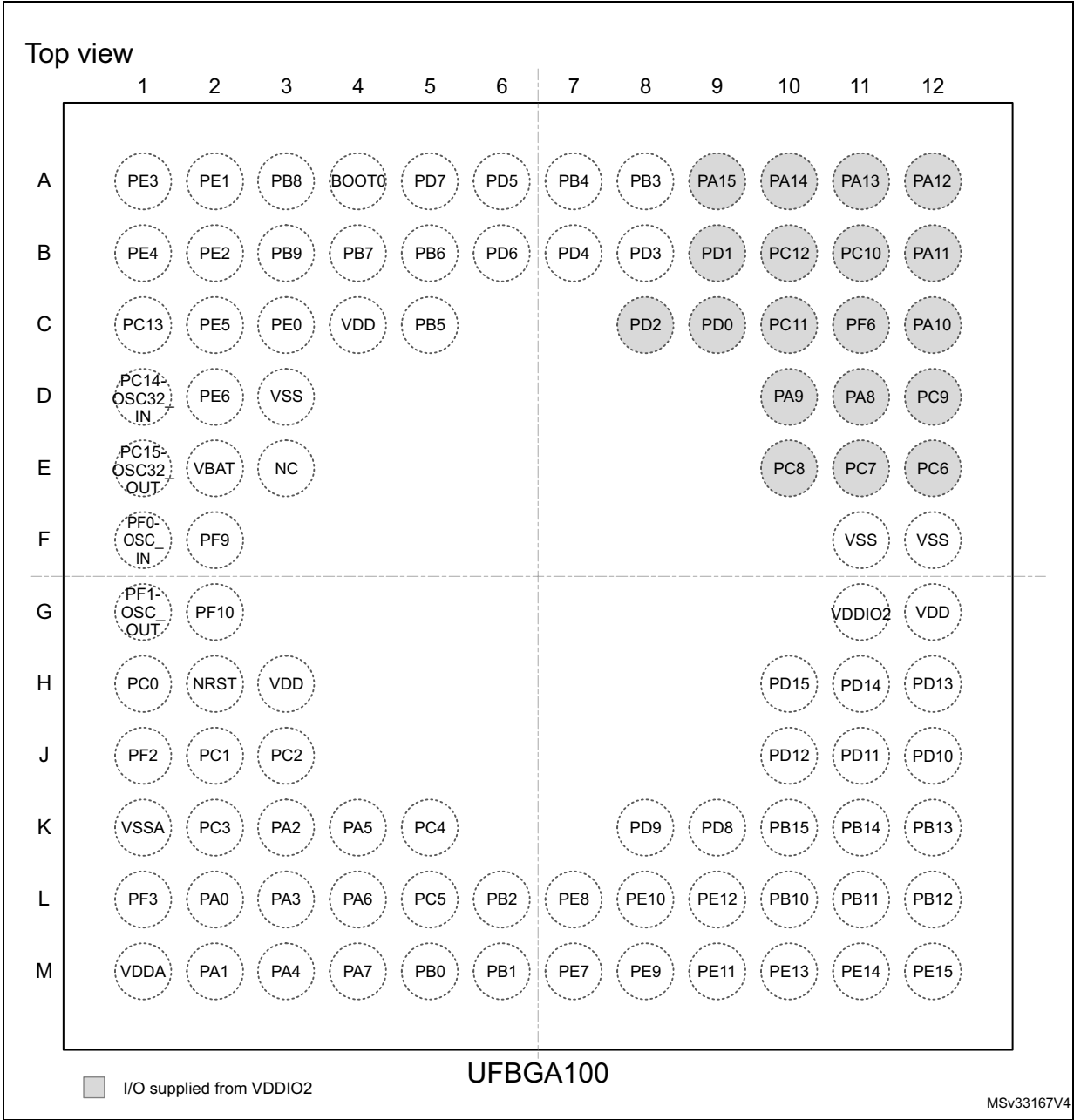**Figure 3. UFBGA100 package pinout**

**Table 12. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |
| Pin type | | S | Supply pin |
| | | I | Input-only pin |
| | | I/O | Input / output pin |
| I/O structure | | FT | 5 V-tolerant I/O |
| | | FTf | 5 V-tolerant I/O, FM+ capable |
| | | TTa | 3.3 V-tolerant I/O directly connected to ADC |
| | | TC | Standard 3.3 V I/O |
| | | B | Dedicated BOOT0 pin |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset. |
| Pin functions | Alternate functions | | Functions selected through GPIOx_AFR registers |
| | Additional functions | | Functions directly selected/enabled through peripheral registers |

**Table 13. STM32F072x8/xB pin definitions**

| Pin numbers | | | | | | | | | | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | LQFP48/UFQFPN48 | WLCSP49 | Pin name (function upon reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
| B2 | 1 | - | - | - | - | PE2 | I/O | FT | - | TSC_G7_IO1, TIM3_ETR | - |
| A1 | 2 | - | - | - | - | PE3 | I/O | FT | - | TSC_G7_IO2, TIM3_CH1 | - |
| B1 | 3 | - | - | - | - | PE4 | I/O | FT | - | TSC_G7_IO3, TIM3_CH2 | - |
| C2 | 4 | - | - | - | - | PE5 | I/O | FT | - | TSC_G7_IO4, TIM3_CH3 | - |
| D2 | 5 | - | - | - | - | PE6 | I/O | FT | - | TIM3_CH4 | WKUP3, RTC_TAMP3 |
| E2 | 6 | B2 | 1 | 1 | B7 | VBAT | S | - | - | Backup power supply | |

**Table 14. Alternate functions selected through GPIOA_AFR registers for port A**

| Pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|
| PA0 | - | USART2_CTS | TIM2_CH1_ETR | TSC_G1_IO1 | USART4_TX | - | - | COMP1_OUT |
| PA1 | EVENTOUT | USART2_RTS | TIM2_CH2 | TSC_G1_IO2 | USART4_RX | TIM15_CH1N | - | - |
| PA2 | TIM15_CH1 | USART2_TX | TIM2_CH3 | TSC_G1_IO3 | - | - | - | COMP2_OUT |
| PA3 | TIM15_CH2 | USART2_RX | TIM2_CH4 | TSC_G1_IO4 | - | - | - | - |
| PA4 | SPI1_NSS, I2S1_WS | USART2_CK | - | TSC_G2_IO1 | TIM14_CH1 | - | - | - |
| PA5 | SPI1_SCK, I2S1_CK | CEC | TIM2_CH1_ETR | TSC_G2_IO2 | - | - | - | - |
| PA6 | SPI1_MISO, I2S1_MCK | TIM3_CH1 | TIM1_BKIN | TSC_G2_IO3 | USART3_CTS | TIM16_CH1 | EVENTOUT | COMP1_OUT |
| PA7 | SPI1_MOSI, I2S1_SD | TIM3_CH2 | TIM1_CH1N | TSC_G2_IO4 | TIM14_CH1 | TIM17_CH1 | EVENTOUT | COMP2_OUT |
| PA8 | MCO | USART1_CK | TIM1_CH1 | EVENTOUT | CRS_SYNC | - | - | - |
| PA9 | TIM15_BKIN | USART1_TX | TIM1_CH2 | TSC_G4_IO1 | - | - | - | - |
| PA10 | TIM17_BKIN | USART1_RX | TIM1_CH3 | TSC_G4_IO2 | - | - | - | - |
| PA11 | EVENTOUT | USART1_CTS | TIM1_CH4 | TSC_G4_IO3 | CAN_RX | - | - | COMP1_OUT |
| PA12 | EVENTOUT | USART1_RTS | TIM1_ETR | TSC_G4_IO4 | CAN_TX | - | - | COMP2_OUT |
| PA13 | SWDIO | IR_OUT | USB_NOE | - | - | - | - | - |
| PA14 | SWCLK | USART2_TX | - | - | - | - | - | - |
| PA15 | SPI1_NSS, I2S1_WS | USART2_RX | TIM2_CH1_ETR | EVENTOUT | USART4_RTS | - | - | - |

# 5      Memory mapping

To the difference of STM32F072xB memory map in *Figure 10*, the two bottom code memory spaces of STM32F072x8 end at 0x0000 FFFF and 0x0800 FFFF, respectively.
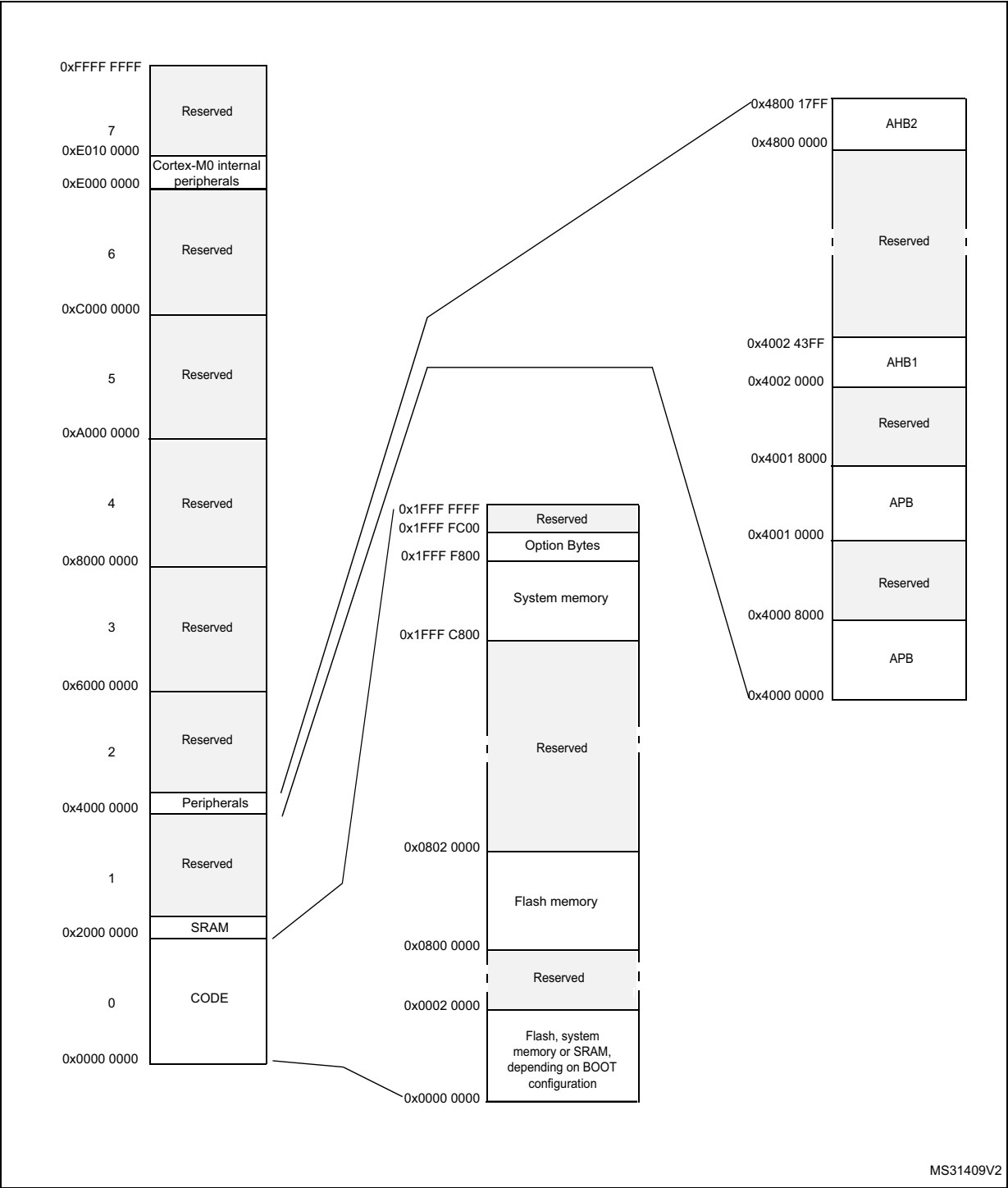
**Figure 10. STM32F072xB memory map**

**Table 35. Peripheral current consumption (continued)**

| | Peripheral | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| APB | APB-Bridge[2] | 2.8 | µA/MHz |
| | ADC[3] | 4.1 | |
| | CAN | 12.4 | |
| | CEC | 1.5 | |
| | CRS | 0.8 | |
| | DAC[3] | 4.7 | |
| | DEBUG (MCU debug feature) | 0.1 | |
| | I2C1 | 3.9 | |
| | I2C2 | 4.0 | |
| | PWR | 1.3 | |
| | SPI1 | 8.7 | |
| | SPI2 | 8.5 | |
| | SYSCFG & COMP | 1.7 | |
| | TIM1 | 14.9 | |
| | TIM2 | 15.5 | |
| | TIM3 | 11.4 | |
| | TIM6 | 2.5 | |
| | TIM7 | 2.3 | |
| | TIM14 | 5.3 | |
| | TIM15 | 9.1 | |
| | TIM16 | 6.6 | |
| | TIM17 | 6.8 | |
| | USART1 | 17.0 | |
| | USART2 | 16.7 | |
| | USART3 | 5.4 | |
| | USART4 | 5.4 | |
| | USB | 7.2 | |
| | WWDG | 1.4 | |
| | **All APB peripherals** | **182** | |

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).

2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.

3. The power consumption of the analog part ($I_{DDA}$) of peripherals such as ADC, DAC, Comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

**Table 57. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{TRIG}$[2] | External trigger frequency | $f_{ADC}$ = 14 MHz, 12-bit resolution | - | - | 823 | kHz |
| | | 12-bit resolution | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | - | 0 | - | $V_{DDA}$ | V |
| $R_{AIN}$[2] | External input impedance | See *Equation 1* and *Table 58* for details | - | - | 50 | kΩ |
| $R_{ADC}$[2] | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$[2] | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$[2][3] | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | - | 83 | | | $1/f_{ADC}$ |
| $W_{LATENCY}$[2][4] | ADC_DR register ready latency | ADC clock = HSI14 | 1.5 ADC cycles + 2 $f_{PCLK}$ cycles | - | 1.5 ADC cycles + 3 $f_{PCLK}$ cycles | - |
| | | ADC clock = PCLK/2 | - | 4.5 | - | $f_{PCLK}$ cycle |
| | | ADC clock = PCLK/4 | - | 8.5 | - | $f_{PCLK}$ cycle |
| $t_{latr}$[2] | Trigger conversion latency | $f_{ADC}$ = $f_{PCLK}$/2 = 14 MHz | 0.196 | | | µs |
| | | $f_{ADC}$ = $f_{PCLK}$/2 | 5.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC}$ = $f_{PCLK}$/4 = 12 MHz | 0.219 | | | µs |
| | | $f_{ADC}$ = $f_{PCLK}$/4 | 10.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC}$ = $f_{HSI14}$ = 14 MHz | 0.179 | - | 0.250 | µs |
| $Jitter_{ADC}$ | ADC jitter on trigger conversion | $f_{ADC}$ = $f_{HSI14}$ | - | 1 | - | $1/f_{HSI14}$ |
| $t_S$[2] | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | - | 17.1 | µs |
| | | - | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$[2] | Stabilization time | - | 14 | | | $1/f_{ADC}$ |
| $t_{CONV}$[2] | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz, 12-bit resolution | 1 | - | 18 | µs |
| | | 12-bit resolution | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on $I_{DDA}$ and 60 µA on $I_{DD}$ should be taken into account.

2. Guaranteed by design, not tested in production.

3. Specified value includes only ADC timing. It does not include the latency of the register access.

4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Table 60. DAC characteristics (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Gain error[3] | Gain error | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| $t_{SETTLING}$[3] | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | - | 3 | 4 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| Update rate[3] | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| $t_{WAKEUP}$[3] | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR+ [1] | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD} = 50$ pF |

1. Guaranteed by design, not tested in production.

2. The DAC is in "quiescent mode" when it keeps the value steady on the output so no dynamic consumption is involved.

3. Data based on characterization results, not tested in production.

Figure 28. 12-bit buffered / non-buffered DAC
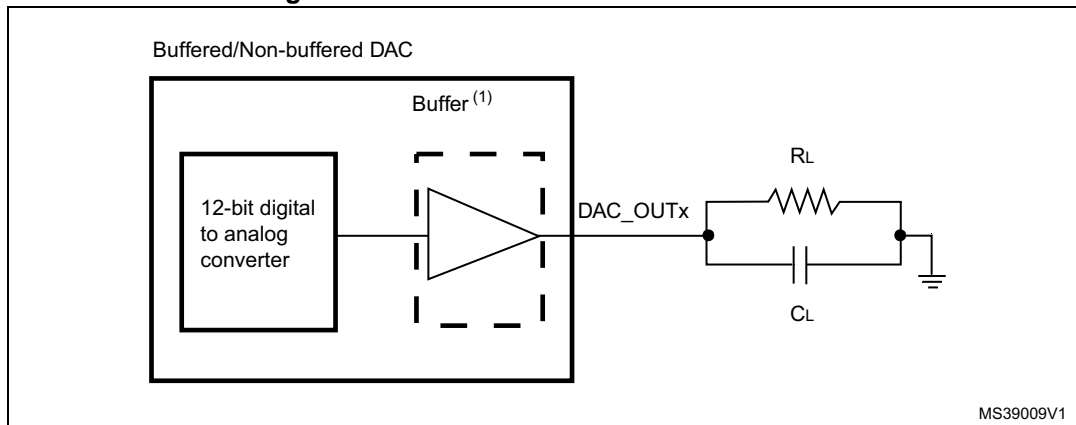


1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

**Figure 32. SPI timing diagram - master mode**
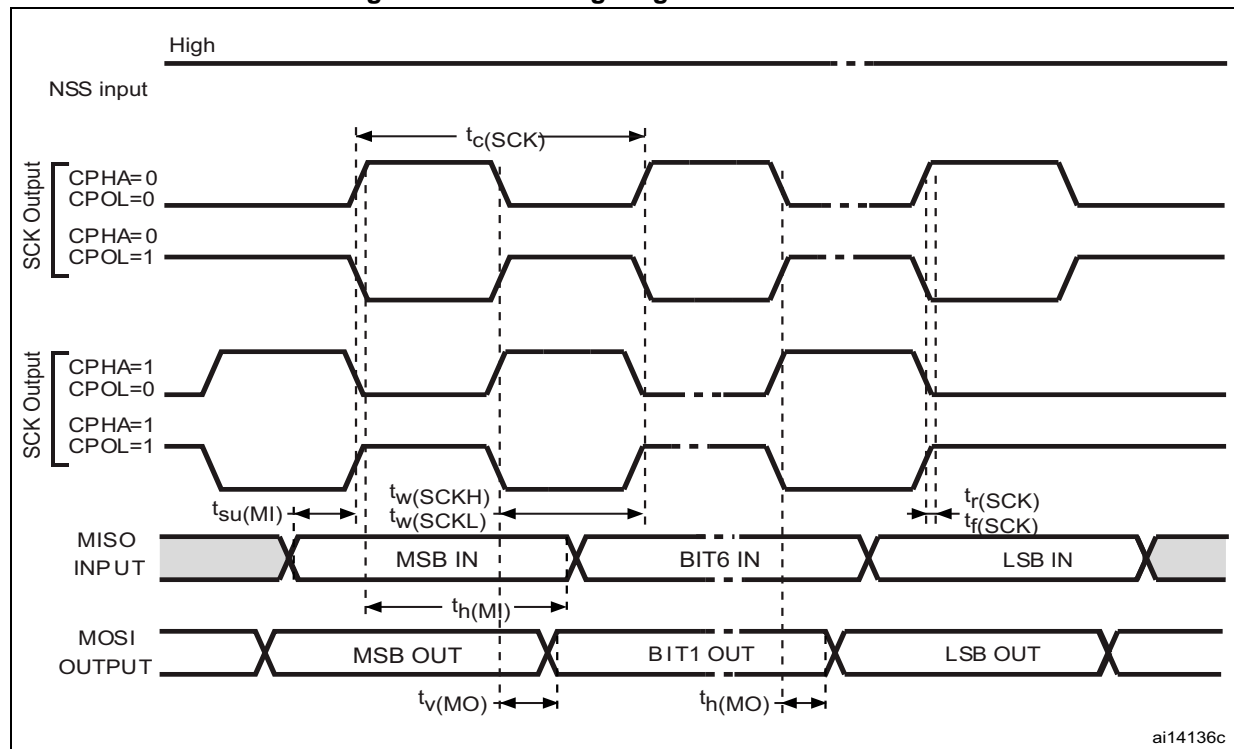


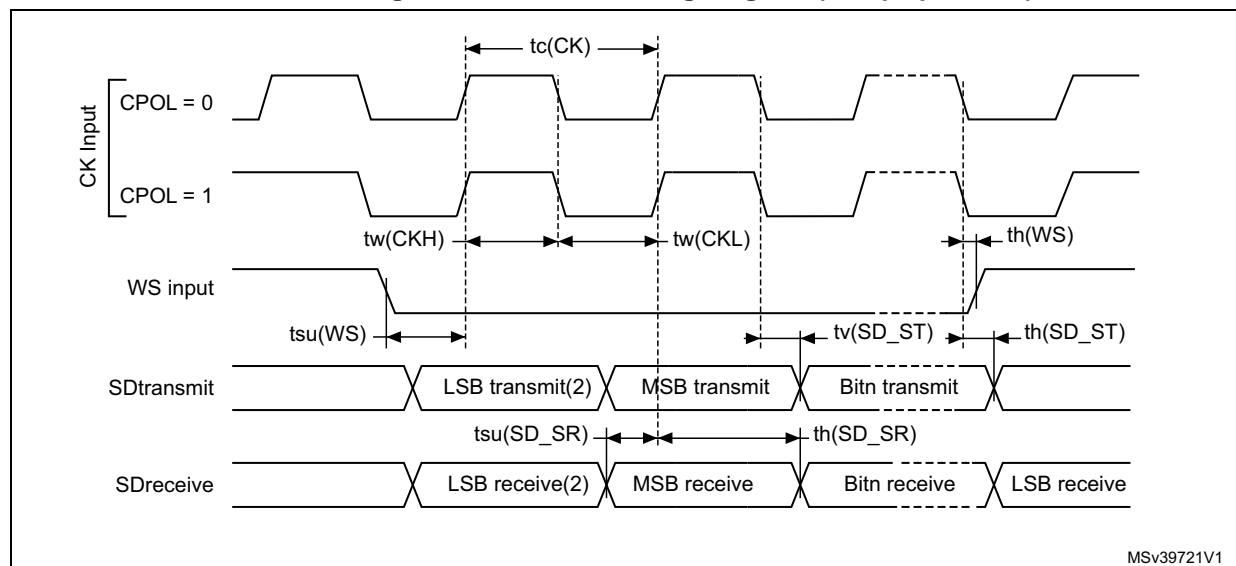1. Measurement points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**Table 69. I²S characteristics[1]**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CK}$ $1/t_{c(CK)}$ | I²S clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | 1.597 | 1.601 | MHz |
| | | Slave mode | 0 | 6.5 | |
| $t_{r(CK)}$ | I²S clock rise time | Capacitive load $C_L$ = 15 pF | - | 10 | ns |
| $t_{f(CK)}$ | I²S clock fall time | | - | 12 | |
| $t_{w(CKH)}$ | I²S clock high time | Master $f_{PCLK}$= 16 MHz, audio frequency = 48 kHz | 306 | - | |
| $t_{w(CKL)}$ | I²S clock low time | | 312 | - | |
| $t_{v(WS)}$ | WS valid time | Master mode | 2 | - | |
| $t_{h(WS)}$ | WS hold time | Master mode | 2 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 7 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 0 | - | |
| DuCy(SCK) | I²S slave input clock duty cycle | Slave mode | 25 | 75 | % |

**Table 69. I²S characteristics[1] (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|-----------|-----|-----|------|
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 6 | - | ns |
| $t_{su(SD\_SR)}$ |  | Slave receiver | 2 | - |  |
| $t_{h(SD\_MR)}$[2] | Data input hold time | Master receiver | 4 | - |  |
| $t_{h(SD\_SR)}$[2] |  | Slave receiver | 0.5 | - |  |
| $t_{v(SD\_MT)}$[2] | Data output valid time | Master transmitter | - | 4 |  |
| $t_{v(SD\_ST)}$[2] |  | Slave transmitter | - | 20 |  |
| $t_{h(SD\_MT)}$ | Data output hold time | Master transmitter | 0 | - |  |
| $t_{h(SD\_ST)}$ |  | Slave transmitter | 13 | - |  |

1. Data based on design simulation and/or characterization results, not tested in production.

2. Depends on $f_{PCLK}$. For example, if $f_{PCLK}$ = 8 MHz, then $T_{PCLK}$ = $1/f_{PLCLK}$ = 125 ns.

**Figure 33. I²S slave timing diagram (Philips protocol)**



1. Measurement points are done at CMOS levels: 0.3 × $V_{DDIOx}$ and 0.7 × $V_{DDIOx}$.

2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Table 74. UFBGA64 package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|--------|-----|-----|-----|-----|-----|-----|
| | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 42. Recommended footprint for UFBGA64 package**



A019_FP_V2
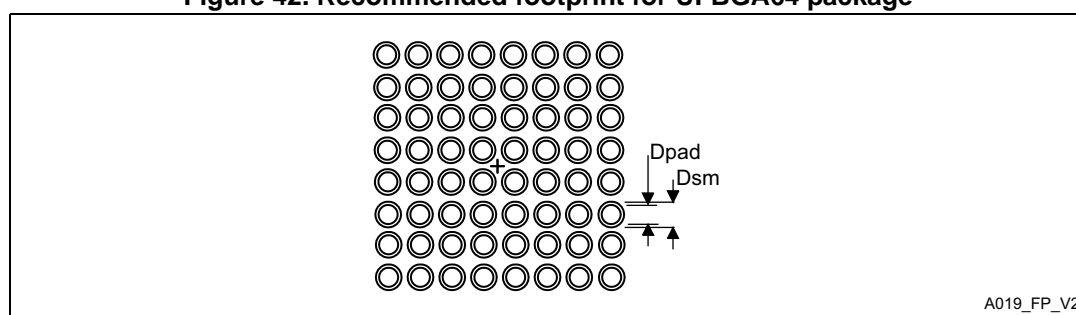
**Table 75. UFBGA64 recommended PCB design rules**

| Dimension | Recommended values |
|-----------|-------------------|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.100 mm |

## Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 43. UFBGA64 package marking example**
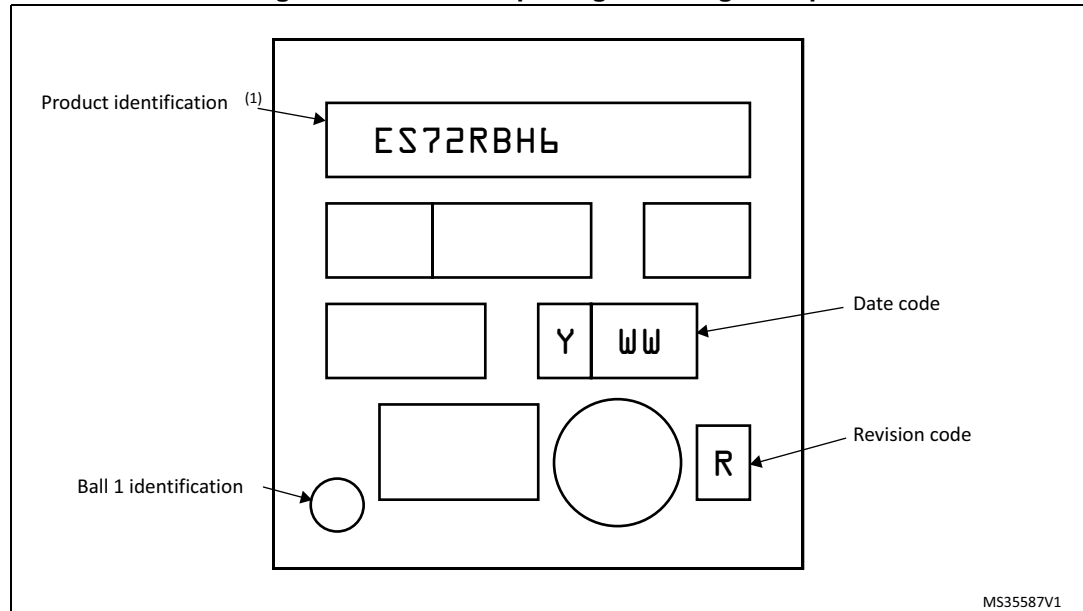


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.4 LQFP64 package information

**LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.**

**Figure 44. LQFP64 package outline**
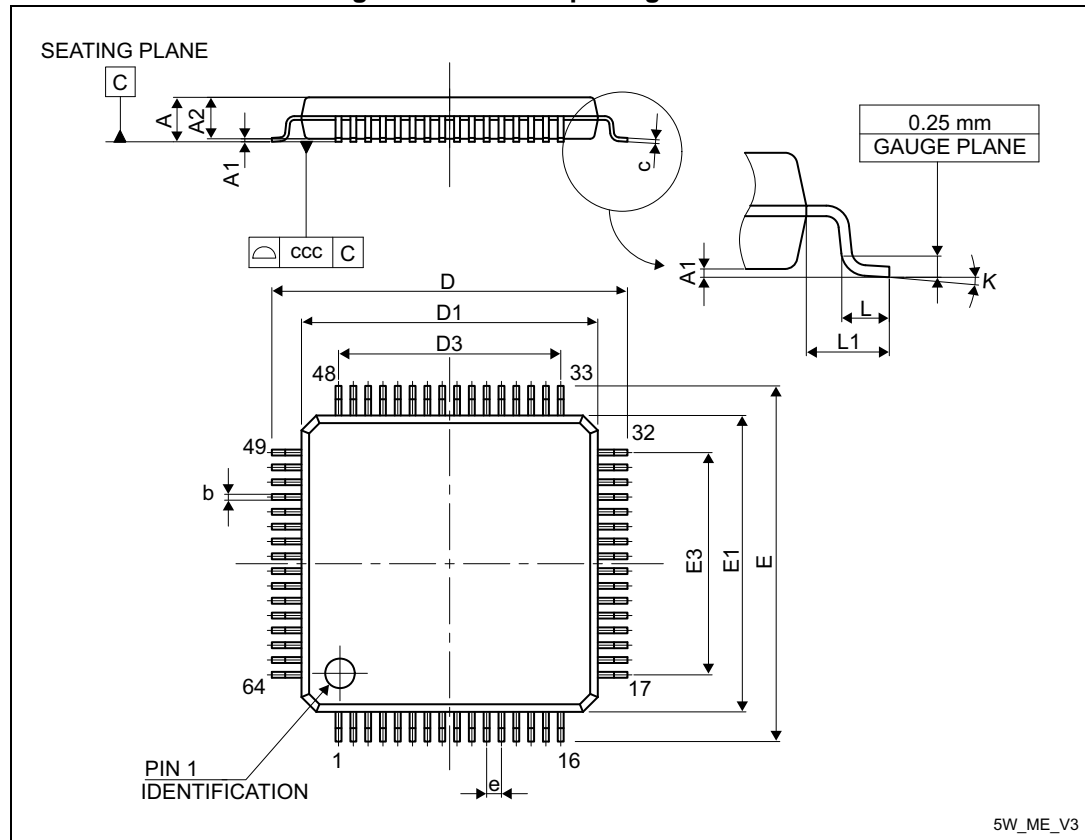


1. Drawing is not to scale.
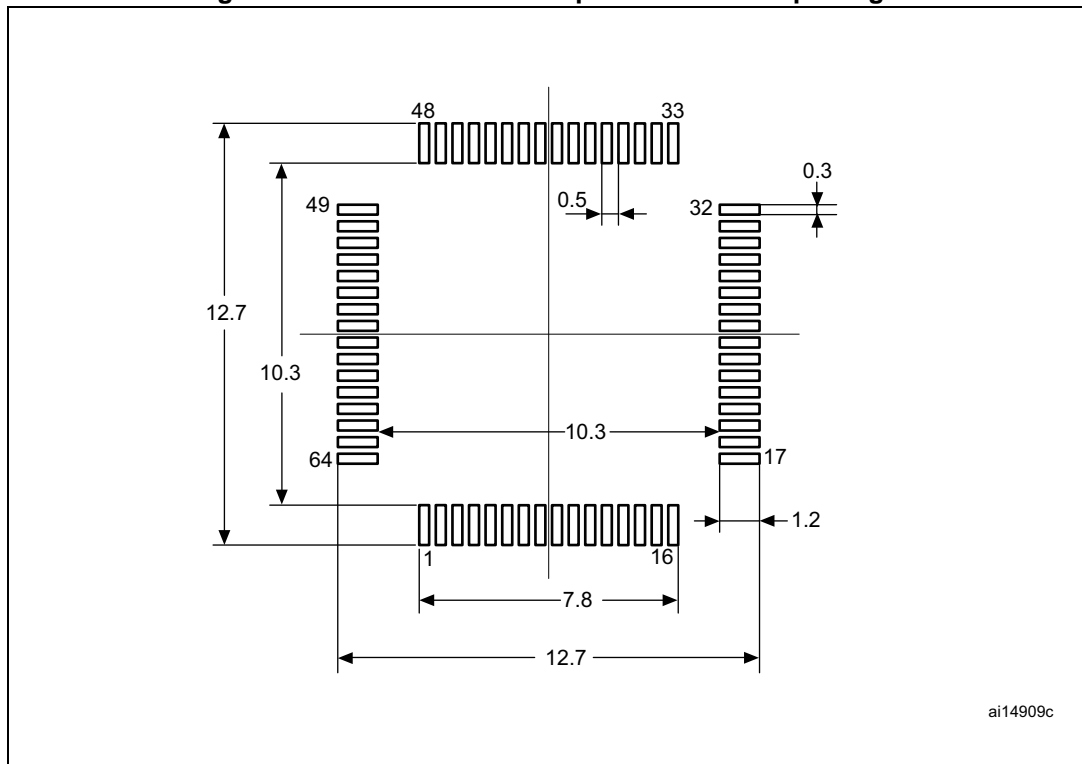
**Table 76. LQFP64 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

**Table 76. LQFP64 package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 45. Recommended footprint for LQFP64 package**



1. Dimensions are expressed in millimeters.

## 7.6 LQFP48 package information

**LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.**

**Figure 49. LQFP48 package outline**
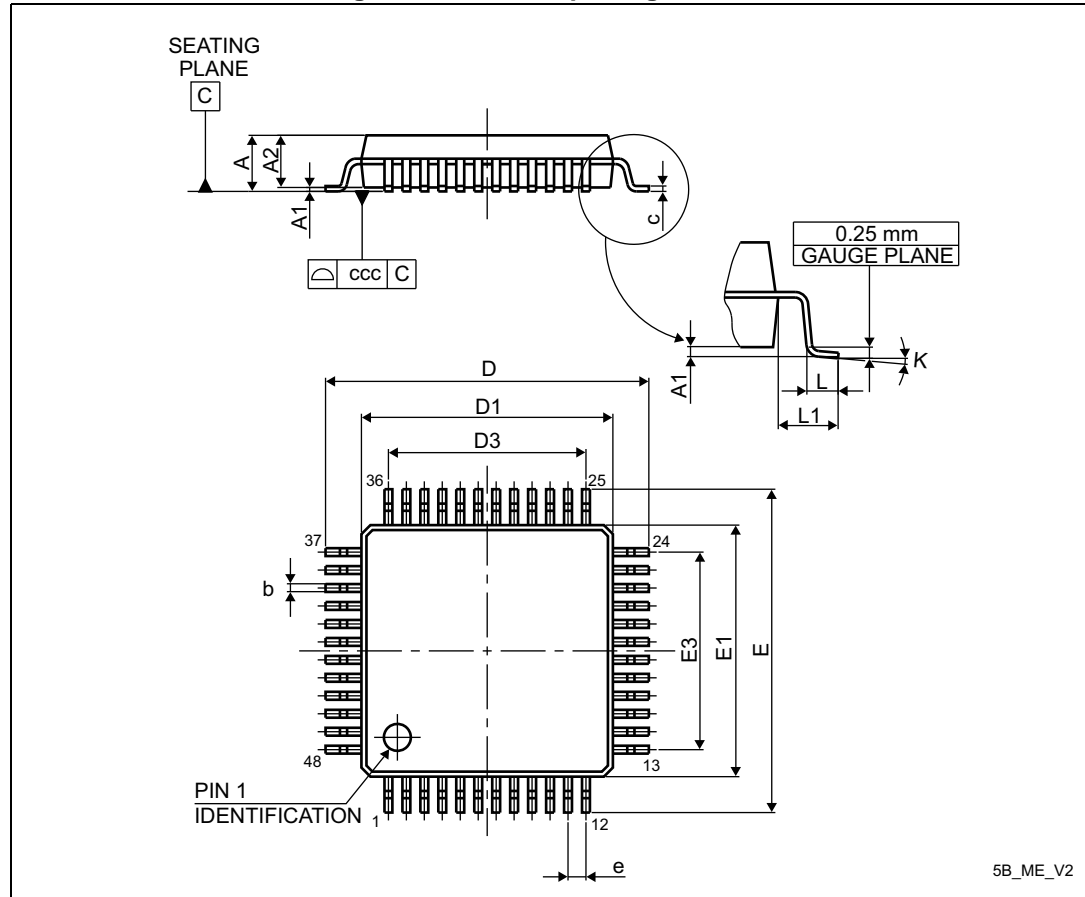


1. Drawing is not to scale.

#### Table 78. LQFP48 package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

#### Figure 50. Recommended footprint for LQFP48 package
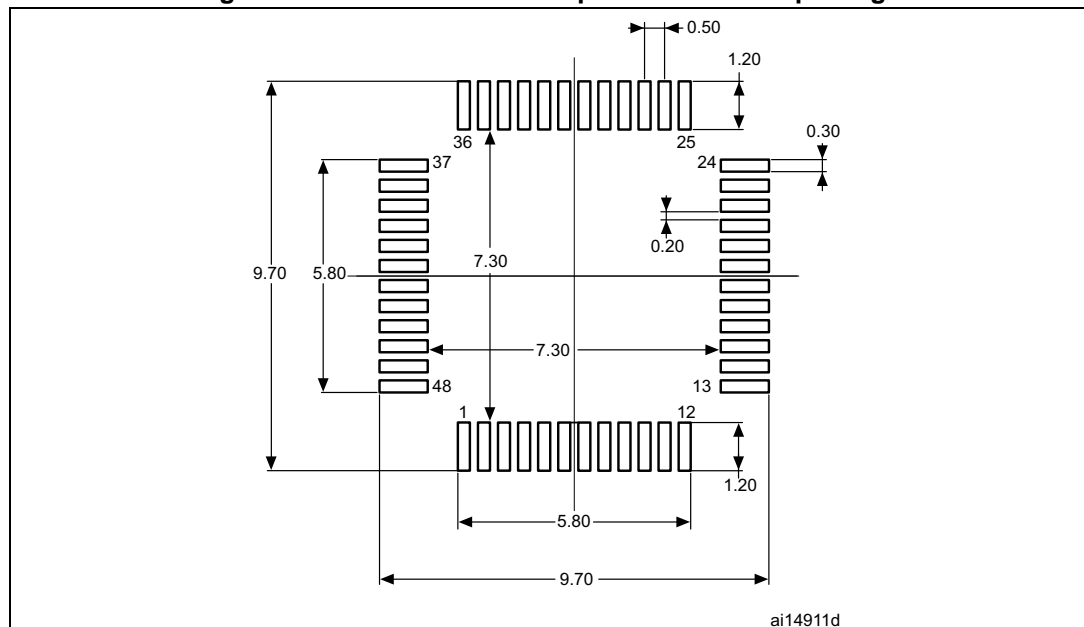


1. Dimensions are expressed in millimeters.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**