**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-UFQFN Exposed Pad |
| Supplier Device Package | 48-UFQFPN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072cbu7 |

# Contents

**Table 2. STM32F072x8/xB family device features and peripheral counts**

| Peripheral | | STM32F072Cx | | STM32F072Rx | | STM32F072Vx | |
|---|---|---|---|---|---|---|---|
| Flash memory (Kbyte) | | 64 | 128 | 64 | 128 | 64 | 128 |
| SRAM (Kbyte) | | 16 | | | | | |
| Timers | Advanced control | 1 (16-bit) | | | | | |
| | General purpose | 5 (16-bit)<br>1 (32-bit) | | | | | |
| | Basic | 2 (16-bit) | | | | | |
| Comm. interfaces | SPI [$I^2S$](1) | 2 [2] | | | | | |
| | $I^2C$ | 2 | | | | | |
| | USART | 4 | | | | | |
| | CAN | 1 | | | | | |
| | USB | 1 | | | | | |
| | CEC | 1 | | | | | |
| 12-bit ADC (number of channels) | | 1<br>(10 ext. + 3 int.) | | 1<br>(16 ext. + 3 int.) | | | |
| 12-bit DAC (number of channels) | | 1<br>(2) | | | | | |
| Analog comparator | | 2 | | | | | |
| GPIOs | | 37 | | 51 | | 87 | |
| Capacitive sensing channels | | 17 | | 18 | | 24 | |
| Max. CPU frequency | | 48 MHz | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | |
| Operating temperature | | Ambient operating temperature: -40°C to 85°C / -40°C to 105°C<br>Junction temperature: -40°C to 105°C / -40°C to 125°C | | | | | |
| Packages | | LQFP48<br>UFQFPN48<br>WLCSP49 | | LQFP64<br>UFBGA64 | | LQFP100<br>UFBGA100 | |

1. The SPI interface can be used either in SPI mode or in $I^2S$ audio mode.

**Table 6. Number of capacitive sensing channels available on STM32F072x8/xB devices**

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
| | STM32F072Vx | STM32F072Rx | STM32F072Cx |
| G1 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 |
| G3 | 3 | 3 | 2 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 3 | 3 | 3 |
| G7 | 3 | 0 | 0 |
| G8 | 3 | 0 | 0 |
| Number of capacitive sensing channels | 24 | 18 | 17 |

## 3.14 Timers and watchdogs

The STM32F072x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

*Table 7* compares the features of the different timers.

**Table 7. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | 3 |
| General purpose | TIM2 | 32-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM3 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM14 | 16-bit | Up | integer from 1 to 65536 | No | 1 | - |
| | TIM15 | 16-bit | Up | integer from 1 to 65536 | Yes | 2 | 1 |
| | TIM16 TIM17 | 16-bit | Up | integer from 1 to 65536 | Yes | 1 | 1 |
| Basic | TIM6 TIM7 | 16-bit | Up | integer from 1 to 65536 | Yes | - | - |

Table 13. STM32F072x8/xB pin definitions (continued)

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | LQFP48/UFQFPN48 | WLCSP49 | | | | | Alternate functions | Additional functions |
| C10 | 79 | B6 | 52 | - | - | PC11 | I/O | FT | (3) | USART3_RX, USART4_RX | - |
| B10 | 80 | C5 | 53 | - | - | PC12 | I/O | FT | (3) | USART3_CK, USART4_CK | - |
| C9 | 81 | - | - | - | - | PD0 | I/O | FT | (3) | SPI2_NSS, I2S2_WS, CAN_RX | - |
| B9 | 82 | - | - | - | - | PD1 | I/O | FT | (3) | SPI2_SCK, I2S2_CK, CAN_TX | - |
| C8 | 83 | B5 | 54 | - | - | PD2 | I/O | FT | (3) | USART3_RTS, TIM3_ETR | - |
| B8 | 84 | - | - | - | - | PD3 | I/O | FT | - | SPI2_MISO, I2S2_MCK, USART2_CTS | - |
| B7 | 85 | - | - | - | - | PD4 | I/O | FT | - | SPI2_MOSI, I2S2_SD, USART2_RTS | - |
| A6 | 86 | - | - | - | - | PD5 | I/O | FT | - | USART2_TX | - |
| B6 | 87 | - | - | - | - | PD6 | I/O | FT | - | USART2_RX | - |
| A5 | 88 | - | - | - | - | PD7 | I/O | FT | - | USART2_CK | - |
| A8 | 89 | A5 | 55 | 39 | A3 | PB3 | I/O | FT | - | SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT | - |
| A7 | 90 | A4 | 56 | 40 | A4 | PB4 | I/O | FT | - | SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT | - |
| C5 | 91 | C4 | 57 | 41 | B4 | PB5 | I/O | FT | - | SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2 | WKUP6 |
| B5 | 92 | D3 | 58 | 42 | C4 | PB6 | I/O | FTf | - | I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03 | - |

**Table 14. Alternate functions selected through GPIOA_AFR registers for port A**

| Pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|
| PA0 | - | USART2_CTS | TIM2_CH1_ETR | TSC_G1_IO1 | USART4_TX | - | - | COMP1_OUT |
| PA1 | EVENTOUT | USART2_RTS | TIM2_CH2 | TSC_G1_IO2 | USART4_RX | TIM15_CH1N | - | - |
| PA2 | TIM15_CH1 | USART2_TX | TIM2_CH3 | TSC_G1_IO3 | - | - | - | COMP2_OUT |
| PA3 | TIM15_CH2 | USART2_RX | TIM2_CH4 | TSC_G1_IO4 | - | - | - | - |
| PA4 | SPI1_NSS, I2S1_WS | USART2_CK | - | TSC_G2_IO1 | TIM14_CH1 | - | - | - |
| PA5 | SPI1_SCK, I2S1_CK | CEC | TIM2_CH1_ETR | TSC_G2_IO2 | - | - | - | - |
| PA6 | SPI1_MISO, I2S1_MCK | TIM3_CH1 | TIM1_BKIN | TSC_G2_IO3 | USART3_CTS | TIM16_CH1 | EVENTOUT | COMP1_OUT |
| PA7 | SPI1_MOSI, I2S1_SD | TIM3_CH2 | TIM1_CH1N | TSC_G2_IO4 | TIM14_CH1 | TIM17_CH1 | EVENTOUT | COMP2_OUT |
| PA8 | MCO | USART1_CK | TIM1_CH1 | EVENTOUT | CRS_SYNC | - | - | - |
| PA9 | TIM15_BKIN | USART1_TX | TIM1_CH2 | TSC_G4_IO1 | - | - | - | - |
| PA10 | TIM17_BKIN | USART1_RX | TIM1_CH3 | TSC_G4_IO2 | - | - | - | - |
| PA11 | EVENTOUT | USART1_CTS | TIM1_CH4 | TSC_G4_IO3 | CAN_RX | - | - | COMP1_OUT |
| PA12 | EVENTOUT | USART1_RTS | TIM1_ETR | TSC_G4_IO4 | CAN_TX | - | - | COMP2_OUT |
| PA13 | SWDIO | IR_OUT | USB_NOE | - | - | - | - | - |
| PA14 | SWCLK | USART2_TX | - | - | - | - | - | - |
| PA15 | SPI1_NSS, I2S1_WS | USART2_RX | TIM2_CH1_ETR | EVENTOUT | USART4_RTS | - | - | - |

**Table 29. Typical and maximum current consumption from $V_{DD}$ supply at $V_{DD}$ = 3.6 V (continued)**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | All peripherals enabled(1) | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$(2) | | | Typ | Max @ $T_A$(2) | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DD}$ | Supply current in Run mode, code executing from RAM | HSI48 | 48 MHz | 23.1 | 25.4 | 25.8 | 26.6 | 12.8 | 13.5 | 13.7 | 13.9 | mA |
| | | HSE bypass, PLL on | 48 MHz | 23.0 | 25.3(3) | 25.7 | 26.5(3) | 12.6 | 13.3(3) | 13.5 | 13.8(3) | |
| | | | 32 MHz | 15.4 | 17.3 | 17.8 | 18.3 | 7.96 | 8.92 | 9.17 | 9.73 | |
| | | | 24 MHz | 11.4 | 12.9 | 13.5 | 13.7 | 6.48 | 8.04 | 8.23 | 8.41 | |
| | | HSE bypass, PLL off | 8 MHz | 4.21 | 4.6 | 4.89 | 5.25 | 2.07 | 2.3 | 2.35 | 2.94 | |
| | | | 1 MHz | 0.78 | 0.9 | 0.92 | 1.15 | 0.36 | 0.48 | 0.59 | 0.82 | |
| | | HSI clock, PLL on | 48 MHz | 23.1 | 24.5 | 25.0 | 25.2 | 12.6 | 13.7 | 13.9 | 14.0 | |
| | | | 32 MHz | 15.4 | 17.4 | 17.7 | 18.2 | 8.05 | 8.85 | 9.16 | 9.94 | |
| | | | 24 MHz | 11.5 | 13.0 | 13.6 | 13.9 | 6.49 | 8.06 | 8.21 | 8.47 | |
| | | HSI clock, PLL off | 8 MHz | 4.34 | 4.75 | 5.03 | 5.41 | 2.11 | 2.36 | 2.38 | 2.98 | |
| | Supply current in Sleep mode | HSI48 | 48 MHz | 15.1 | 16.6 | 16.8 | 17.5 | 3.08 | 3.43 | 3.56 | 3.61 | |
| | | HSE bypass, PLL on | 48 MHz | 15.0 | 16.5(3) | 16.7 | 17.3(3) | 2.93 | 3.28(3) | 3.41 | 3.46(3) | |
| | | | 32 MHz | 9.9 | 11.4 | 11.6 | 11.9 | 2.0 | 2.24 | 2.32 | 2.49 | |
| | | | 24 MHz | 7.43 | 8.17 | 8.71 | 8.82 | 1.63 | 1.82 | 1.88 | 1.9 | |
| | | HSE bypass, PLL off | 8 MHz | 2.83 | 3.09 | 3.26 | 3.66 | 0.76 | 0.88 | 0.91 | 0.93 | |
| | | | 1 MHz | 0.42 | 0.54 | 0.55 | 0.67 | 0.28 | 0.39 | 0.41 | 0.43 | |
| | | HSI clock, PLL on | 48 MHz | 15.0 | 17.2 | 17.3 | 17.9 | 3.04 | 3.37 | 3.41 | 3.46 | |
| | | | 32 MHz | 9.93 | 11.3 | 11.6 | 11.7 | 2.11 | 2.35 | 2.44 | 2.65 | |
| | | | 24 MHz | 7.53 | 8.45 | 8.87 | 8.95 | 1.64 | 1.83 | 1.9 | 1.93 | |
| | | HSI clock, PLL off | 8 MHz | 2.95 | 3.24 | 3.41 | 3.8 | 0.8 | 0.92 | 0.94 | 0.97 | |

1. USB is kept disabled as this IP functions only with a 48 MHz clock.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of $I_{DD}$ and $I_{DDA}$).

**Table 32. Typical and maximum current consumption from the $V_{BAT}$ supply**

| Symbol | Parameter | Conditions | Typ @ $V_{BAT}$ | | | | | | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.65 V | 1.8 V | 2.4 V | 2.7 V | 3.3 V | 3.6 V | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD\_VBAT}$ | RTC domain supply current | LSE & RTC ON; “Xtal mode”: lower driving capability; LSEDRV[1:0] = '00' | 0.5 | 0.6 | 0.7 | 0.8 | 1.1 | 1.2 | 1.3 | 1.7 | 2.3 | µA |
| | | LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11' | 0.8 | 0.9 | 1.1 | 1.2 | 1.4 | 1.6 | 1.7 | 2.1 | 2.8 | |

1. Data based on characterization results, not tested in production.

### Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to $f_{HCLK}$ frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

**I/O dynamic current consumption**

In addition to the internal peripheral current consumption measured previously (see *Table 35: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DDIOx}$ is the I/O supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

$C_S$ is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 34. Switching output I/O current consumption**

| Symbol | Parameter | Conditions[1] | I/O toggling frequency ($f_{SW}$) | Typ | Unit |
|---|---|---|---|---|---|
| $I_{SW}$ | I/O current consumption | $V_{DDIOx}$ = 3.3 V<br>C =$C_{INT}$ | 4 MHz | 0.07 | mA |
| | | | 8 MHz | 0.15 | |
| | | | 16 MHz | 0.31 | |
| | | | 24 MHz | 0.53 | |
| | | | 48 MHz | 0.92 | |
| | | $V_{DDIOx}$ = 3.3 V<br>$C_{EXT}$ = 0 pF<br>C = $C_{INT}$ + $C_{EXT}$+ $C_S$ | 4 MHz | 0.18 | |
| | | | 8 MHz | 0.37 | |
| | | | 16 MHz | 0.76 | |
| | | | 24 MHz | 1.39 | |
| | | | 48 MHz | 2.188 | |
| | | $V_{DDIOx}$ = 3.3 V<br>$C_{EXT}$ = 10 pF<br>C = $C_{INT}$ + $C_{EXT}$+ $C_S$ | 4 MHz | 0.32 | |
| | | | 8 MHz | 0.64 | |
| | | | 16 MHz | 1.25 | |
| | | | 24 MHz | 2.23 | |
| | | | 48 MHz | 4.442 | |
| | | $V_{DDIOx}$ = 3.3 V<br>$C_{EXT}$ = 22 pF<br>C = $C_{INT}$ + $C_{EXT}$+ $C_S$ | 4 MHz | 0.49 | |
| | | | 8 MHz | 0.94 | |
| | | | 16 MHz | 2.38 | |
| | | | 24 MHz | 3.99 | |
| | | $V_{DDIOx}$ = 3.3 V<br>$C_{EXT}$ = 33 pF<br>C = $C_{INT}$ + $C_{EXT}$+ $C_S$ | 4 MHz | 0.64 | |
| | | | 8 MHz | 1.25 | |
| | | | 16 MHz | 3.24 | |
| | | | 24 MHz | 5.02 | |
| | | $V_{DDIOx}$ = 3.3 V<br>$C_{EXT}$ = 47 pF<br>C = $C_{INT}$ + $C_{EXT}$+ $C_S$<br>C = $C_{int}$ | 4 MHz | 0.81 | |
| | | | 8 MHz | 1.7 | |
| | | | 16 MHz | 3.67 | |
| | | $V_{DDIOx}$ = 2.4 V<br>$C_{EXT}$ = 47 pF<br>C = $C_{INT}$ + $C_{EXT}$+ $C_S$<br>C = $C_{int}$ | 4 MHz | 0.66 | |
| | | | 8 MHz | 1.43 | |
| | | | 16 MHz | 2.45 | |
| | | | 24 MHz | 4.97 | |

1. $C_S$ = 7 pF (estimated value).

**Table 35. Peripheral current consumption (continued)**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| APB | APB-Bridge(2) | 2.8 | µA/MHz |
| | ADC(3) | 4.1 | |
| | CAN | 12.4 | |
| | CEC | 1.5 | |
| | CRS | 0.8 | |
| | DAC(3) | 4.7 | |
| | DEBUG (MCU debug feature) | 0.1 | |
| | I2C1 | 3.9 | |
| | I2C2 | 4.0 | |
| | PWR | 1.3 | |
| | SPI1 | 8.7 | |
| | SPI2 | 8.5 | |
| | SYSCFG & COMP | 1.7 | |
| | TIM1 | 14.9 | |
| | TIM2 | 15.5 | |
| | TIM3 | 11.4 | |
| | TIM6 | 2.5 | |
| | TIM7 | 2.3 | |
| | TIM14 | 5.3 | |
| | TIM15 | 9.1 | |
| | TIM16 | 6.6 | |
| | TIM17 | 6.8 | |
| | USART1 | 17.0 | |
| | USART2 | 16.7 | |
| | USART3 | 5.4 | |
| | USART4 | 5.4 | |
| | USB | 7.2 | |
| | WWDG | 1.4 | |
| | **All APB peripherals** | **182** | |

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part ($I_{DDA}$) of peripherals such as ADC, DAC, Comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

**Software recommendations**

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 49. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/48 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | -2 | dBµV |
| | | | 30 to 130 MHz | 27 | |
| | | | 130 MHz to 1 GHz | 17 | |
| | | | EMI Level | 4 | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 53. I/O static characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{lkg}$ | Input leakage current(2) | TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$ | - | - | ± 0.1 | µA |
| | | TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$ | - | - | 1 | |
| | | TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$ | - | - | ± 0.2 | |
| | | FT and FTf I/O $V_{DDIOx} \le V_{IN} \le 5$ V | - | - | 10 | |
| $R_{PU}$ | Weak pull-up equivalent resistor (3) | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(3) | $V_{IN} = - V_{DDIOx}$ | 25 | 40 | 55 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 52: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx}$, plus the maximum consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 21: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$, plus the maximum consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 21: Voltage characteristics*).

### Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

**Table 54. Output voltage characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage for an I/O pin | CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | |
| $V_{OL}$ | Output low level voltage for an I/O pin | TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 1.3 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$–1.3 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 6 mA $V_{DDIOx} \geq 2$ V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | |
| $V_{OL}$(4) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 4 mA | - | 0.4 | V |
| $V_{OH}$(4) | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | V |
| $V_{OLFm+}$(3) | Output low level voltage for an FTf I/O pin in Fm+ mode | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| | | $\|I_{IO}\|$ = 10 mA | - | 0.4 | V |

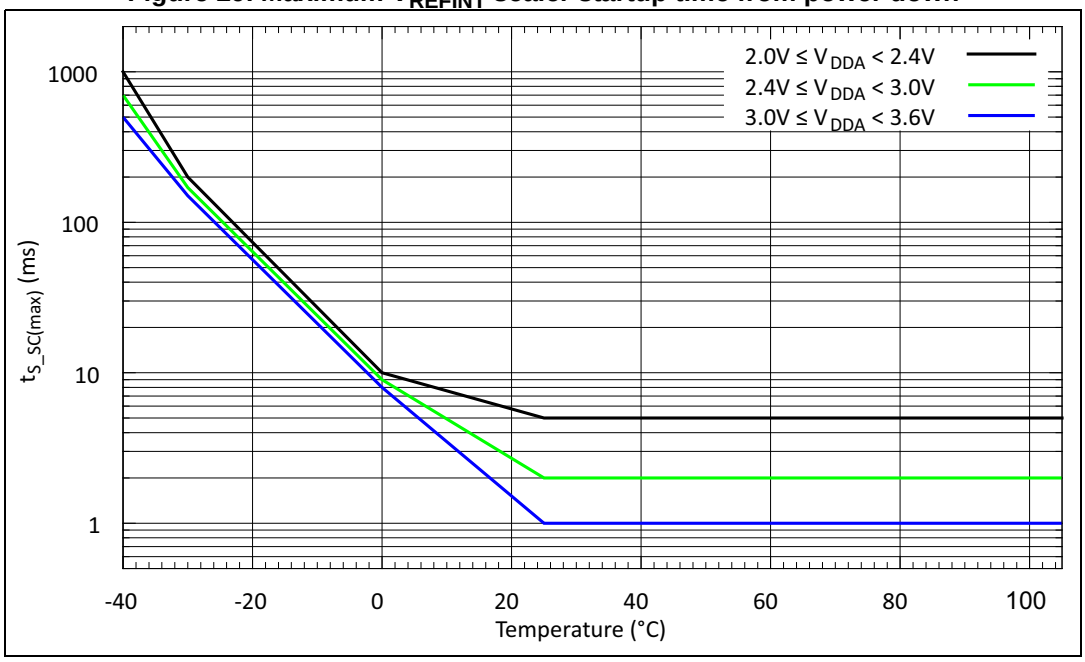
1. The $I_{IO}$ current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 21: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{IO}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.
4. Data based on characterization results. Not tested in production.

**Table 61. Comparator characteristics (continued)**

| Symbol | Parameter | Conditions | | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Comparator hysteresis | No hysteresis (COMPxHYST[1:0]=00) | - | - | 0 | - | mV |
| | | Low hysteresis (COMPxHYST[1:0]=01) | High speed mode | 3 | 8 | 13 | |
| | | | All other power modes | 5 | | 10 | |
| | | Medium hysteresis (COMPxHYST[1:0]=10) | High speed mode | 7 | 15 | 26 | |
| | | | All other power modes | 9 | | 19 | |
| | | High hysteresis (COMPxHYST[1:0]=11) | High speed mode | 18 | 31 | 49 | |
| | | | All other power modes | 19 | | 40 | |

1. Data based on characterization results, not tested in production.
2. For more details and conditions see *Figure 29: Maximum $V_{REFINT}$ scaler startup time from power down*.

**Figure 29. Maximum $V_{REFINT}$ scaler startup time from power down**

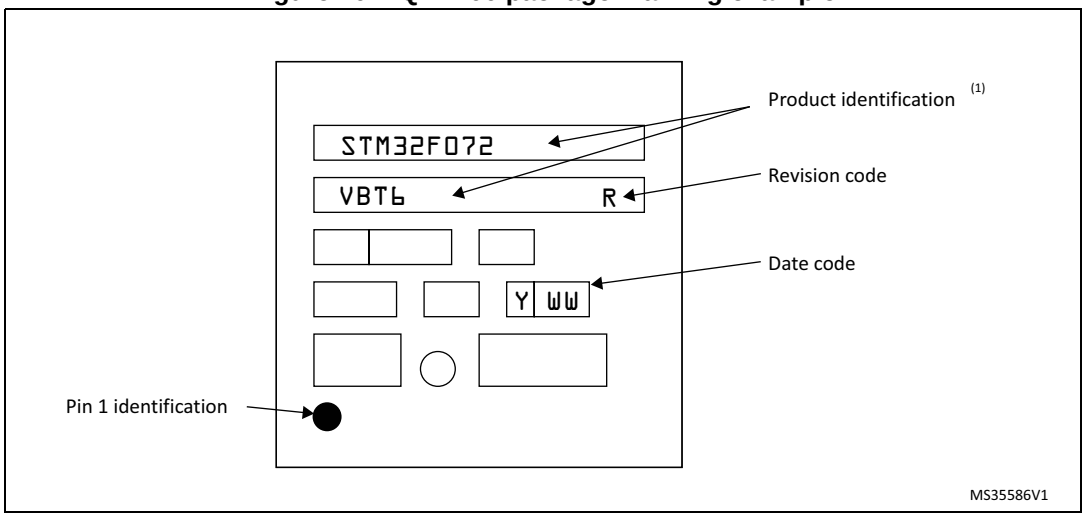


### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 40. LQFP100 package marking example**



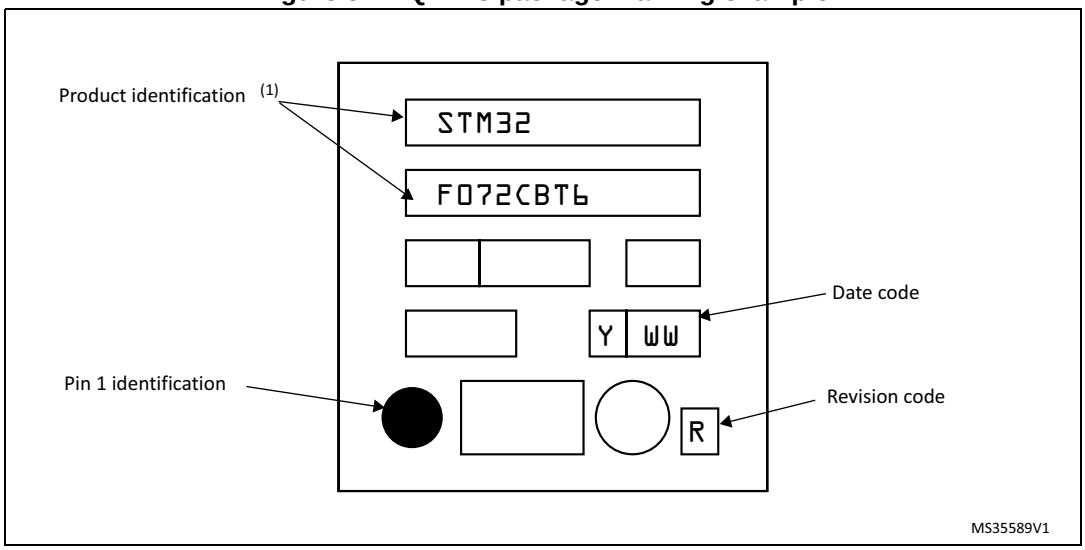

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 51. LQFP48 package marking example**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F072x8/xB at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW:

$P_{Dmax}$= 175 + 272 = 447 mW

Using the values obtained in *Table 80* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

*Note: With this given $P_{Dmax}$ we can find the $T_{Amax}$ allowed for a given device temperature range (order code suffix 6 or 7).*

*Suffix 6: $T_{Amax} = T_{Jmax}$ - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C*

*Suffix 7: $T_{Amax} = T_{Jmax}$ - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C*

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum temperature $T_{Amax}$ = 100 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 20 mA × 3.5 V= 70 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW

Using the values obtained in *Table 80* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 55* to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

**Figure 55. LQFP64 $P_D$ max versus $T_A$**