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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072cbu7tr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F072x8/xB microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F072x8/xB microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two I^2Cs, two SPI/I^2S, one HDMI CEC and four USARTs), one USB Full-speed device (crystal-less), one CAN, one 12-bit ADC, one 12-bit DAC with two channels, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F072x8/xB microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F072x8/xB microcontrollers include devices in seven different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F072x8/xB microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).Refer to *Table 28: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- Periodic wakeup unit with programmable resolution and period.
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I^2C)

Up to two I^2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on most of the associated I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I^2C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts

Table 13. STM32F072x8/xB pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	LQFP48/UFQFPN48	WLCSP49					Alternate functions	Additional functions
B4	93	C3	59	43	D4	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_IO4	-
A4	94	B4	60	44	A5	BOOT0	I	B	-	Boot memory selection	
A3	95	B3	61	45	B5	PB8	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-
B3	96	A3	62	46	C5	PB9	I/O	FTf	-	SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX	-
C3	97	-	-	-	-	PE0	I/O	FT	-	EVENTOUT, TIM16_CH1	-
A2	98	-	-	-	-	PE1	I/O	FT	-	EVENTOUT, TIM17_CH1	-
D3	99	D4	63	47	A6	VSS	S	-	-	Ground	
C4	100	E4	64	48	A7	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. PC6, PC7, PC8, PC9, PA8, PA9, PA10, PA11, PA12, PA13, PF6, PA14, PA15, PC10, PC11, PC12, PD0, PD1 and PD2 I/Os are supplied by VDDIO2.
4. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 30. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Para-meter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSI48	48 MHz	311	326	334	343	322	337	345	354	µA
		HSE bypass, PLL on	48 MHz	152	170(3)	178	182(3)	165	184(3)	196	200(3)	
			32 MHz	105	121	126	128	113	129	136	138	
			24 MHz	81.9	95.9	99.5	101	88.7	102	107	108	
		HSE bypass, PLL off	8 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
			1 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
		HSI clock, PLL on	48 MHz	223	244	255	260	245	265	279	284	
			32 MHz	176	195	203	206	193	212	221	224	
			24 MHz	154	171	178	181	168	185	192	195	
		HSI clock, PLL off	8 MHz	74.2	83.4	86.4	87.3	83.4	92.5	95.3	96.6	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 34. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3 V C =C_{INT}	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V_{DDIOx} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DDIOx} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V_{DDIOx} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DDIOx} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.64	
			8 MHz	1.25	
			16 MHz	3.24	
			24 MHz	5.02	
		V_{DDIOx} = 3.3 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	
		V_{DDIOx} = 2.4 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.66	
			8 MHz	1.43	
			16 MHz	2.45	
			24 MHz	4.97	

1. C_S = 7 pF (estimated value).

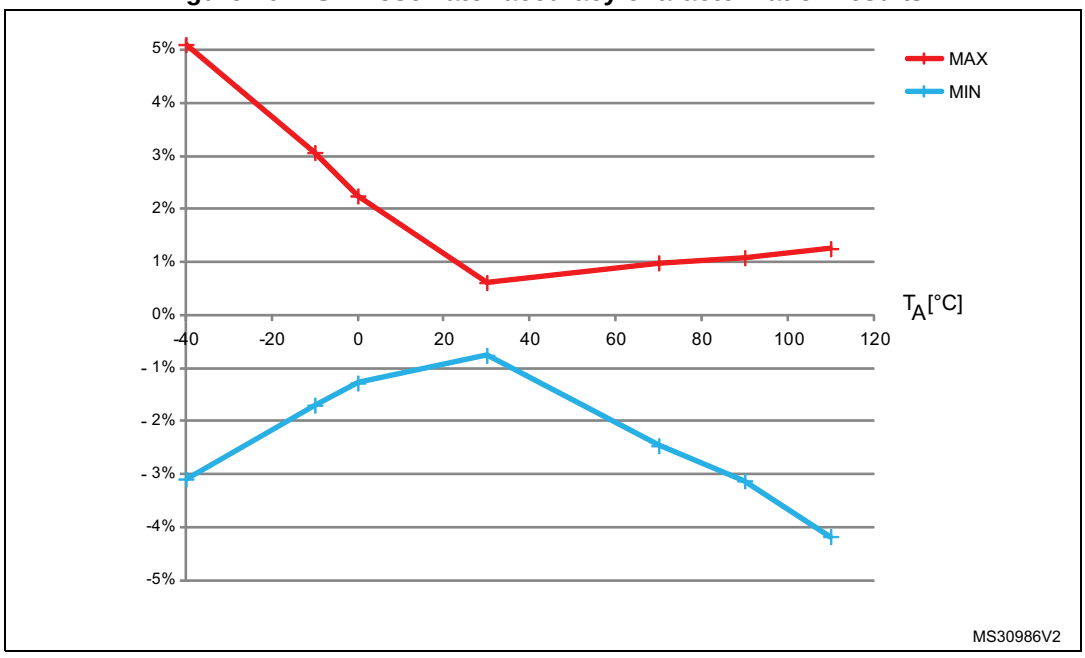
High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 42. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 105 °C	–4.2(3)	-	5.1(3)	%
		T_A = –10 to 85 °C	–3.2(3)	-	3.1(3)	%
		T_A = 0 to 70 °C	–2.5(3)	-	2.3(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	150(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 20. HSI14 oscillator accuracy characterization results



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 21: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 21: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 54. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 6 mA $V_{DDIOx} \geq 2$ V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	
V_{OL}(4)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA	-	0.4	V
V_{OH}(4)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	V
V_{OLFm+}(3)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
		$\|I_{IO}\|$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 21: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.
4. Data based on characterization results. Not tested in production.

Table 65. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 66. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.22 Communication interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 67. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 68* for SPI or in *Table 69* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 68. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

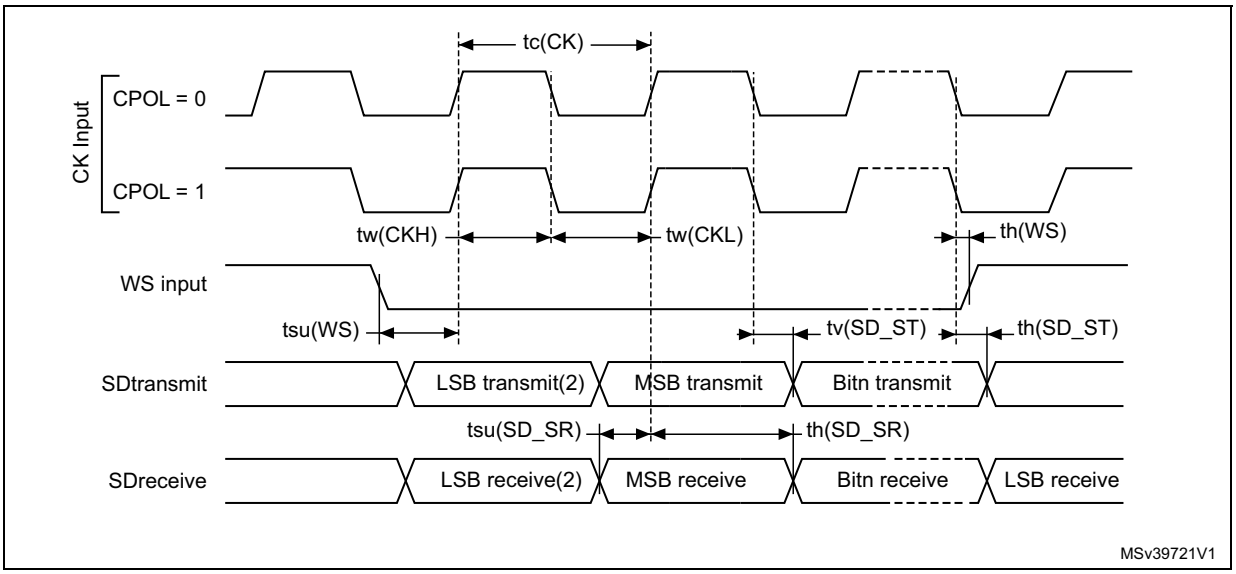
1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Table 69. I²S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$(2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(2)		Slave receiver	0.5	-	
$t_{v(SD\_MT)}$(2)	Data output valid time	Master transmitter	-	4	
$t_{v(SD\_ST)}$(2)		Slave transmitter	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter	0	-	
$t_{h(SD\_ST)}$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/f_{PLCLK} = 125 ns.

Figure 33. I²S slave timing diagram (Philips protocol)



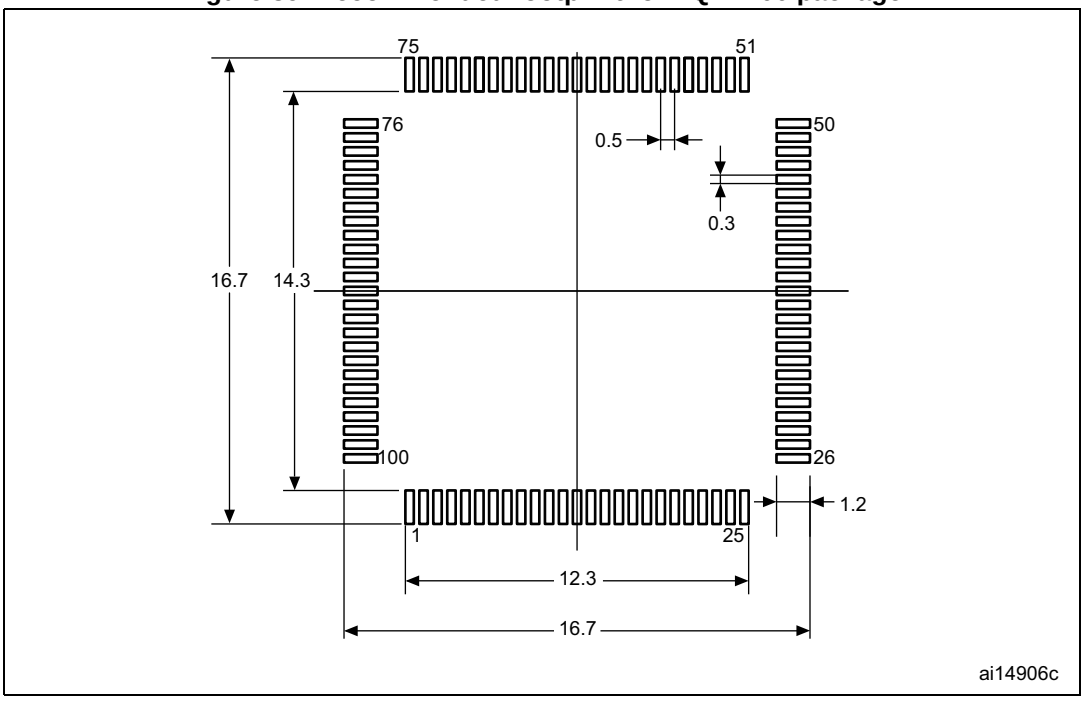
1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 73. LQPF100 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. Recommended footprint for LQFP100 package



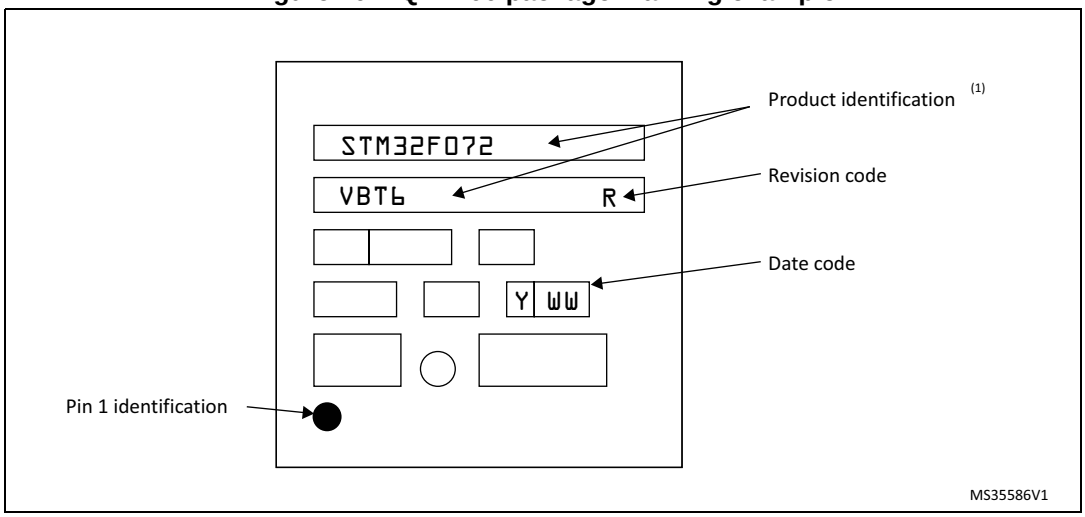
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 40. LQFP100 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 74. UFBGA64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. Recommended footprint for UFBGA64 package

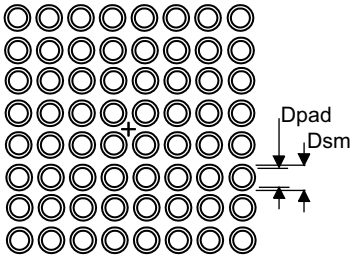


Table 75. UFBGA64 recommended PCB design rules

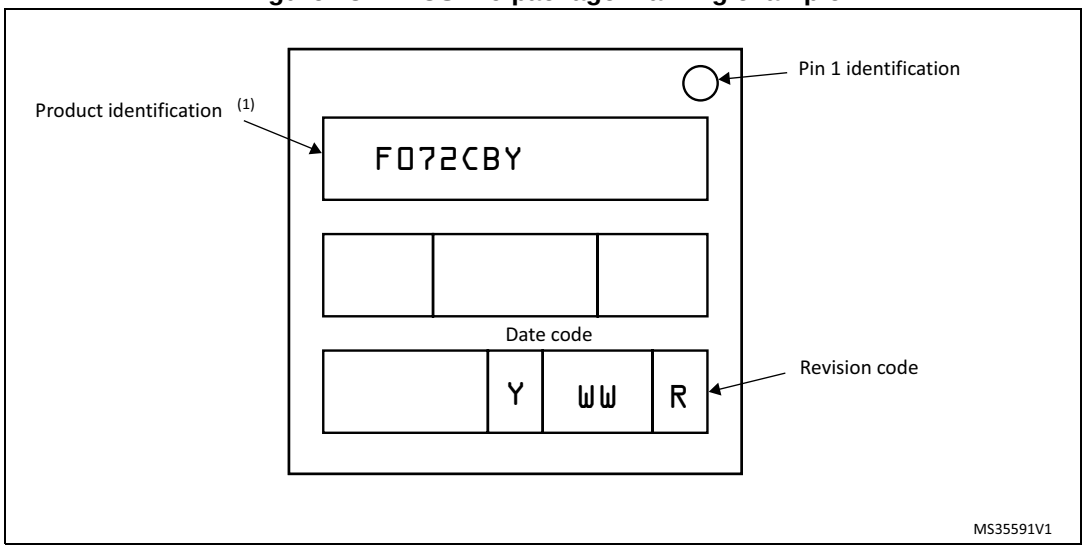
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 48. WLCSP49 package marking example



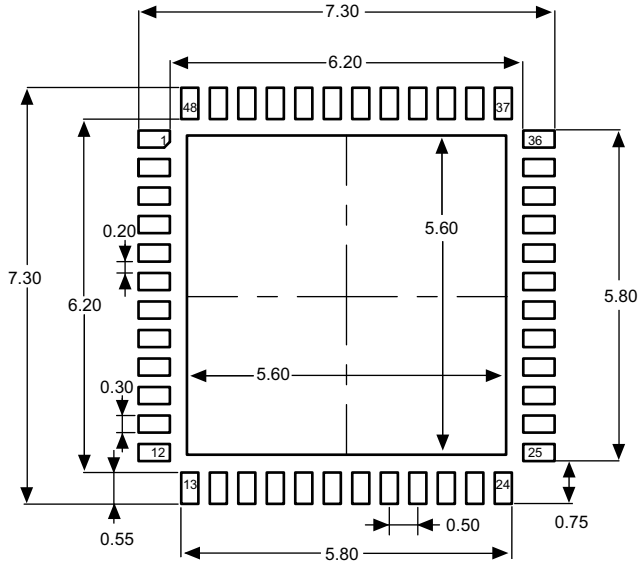
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 79. UFQFPN48 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 53. Recommended footprint for UFQFPN48 package



1. Dimensions are expressed in millimeters.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 81. Ordering information scheme

Example: STM32 F 072 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

072 = STM32F072xx

Pin count

C = 48/49 pins

R = 64 pins

V = 100 pins

User code memory size

8 = 64 Kbyte

B = 128 Kbyte

Package

H = UFBGA

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = –40 to 85 °C

7 = –40 to 105 °C

Options

xxx = code ID of programmed parts (includes packing type)

TR = tape and reel packing

blank = tray packing