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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072r8t6tr

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2 Description

The STM32F072x8/xB microcontrollers incorporate the high-performance ARM[®] Cortex[®]-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two I²Cs, two SPI/I²S, one HDMI CEC and four USARTs), one USB Full-speed device (crystal-less), one CAN, one 12-bit ADC, one 12-bit DAC with two channels, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F072x8/xB microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F072x8/xB microcontrollers include devices in seven different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F072x8/xB microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.



Analog 1/O group	Number of capacitive sensing channels			
	STM32F072Vx	STM32F072Rx	STM32F072Cx	
G1	3	3	3	
G2	3	3	3	
G3	3	3	2	
G4	3	3	3	
G5	3	3	3	
G6	3	3	3	
G7	3	0	0	
G8	3	0	0	
Number of capacitive sensing channels	24	18	17	

Table 6. Number of capacitive sensing channels available on STM32F072x8/xB devices

3.14 Timers and watchdogs

The STM32F072x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 7 compares the features of the different timers.

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
General purpose	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

Table 7. Timer feature comparison



The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- Periodic wakeup unit with programmable resolution and period.
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I²C)

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on most of the associated I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	 Extra filtering capability vs. standard requirements Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts



USART modes/features ⁽¹⁾	USART1 and USART2	USART3 and USART4
IrDA SIR ENDEC block	Х	-
LIN mode	Х	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	Х	-
Auto baud rate detection	Х	-
Driver Enable	X	Х

Table 10. STM32F072x8/xB USART ir	mplementation (continued)

1. X = supported.

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I²S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F0	72x8/xB SPI/I ² S	implementation
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SPI features ⁽¹⁾	SPI1 and SPI2
Hardware CRC calculation	Х
Rx/Tx FIFO	Х
NSS pulse mode	Х
I ² S mode	Х
TI mode	Х

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory



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Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	-
PE8	TIM1_CH1N	-
PE9	TIM1_CH1	-
PE10	TIM1_CH2N	-
PE11	TIM1_CH2	-
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 18. Alternate functions selected through GPIOE_AFR registers for port E

Table 19. Alternate functions available on port F

	•
Pin name	AF
PF0	CRS_SYNC
PF1	-
PF2	EVENTOUT
PF3	EVENTOUT
PF6	-
PF9	TIM15_CH1
PF10	TIM15_CH2



Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
AIIDZ	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
AHB1	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
APB	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 20. STM32F072x8/xB peripheral register boundary addresses

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6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics* and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Min	Max	Unit
V _{DD} -V _{SS}	External main supply voltage	- 0.3	4.0	V
V _{DDIO2} -V _{SS}	External I/O supply voltage	- 0.3	4.0	V
$V_{DDA} - V_{SS}$	External analog supply voltage	- 0.3	4.0	V
V _{DD} -V _{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V _{BAT} –V _{SS}	External backup supply voltage	- 0.3	4.0	V
	Input voltage on FT and FTf pins	V _{SS} - 0.3	V _{DDIOx} + 4.0 ⁽³⁾	V
V(2)	Input voltage on TTa pins	V _{SS} - 0.3	4.0	V
VIN` '	BOOT0	0	9.0	V
	Input voltage on any other pin	V _{SS} - 0.3	4.0	V
ΔV _{DDx}	Variations between different V_{DD} power pins	-	50	mV
V _{SSx} - V _{SS}	Variations between all the different ground pins	-	50	mV
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	see Section 6.3 sensitivity chara	.12: Electrical acteristics	-

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to *Table 22: Current characteristics* for the maximum allowed injected current values.

3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.



6.3 Operating conditions

6.3.1 General operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit		
f _{HCLK}	Internal AHB clock frequency	-	0	48	Mu-		
f _{PCLK}	Internal APB clock frequency	-	0	48	IVITIZ		
V _{DD}	Standard operating voltage	-	2.0	3.6	V		
V _{DDIO2}	I/O supply voltage	Must not be supplied if V_{DD} is not present	1.65	3.6	V		
	Analog operating voltage (ADC and DAC not used)	Must have a potential equal	V_{DD}	3.6	V		
⊻DDA	Analog operating voltage (ADC and DAC used)	to or higher than V _{DD}	2.4	3.6	V		
V _{BAT}	Backup operating voltage	-	1.65	3.6	V		
		TC and RST I/O	-0.3	V _{DDIOx} +0.3	V		
V _{IN}	I/O input voltage	TTa I/O	-0.3	V _{DDA} +0.3 ⁽¹⁾			
		FT and FTf I/O -0.3 5.5 ⁽			v		
		BOOT0	0	5.5			
		UFBGA100	-	364			
	Power dissipation at $T_A = 85 \degree C$ for suffix $6 \circ T_A = 105 \degree C$ for	LQFP100 -		476			
		UFBGA64	-	308	mW		
PD		LQFP64	-	455			
	suffix 7 ⁽²⁾	LQFP48	-	370			
		UFQFPN48	-	625			
		WLCSP49	-	408	1		
	Ambient temperature for the	Maximum power dissipation	-40	85	°C		
т	suffix 6 version	Low power dissipation ⁽³⁾	-40	105	C		
IA	Ambient temperature for the	Maximum power dissipation	-40	105	°C		
	suffix 7 version	Low power dissipation ⁽³⁾ –40 125		125	C		
T.		Suffix 6 version	-40	105	°C		
IJ		Suffix 7 version	-40	125	°C		

Table 24. General operating conditions

1. For operation with a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up resistor must be disabled.

2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} . See Section 7.8: Thermal characteristics.

 In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see Section 7.8: Thermal characteristics).



							-		0011			
					V _{DDA}	= 2.4 V	,		V _{DDA} = 3.6 V			
Symbol	Para- meter	Conditions (1)	s f _{HCLK}	Tun	Max @ T _A ⁽²⁾		Tun	Max @ T _A ⁽²⁾			Unit	
				тур	25 °C	85 °C	105 °C	тур	25 °C	85 °C	105 °C	1
		HSI48	48 MHz	311	326	334	343	322	337	345	354	
		HSE	48 MHz	152	170 ⁽³⁾	178	182 ⁽³⁾	165	184 ⁽³⁾	196	200 ⁽³⁾	
	Supply current in Run or Sleep mode, code executing	bypass, PLL on	32 MHz	105	121	126	128	113	129	136	138	
			24 MHz	81.9	95.9	99.5	101	88.7	102	107	108]
		HSE	8 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
I _{DDA}		1 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	μA	
	from		48 MHz	223	244	255	260	245	265	279	284	
	Flash memory	HSI clock, PLL on	32 MHz	176	195	203	206	193	212	221	224	
	or RAM		24 MHz	154	171	178	181	168	185	192	195	
		HSI clock, PLL off	8 MHz	74.2	83.4	86.4	87.3	83.4	92.5	95.3	96.6	

Table 30. Typical and maximum current consumption from the $\rm V_{\rm DDA}$ supply

 Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.

2. Data based on characterization results, not tested in production unless otherwise specified.

3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).



Sym- Para-					Typ @V _{DD} (V _{DD} = V _{DDA})					Max ⁽¹⁾			
bol	meter	Conditions		2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 ℃	T _A = 105 °C	Unit
Supply current in	Reg mod osc	gulator in run de, all illators OFF	15.4	15.5	15.6	15.7	15.8	15.9	23 ⁽²⁾	49	68 ⁽²⁾		
I _{DD}	Stop mode	Reg pow osc	ulator in low- ver mode, all illators OFF	3.2	3.3	3.4	3.5	3.6	3.7	8 ⁽²⁾	33	51 ⁽²⁾	
	Supply current in	LSI ON	ON and IWDG	0.8	1.0	1.1	1.2	1.3	1.4	-	-	-	
	Standby mode	LSI OFI	OFF and IWDG =	0.6	0.7	0.9	0.9	1.0	1.1	2.1 ⁽²⁾	2.6	3.1 ⁽²⁾	
Supply current in Stop mode	Supply current in Stop mode	z	Regulator in run mode, all oscillators OFF	2.1	2.2	2.3	2.5	2.6	2.8	3.5 ⁽²⁾	3.6	4.6 ⁽²⁾	
		_A monitoring O	Regulator in low-power mode, all oscillators OFF	2.1	2.2	2.3	2.5	2.6	2.8	3.5 ⁽²⁾	3.6	4.6 ⁽²⁾	μA
	Supply current in	V _{DC}	LSI ON and IWDG ON	2.5	2.7	2.8	3.0	3.2	3.5	-	-	-	
	Standby mode		LSI OFF and IWDG OFF	1.9	2.1	2.2	2.3	2.5	2.6	3.5 ⁽²⁾	3.6	4.6 ⁽²⁾	
	DA Supply current in Stop mode	H.	Regulator in run mode, all oscillators OFF	1.3	1.3	1.4	1.4	1.5	1.5	-	-	-	
		Stop mode	A monitoring Ol	Regulator in low-power mode, all oscillators OFF	1.3	1.3	1.4	1.4	1.5	1.5	-	-	-
	Supply current in	V _{DD}	LSI ON and IWDG ON	1.7	1.8	1.9	2.0	2.1	2.2	-	-	-	
	Standby mode		LSI OFF and IWDG OFF	1.2	1.2	1.2	1.3	1.3	1.4	-	-	-	

Table 31. Typical and maximum consumption in Stop and Standby modes

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).



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Symbol	Parameter	Conditions ⁽¹⁾	I/O toggling frequency (f _{SW})	Тур	Unit
			4 MHz	0.07	
			8 MHz	0.15	
		$C = C_{INT}$	16 MHz	0.31	
			24 MHz	0.53	1
			48 MHz	0.92	
			4 MHz	0.18	
		V _{DDIOx} = 3.3 V	8 MHz	0.37	
		C _{EXT} = 0 pF	16 MHz	0.76	
		$C = C_{INT} + C_{EXT} + C_{S}$	24 MHz	1.39	
			48 MHz	2.188	
			4 MHz	0.32	
		V _{DDIOx} = 3.3 V	8 MHz	0.64	mA
		C_{EXT} = 10 pF C = C _{INT} + C _{EXT} + C _S	16 MHz	1.25	
			24 MHz	2.23	
low	I/O current		48 MHz	4.442	
.200	consumption		4 MHz	0.49	
		$V_{DDIOX} = 3.3 V$ $C_{EXT} = 22 pF$ $C = C_{INT} + C_{EXT} + C_{S}$	8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
			4 MHz	0.64	
		$V_{\text{DDIOX}} = 3.3 \text{ V}$	8 MHz	1.25	
		$C = C_{INT} + C_{EXT} + C_S$	16 MHz	3.24	
			24 MHz	5.02	
		V _{DDIOx} = 3.3 V	4 MHz	0.81	
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.7	
		$C = C_{INT} + C_{EXT} + C_{S}$ $C = C_{int}$	16 MHz	3.67	
		V _{DDIOx} = 2.4 V	4 MHz	0.66	
		$C_{EXT} = 47 \text{ pF}$	8 MHz	1.43	
		$C = C_{INT} + C_{EXT} + C_{S}$	16 MHz	2.45	
		$C = C_{int}$	24 MHz	4.97	

Table 34. Switching output I/O current consumption

1. C_S = 7 pF (estimated value).



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Тур	Max ⁽²⁾	Unit
f _{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R _F	Feedback resistor	-	-	200	-	kΩ
		During startup ⁽³⁾	-	-	8.5	
		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
	HSE current consumption	V _{DD} = 3.3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
I _{DD}		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	mA
		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V _{DD} = 3.3 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
9 _m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

Table 3	39. HSE	oscillator	characteristics

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by design, not tested in production.

3. This consumption level occurs during the first 2/3 of the $t_{\mbox{SU(HSE)}}$ startup time

4. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

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6.3.17 DAC electrical specifications

Symbol	Parameter	Min	Тур	Max	Unit	Comments
V _{DDA}	Analog supply voltage for DAC ON	2.4	-	3.6	V	-
D (1)	Resistive load with buffer	5	-	-	kΩ	Load connected to V _{SSA}
►LOAD` ′	ON	25	-	-	kΩ	Load connected to V _{DDA}
R _O ⁽¹⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V _{SS} to have a 1% accuracy is 1.5 M Ω
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	-	-	V _{DDA} – 0.2	V	$V_{DDA} = 3.6 V \text{ and } (0x155) \text{ and}$ (0xEAB) at $V_{DDA} = 2.4 V$
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	I	-	V _{DDA} – 1LSB	V	excursion of the DAC.
I (1)	DAC DC current	-	-	600	μA	With no load, middle code (0x800) on the input
'DDA'	mode ⁽²⁾	I	-	700	μA	With no load, worst code (0xF1C) on the input
DNL ⁽³⁾	Differential non linearity Difference between two	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
	consecutive code-1LSB)	-	-	±2	LSB	Given for the DAC in 12-bit configuration
	Integral non linearity (difference between	I	-	±1	LSB	Given for the DAC in 10-bit configuration
INL ⁽³⁾	and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±4	LSB	Given for the DAC in 12-bit configuration
	Offset error	-	-	±10	mV	-
Offset ⁽³⁾	(difference between measured value at Code	-	-	±3	LSB	Given for the DAC in 10-bit at V _{DDA} = 3.6 V
	(0x800) and the ideal value = V _{DDA} /2)	-	-	±12	LSB	Given for the DAC in 12-bit at $V_{DDA} = 3.6 V$

Table	60.	DAC	characteristics
Table	00.	DAO	character istics



Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit					
/4	0	0.1	409.6						
/8	1	0.2	819.2						
/16	2	0.4	1638.4						
/32	3	0.8	3276.8	ms					
/64	4	1.6	6553.6						
/128	5	3.2	13107.2						
/256	6 or 7	6.4	26214.4						

Table 65. IWDG min/max timeout period at 40 kHz (LSI)⁽¹⁾

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	
2	1	0.1706	10.9226	me
4	2	0.3413	21.8453	1115
8	3	0.6826	43.6906	

Table 66. WWDG min/max timeout value at 48 MHz (PCLK)

6.3.22 Communication interfaces

I²C interface characteristics

The I^2C interface meets the timings requirements of the I^2C -bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to Section 6.3.14: I/O port characteristics for the I²C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:



Symbol	Parameter	Min	Max	Unit
t _{AF}	Maximum width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

Table 67. I²C analog filter characteristics⁽¹⁾

1. Guaranteed by design, not tested in production.

- 2. Spikes with widths below $t_{AF(min)}$ are filtered.
- 3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 68* for SPI or in *Table 69* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*.

Refer to Section 6.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Symbol	Parameter	Conditions	Min	Мах	Unit	
f _{SCK}	SDI clock froguency	Master mode	-	18		
1/t _{c(SCK)}	SPI Clock frequency	Slave mode	-	18		
t _{r(SCK)} t _{f(SCK)}	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns	
t _{su(NSS)}	NSS setup time	Slave mode	4Tpclk	Tpclk -		
t _{h(NSS)}	NSS hold time	Slave mode	2Tpclk + 10	-		
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode, f _{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1		
t _{su(MI)} t _{su(SI)}	Data input setup time	Master mode	4	-		
		Slave mode	5	-		
t _{h(MI)}	Data input hold time	Master mode	4	-		
t _{h(SI)}		Slave mode	5	-	ns	
t _{a(SO)} ⁽²⁾	Data output access time	Slave mode, f _{PCLK} = 20 MHz	0	3Tpclk		
t _{dis(SO)} ⁽³⁾	Data output disable time	Slave mode	0	18		
t _{v(SO)}	Data output valid time	Slave mode (after enable edge)	-	22.5		
t _{v(MO)}	Data output valid time	Master mode (after enable edge)	-	6		
t _{h(SO)}	Data output hold time	Slave mode (after enable edge)	11.5	-		
t _{h(MO)}		Master mode (after enable edge)	2	2 -		
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%	

Table 68. SPI characteristics ^{(*}

1. Data based on characterization results, not tested in production.

2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z





Figure 34. I²S master timing diagram (Philips protocol)

- 1. Data based on characterization results, not tested in production.
- 2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



		-	<u> </u>	•		
Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Мах
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
CCC	-	-	0.080	-	-	0.0031

Table 73. LQPF100 package mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.





1. Dimensions are expressed in millimeters.



Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Мах	Min	Тур	Мах
А	0.460	0.530	0.600	0.0181	0.0209	0.0236
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

Table 74. UFBGA64 package mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. Recommended footprint for UFBGA64 package



A019_FP_V2

Table 75. UFBGA64 recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm



7.7 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.





1. Drawing is not to scale.

- 2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
- 3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

